GRAVITY+ RTC Design

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On behalf of the GPAO RTC Team

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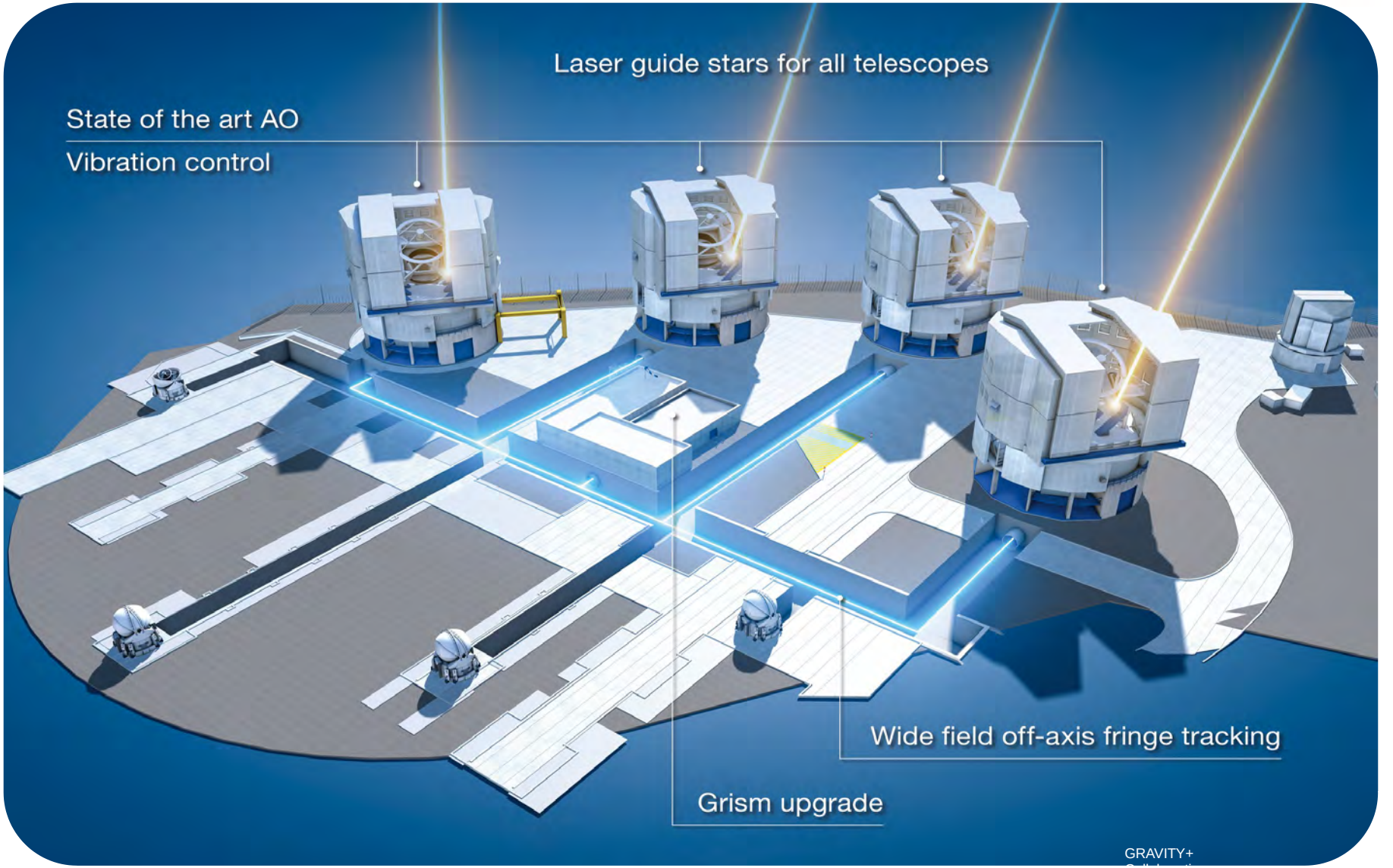
GRAVITY+ Project Overview



- Milestone 1 Review : February 2022
- Milestone 2 Review : July 2022
- Milestone 3 Review : September 2023
- PAE : April 2024
- Hardware to Paranal : July 2024
- Commissioning Start : August 2024

GPAO RTC Hardware Overview

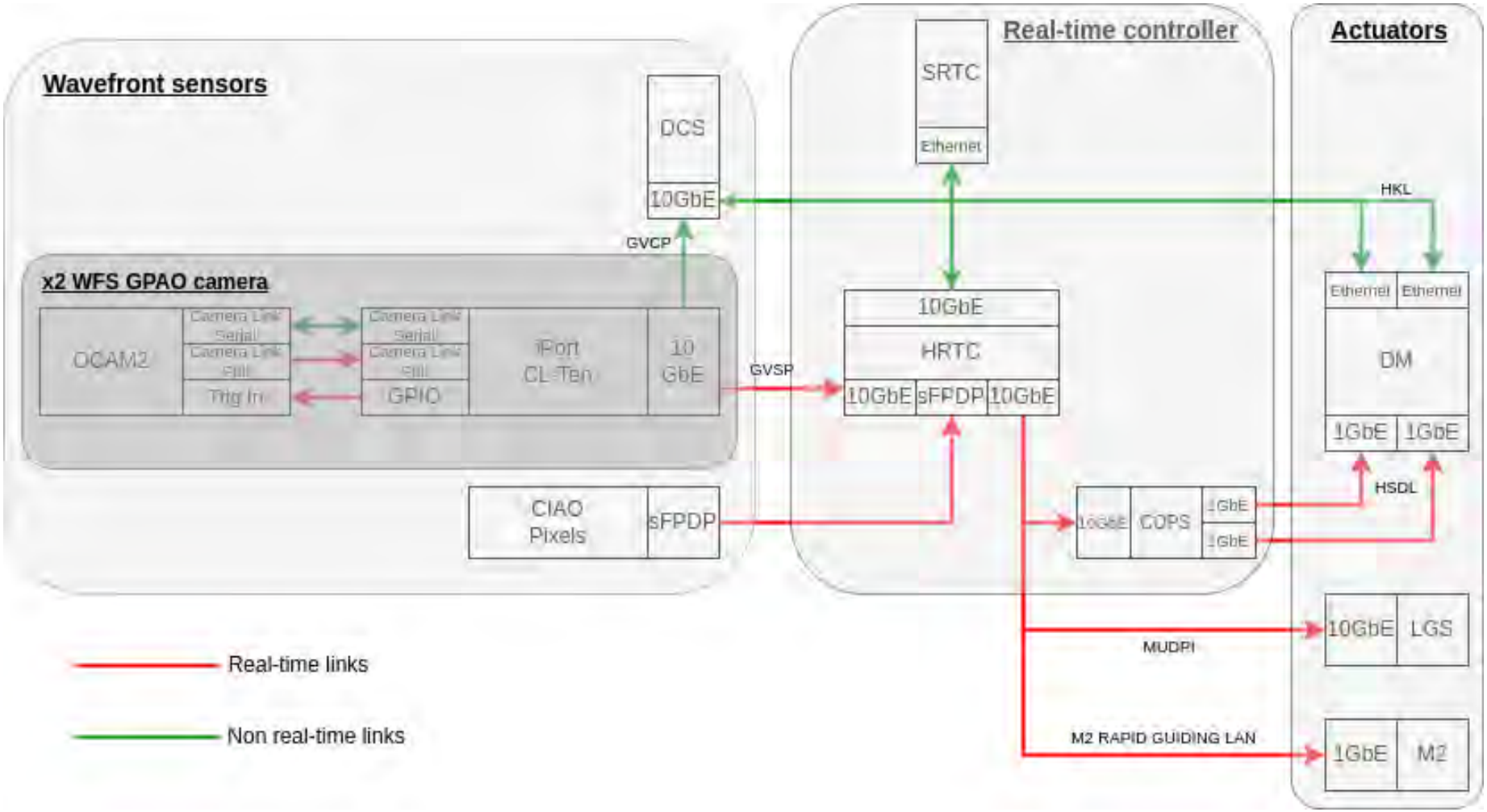
4 RTC Cabinets :
CoolRack CW water cooled 11,61 kW,
800 +150 mm x1200x2100
By Lehmann IT

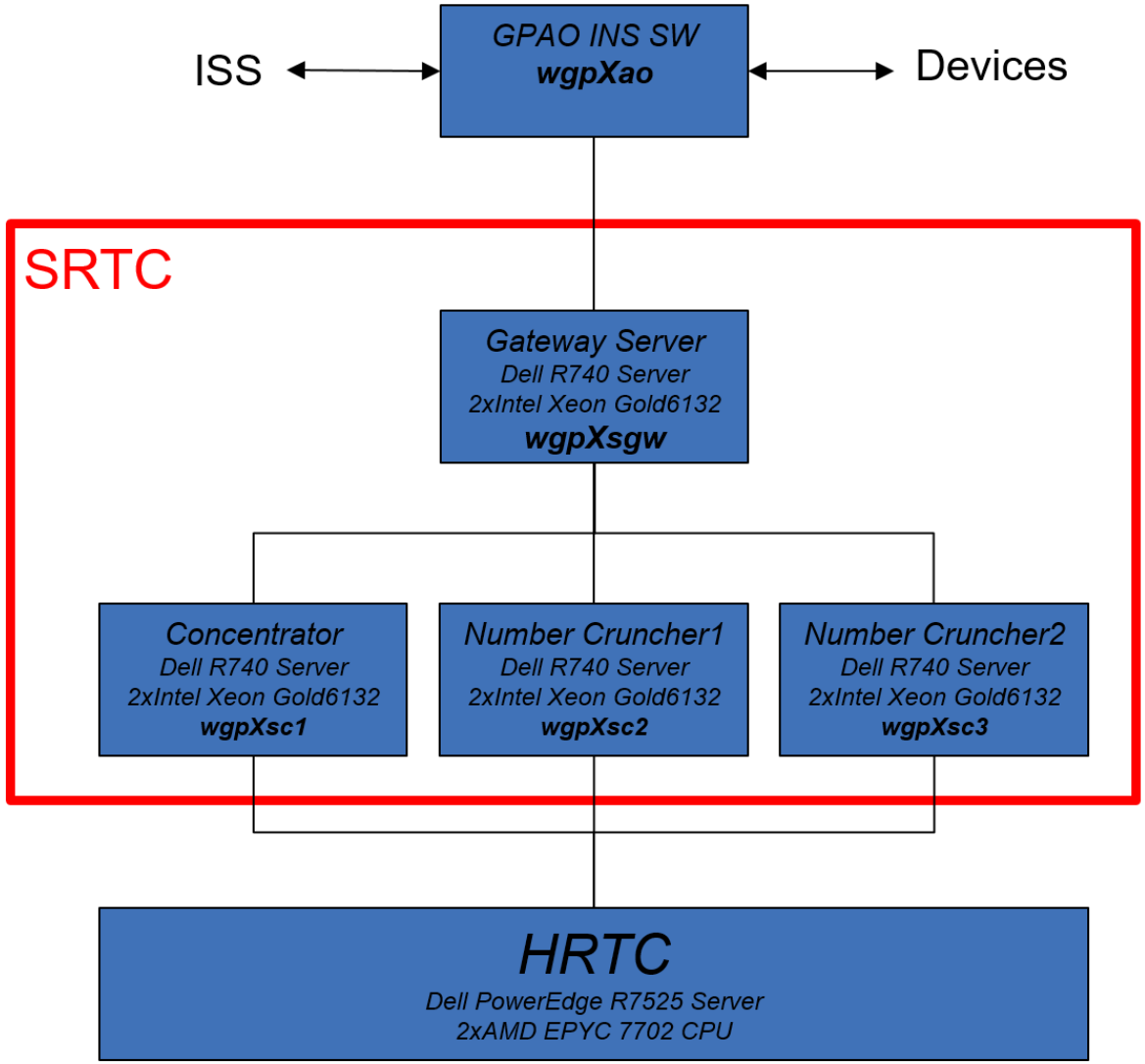
Will be installed in the 4 UT Outer Rings

23 Dell Servers
Cisco Hardware (switches, SFP modules, transceivers)

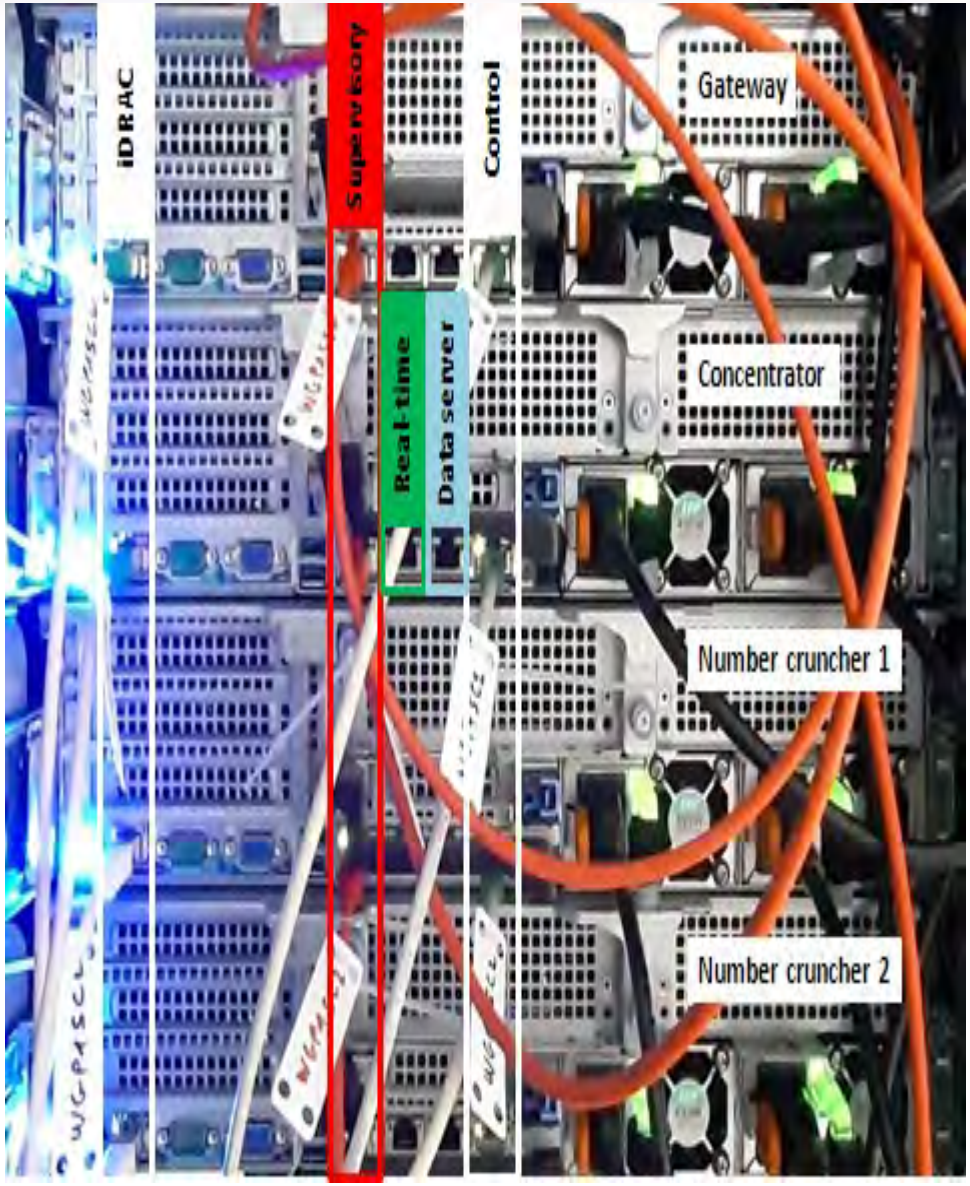
<u>Interface Boards</u> :
Intel X710-T4 NICs
NewWaveDV V5051 sFPDP board

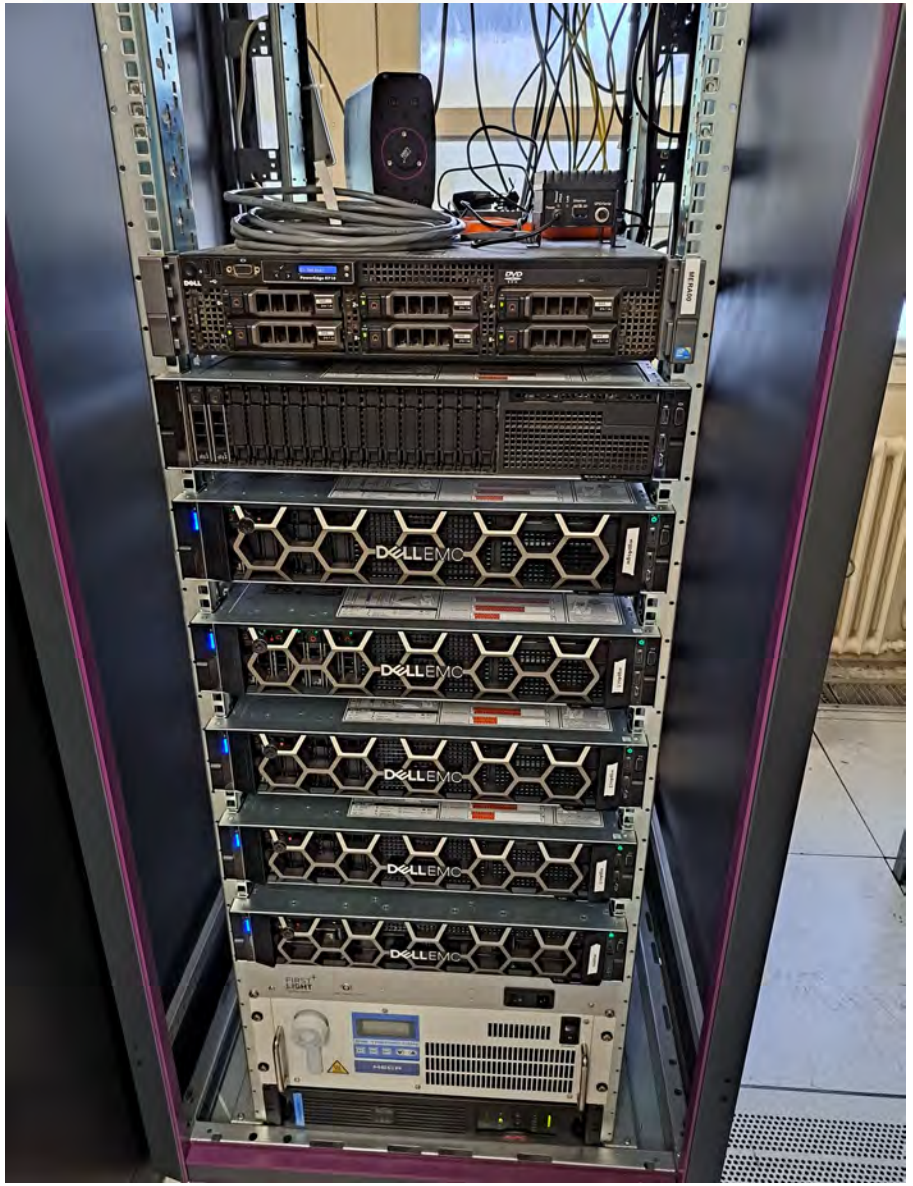
GPAO RTC Design Overview



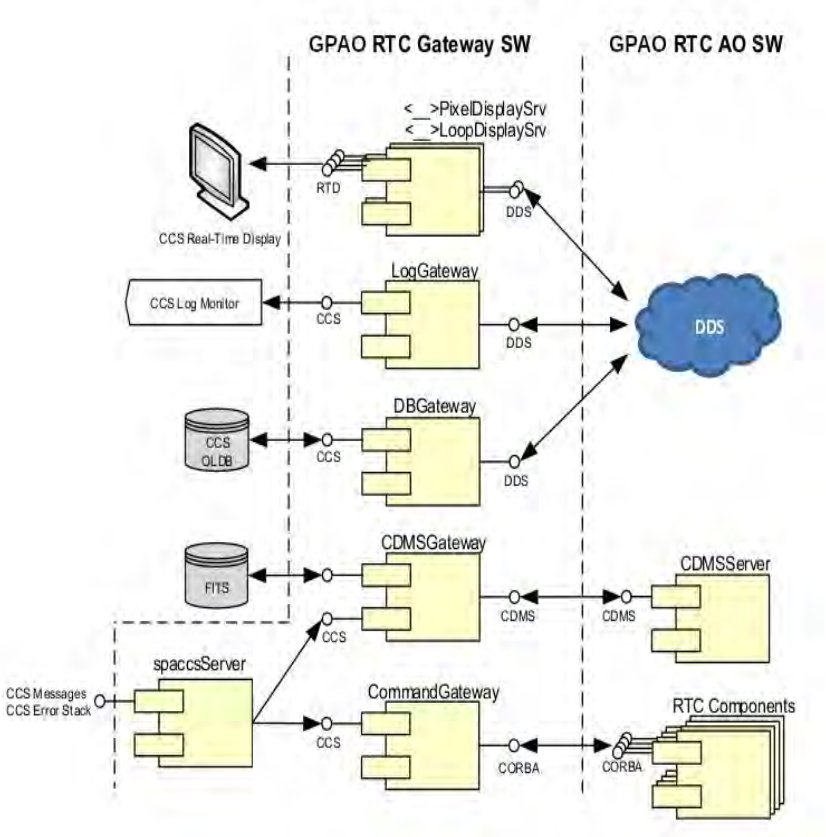

ISS
GPAO INS SW
wgpXao
Devices
SRTC
Gateway Server
Dell R740 Server
2xIntel Xeon Gold6132
wgpXsgw
Concentrator
Dell R740 Server
2xIntel Xeon Gold6132
wgpXsc1
Number Cruncher1
Dell R740 Server
2xIntel Xeon Gold6132
wgpXsc2
Number Cruncher2
Dell R740 Server
2xIntel Xeon Gold6132
wgpXsc3
HRTC
Dell PowerEdge R7525 Server
2xAMD EPYC 7702 CPU

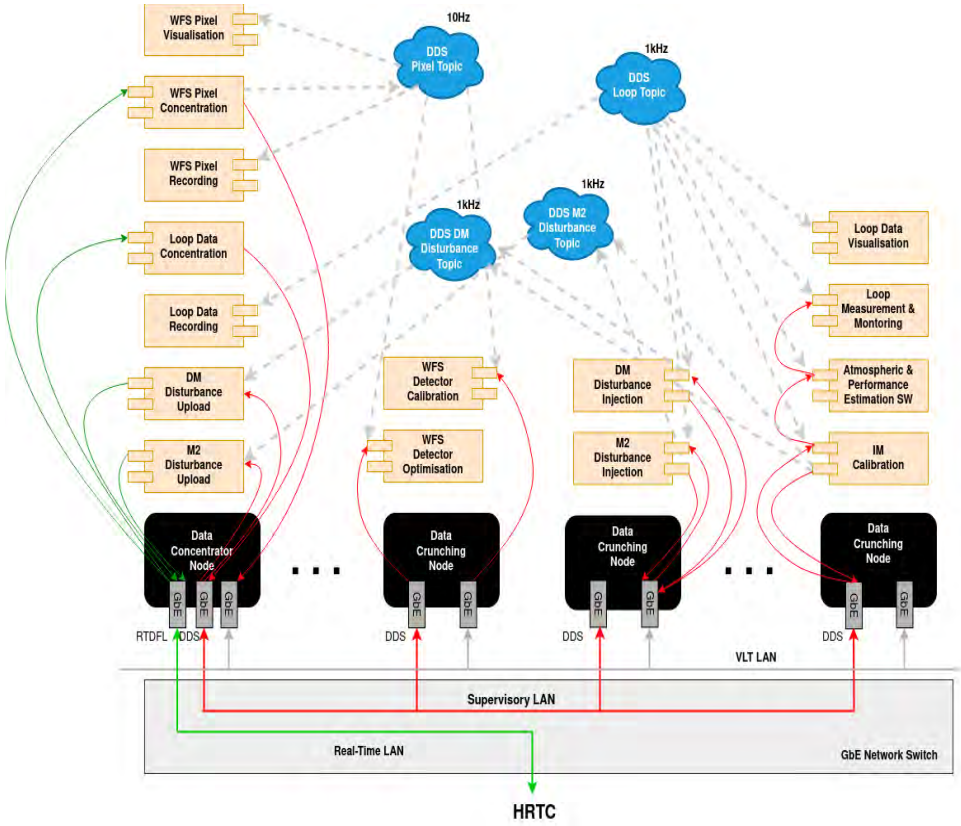
SRTC Overview



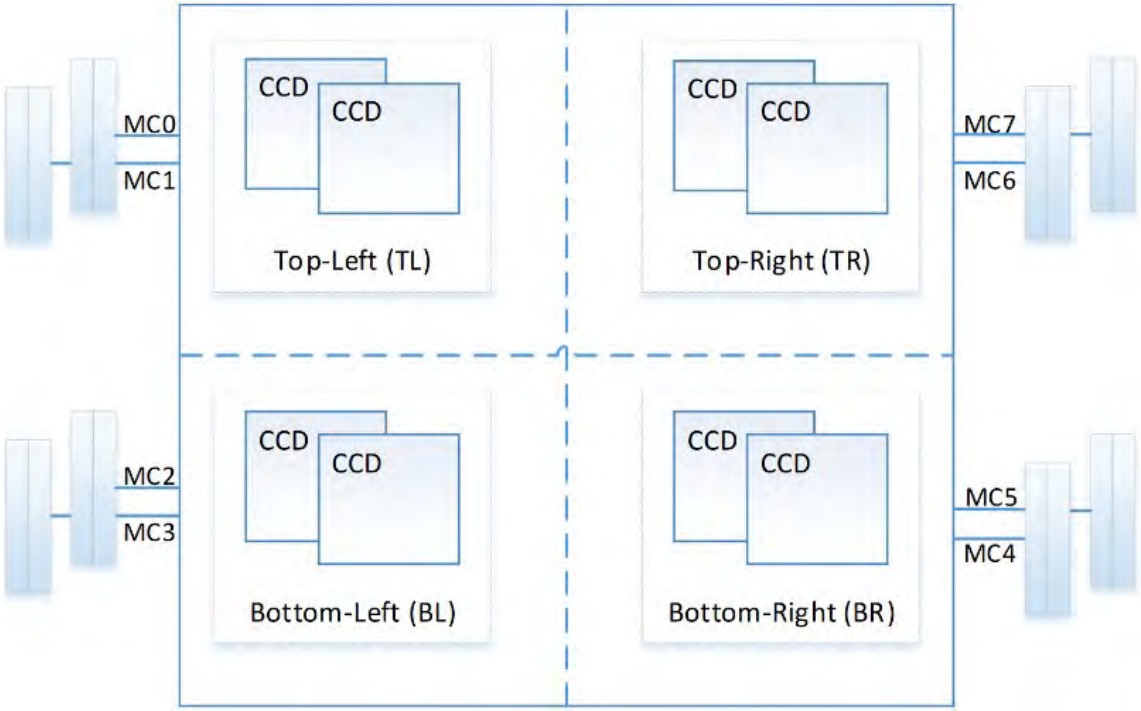


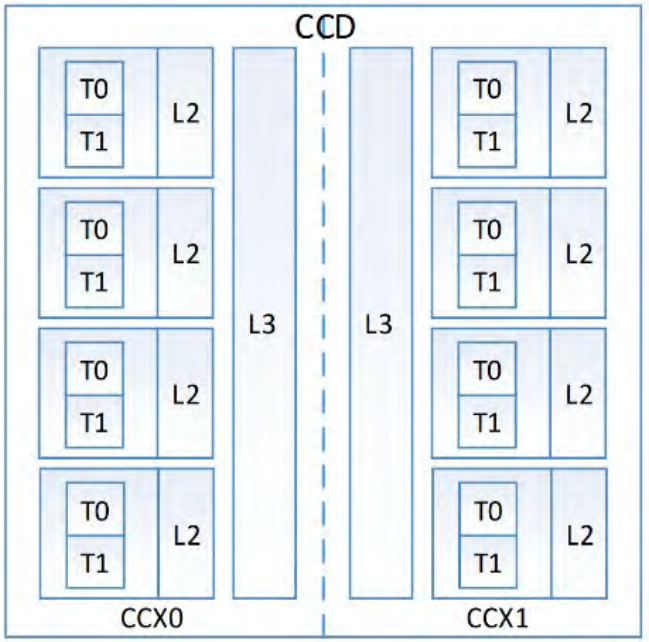
SRTC Overview





HRTC Overview

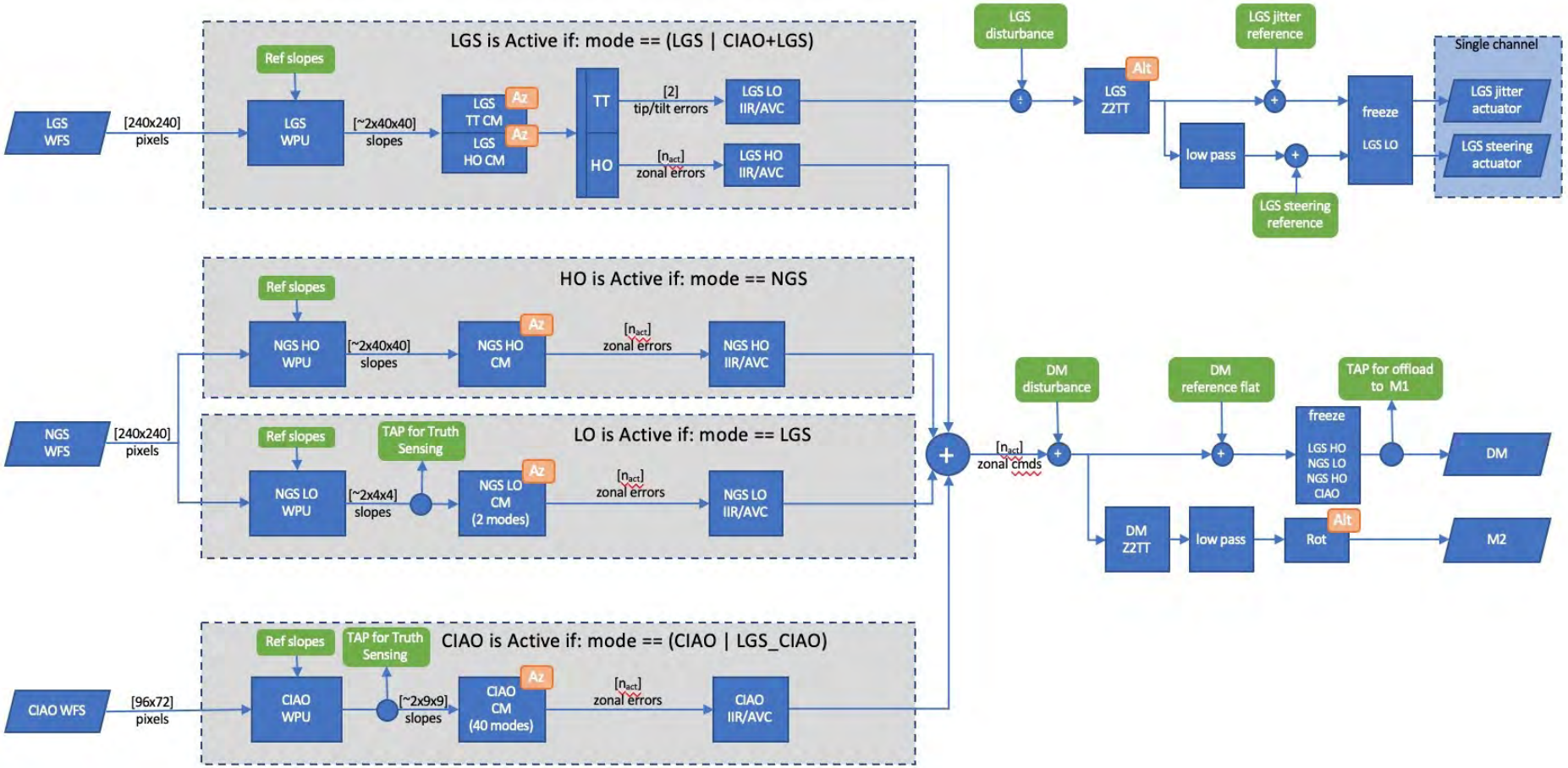




2 x AMD Epyc 7702 CPU « Rome » architecture
- Diskless, using a PXE from CentOS and an *initrd* image
- Isolating specific cores from the operating system scheduler and confines the kernel
- Using non-blocking communications and shared memory areas to exchange intermediate results.
- Processing the data in parallel to their reception as much as possible
- Using IRQ affinity and taking advantage of the NUMA architecture proposed by the Epyc CPU

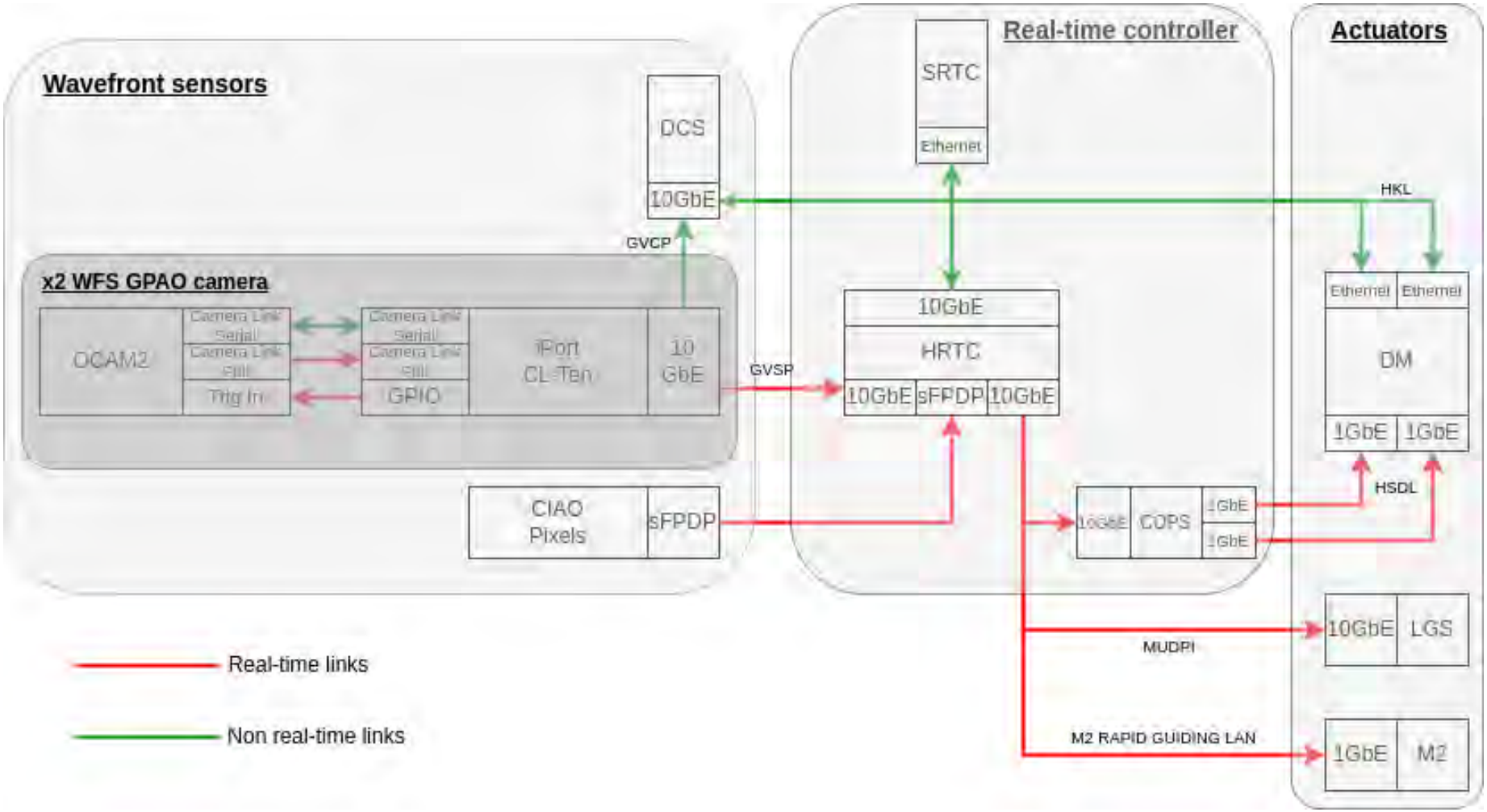
NUMA node 0: HO/LO/CIAO WPU centroider threads;
NUMA node 1: HO/LGS MVM;
NUMA node 2: CIAO sFPDP receiver and CIAO WPU calibrator thread;
NUMA node 3: AWF projection;
NUMA node 4: OS, SPARTA drivers, telemetry;
NUMA node 5: HO/LO GigE RECV and HO/LO WPU (calibrator threads);
NUMA node 6: ALPAO transmitters and DM/M2/Jitter combiners
NUMA node 7: HO/LO AVC and HO/LO/Jitter IIR.

GPAO RTC Design Overview



- GPAO1 : Gateway + HRTC @MPE Garching
- GPAO2 : Full cluster @OCA Nice
- GPAO3 : Gateway + HRTC @ESO Garching
- GPAO4 : Full cluster @LESIA Paris

GPAO Specific Interfaces



OCAM Interface

10 GbE

CISCO C9300-24UX-E

GVSP

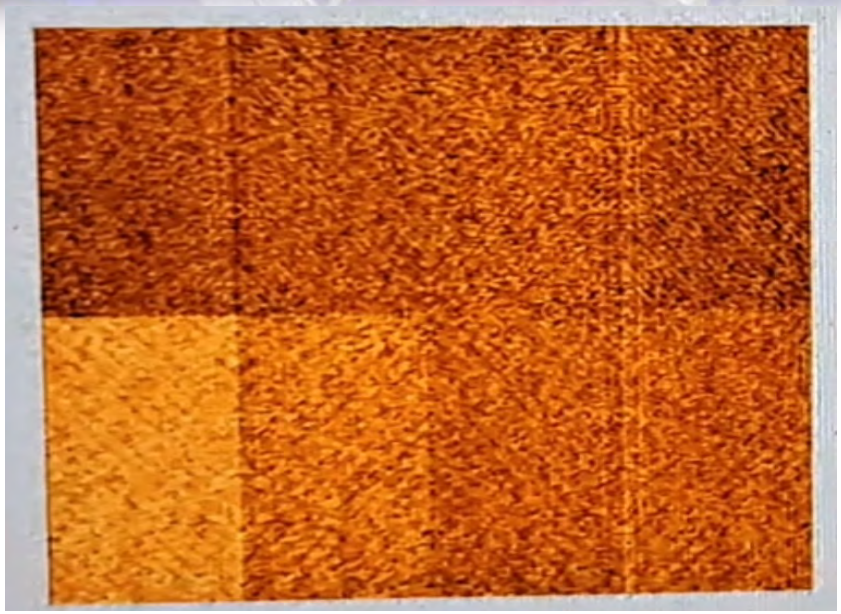
GVCP

Camera Link

HRTC
Dell
PowerEdge
R7525 Server

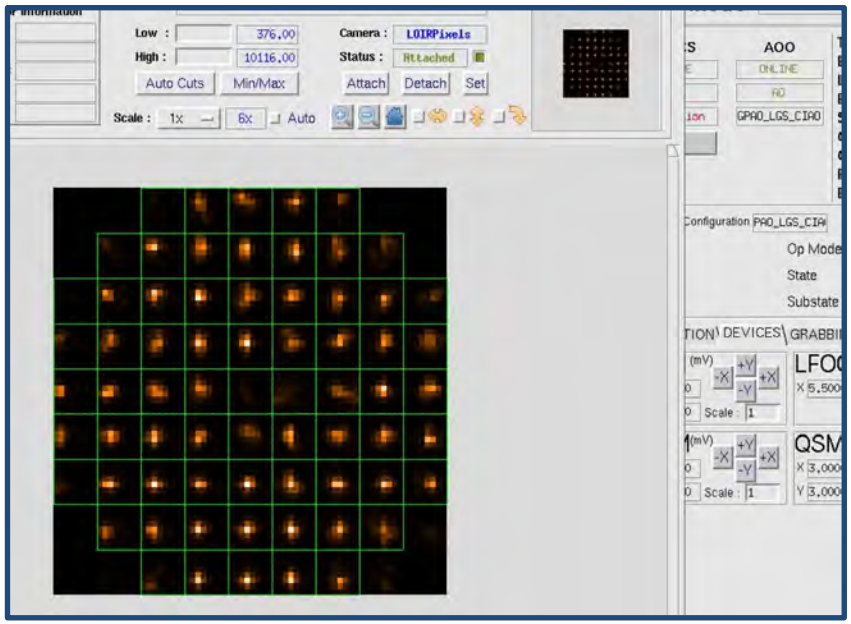
DCS
Dell
PowerEdge
R740 Server

OCAM Interface



Frame size: Height = 121 and Width = 1056.
This setup is mandatory at frame grabber level to correctly obtain the expected
240 x 240 = 57600 pixels

So we are reading in total 8 channels of 66 pixels wide (60 + 6 prescan columns) by 121 pixels high (120 + 1 prescan line)



<u>GVSP principles</u> :
Each packet starts with a GVSP packet leader of 20 bytes.
Each frame starts with a GVSP header of 36 bytes.
Each frame finishes with a GVSP leader of 8 bytes.

Header = 20 + 36 = 56 bytes
Payload = 16 x (20 + 7986) = 128096 bytes
So a useful payload of 16 x 7986 = 127776
= 1056 x 121 bytes as expected
Leader = 20 + 8 = 28 bytes

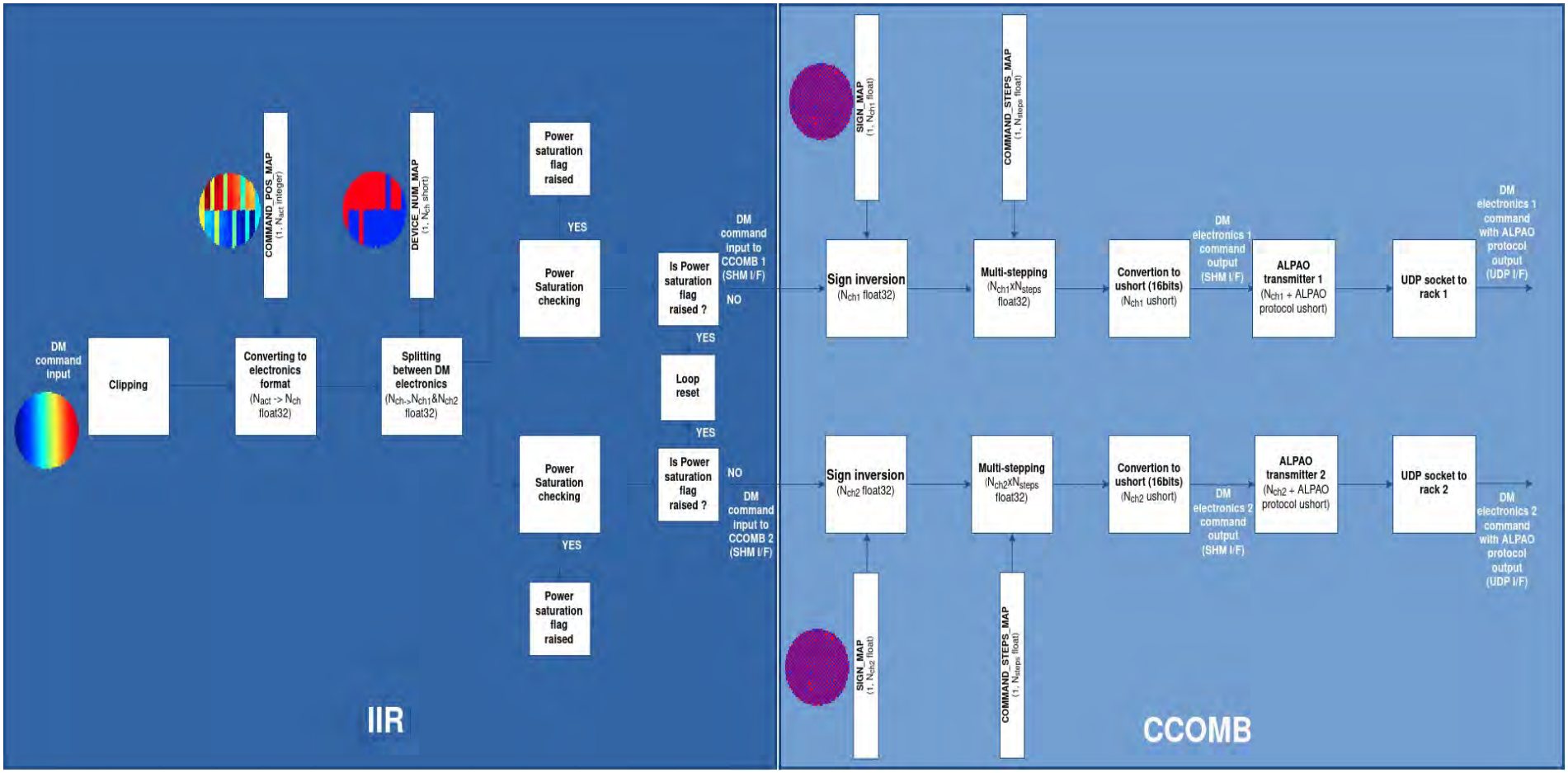
ALPAO UDP-Based Protocol

DM caracteristics :

- Number of actuators : 1432
- Number of channels : 1536
- Number of channels per electronics : 768

Header		Payload	Trailer	
Start of frame	**Start channel**	**Command to the DM *XXXX XXXX XXXX ….***	**End of frame + Checksum**	**Padding**

ALPAO DM Interface



- Based on ESO MUDPI protocol
- To be tested @VCM ESO Garching
- Translation stage needed for UT4 : prototype was implemented by ESO, LCU using VxWorks MUDPI lib can translate MUDPI packets @2kHz into sFPDP

- Based on Rapid Guiding LAN (1GbE)
- Sending alpha/delta corrections to M2 LCU at slower rate
- Booking Mechanism to be implemented
- Switches and Media converters upgrade needed
- To be tested @VCM ESO Garching

GPAO RTC Test Setup

<u>Oscilloscope + Adapter Card from PCIe to DB25 parallel (Startech PEX1P2)</u>

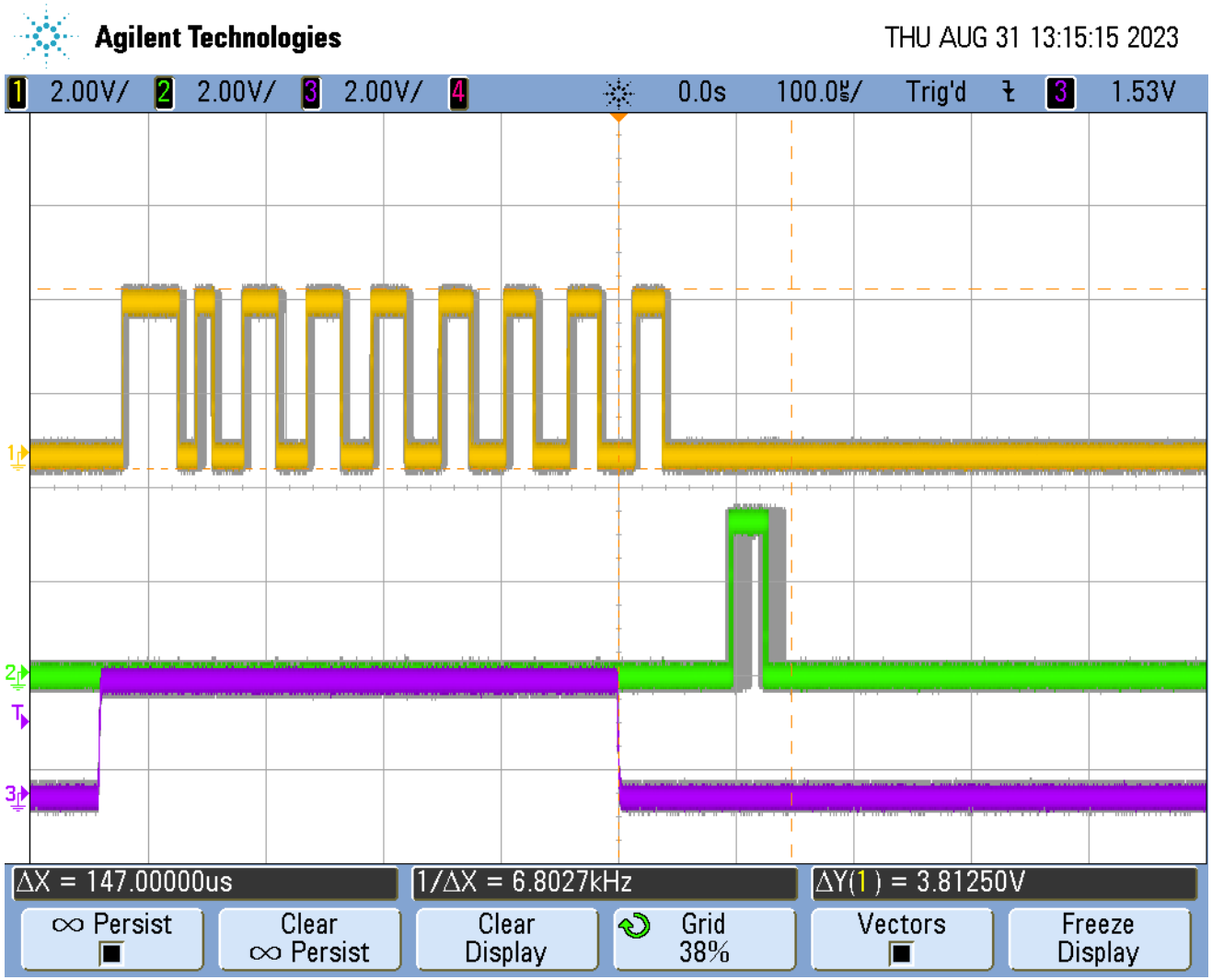
Oscilloscope is plugged at OCAM level and parallel board on HRTC.

Two measurements are made :

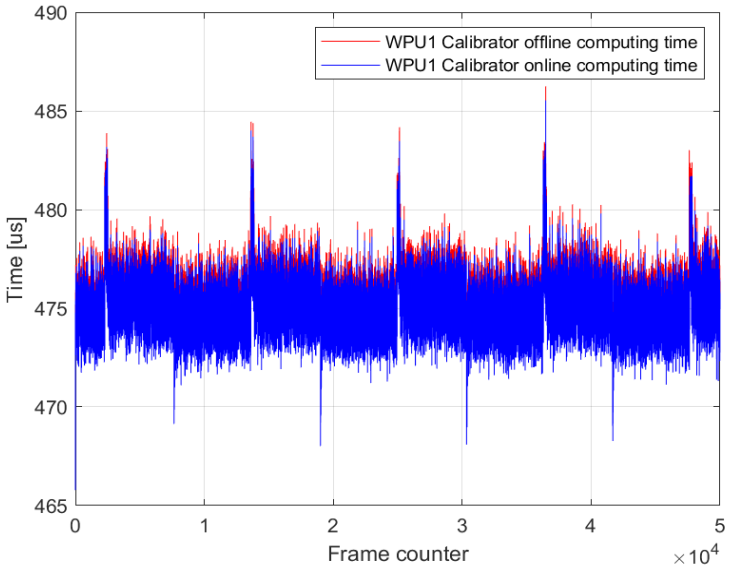
- First one is measuring time for the pixels to arrive to HRTC
- Second is measuring the previous one plus the full HRTC processing time

1st Performance Results

NGS Mode, Closed loop, 0 gain, without disturbance and no CM update



1st Performance Results



min_WPU1_CalibOnline = 465.7859 us

max_WPU1_CalibOnline = 485.5339 us

mean_WPU1_CalibOnline = 474.9323 us

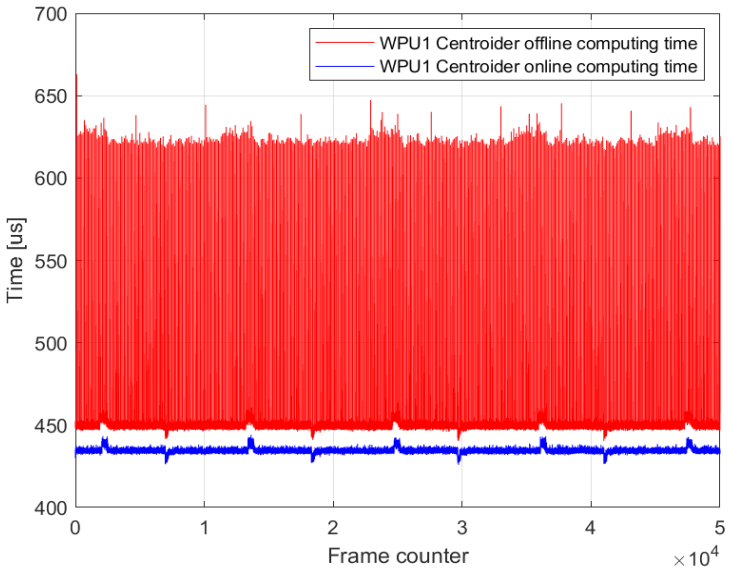
std_WPU1_CalibOnline = 1.0920 us

min_WPU1_CalibOffline = 467.0684 us

max_WPU1_CalibOffline = 486.2453 us

mean_WPU1_CalibOffline = 475.4731 us

std_WPU1_CalibOffline = 1.1086 us



min_WPU1_CentrOnline = 425.8692 us

max_WPU1_CentrOnline = 444.1543 us

mean_WPU1_CentrOnline = 434.2905 us

std_WPU1_CentrOnline = 1.3878

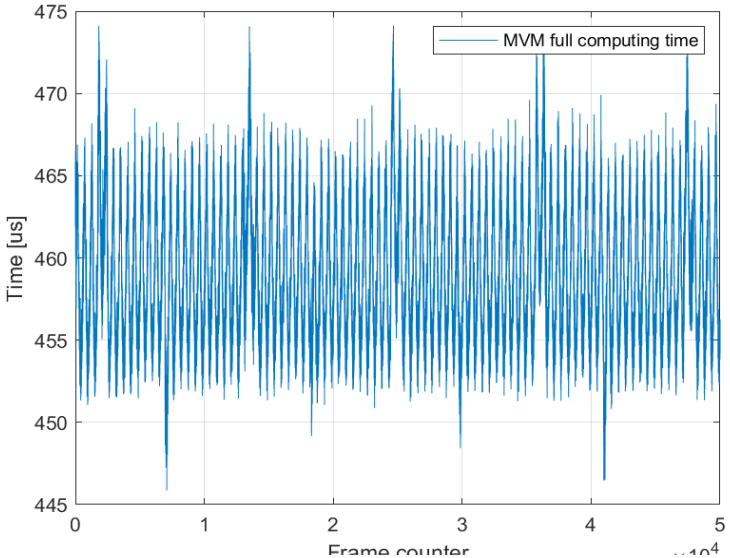
min_WPU1_CentrOffline = 440.4171 us

max_WPU1_CentrOffline = 662.8851 us

mean_WPU1_CentrOffline = 451.5613 us

std_WPU1_CentrOffline = 17.4753 us

1st Performance Results

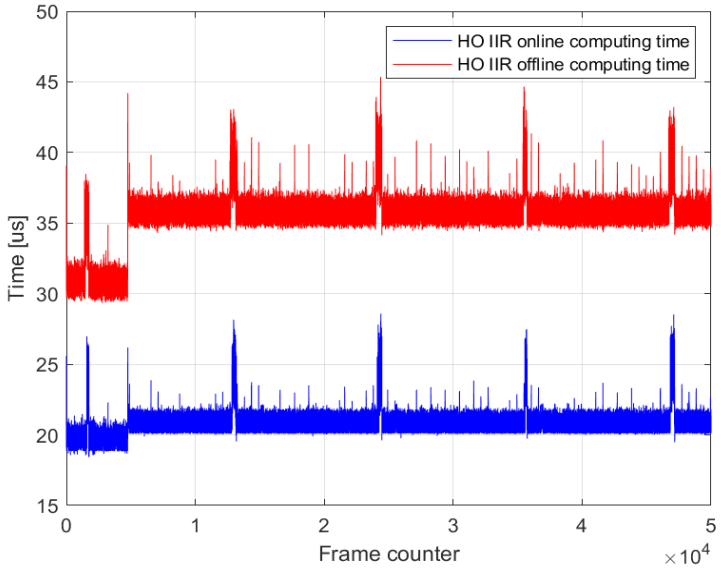


min_MVM_Full = 445.8676 us

max_MVM_Full = 474.1320 us

mean_MVM_Full = 458.8189 us

std_MVM_Full = 4.1732 us



min_HOIIR_online = 18.4355 us

max_HOIIR_online = 28.5850 us

mean_HOIIR_online = 20.9767 us

std_HOIIR_online = 0.8313 us

min_HOIIR_offline = 29.3364 us

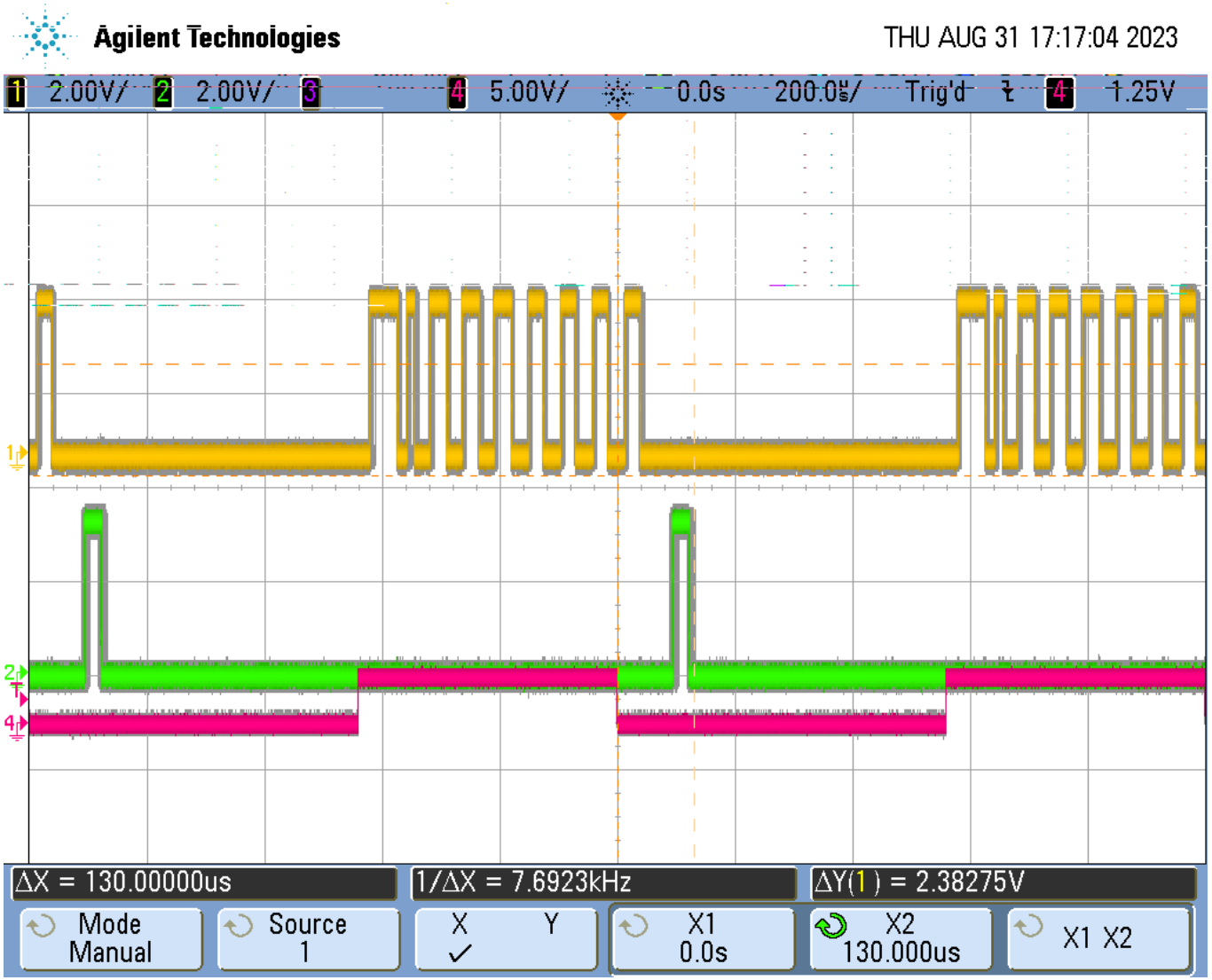
max_HOIIR_offline = 45.3573 us

mean_HOIIR_offline = 35.5698 us

std_HOIIR_offline = 1.7321 us

1st Performance Results : CM Update Optimization

CM update in NGS mode with 16 cores for MVM, IO thread pull



Hardware timestamping using NVIDIA Mellanox ConnectX®-6 Dx, 100GbE Dual-Port
These boards will be plugged on the HRTC to measure the time between pixel reception and the output of HRTC, including the commands to the actuators, DM but also Jitter and M2.

It will be also useful to check the elapsed time between two DM commands for example.

Conclusion