LAB : Laboratoire d'Astrophysique de Bordeaux

# Digitizer and Correlator Upgrade

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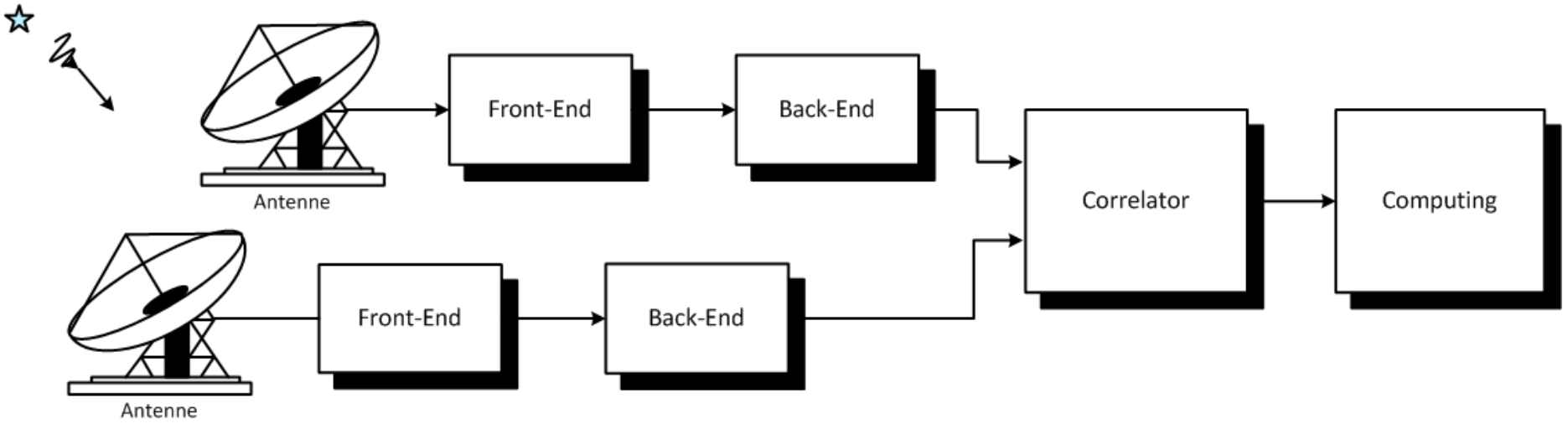
## Outline

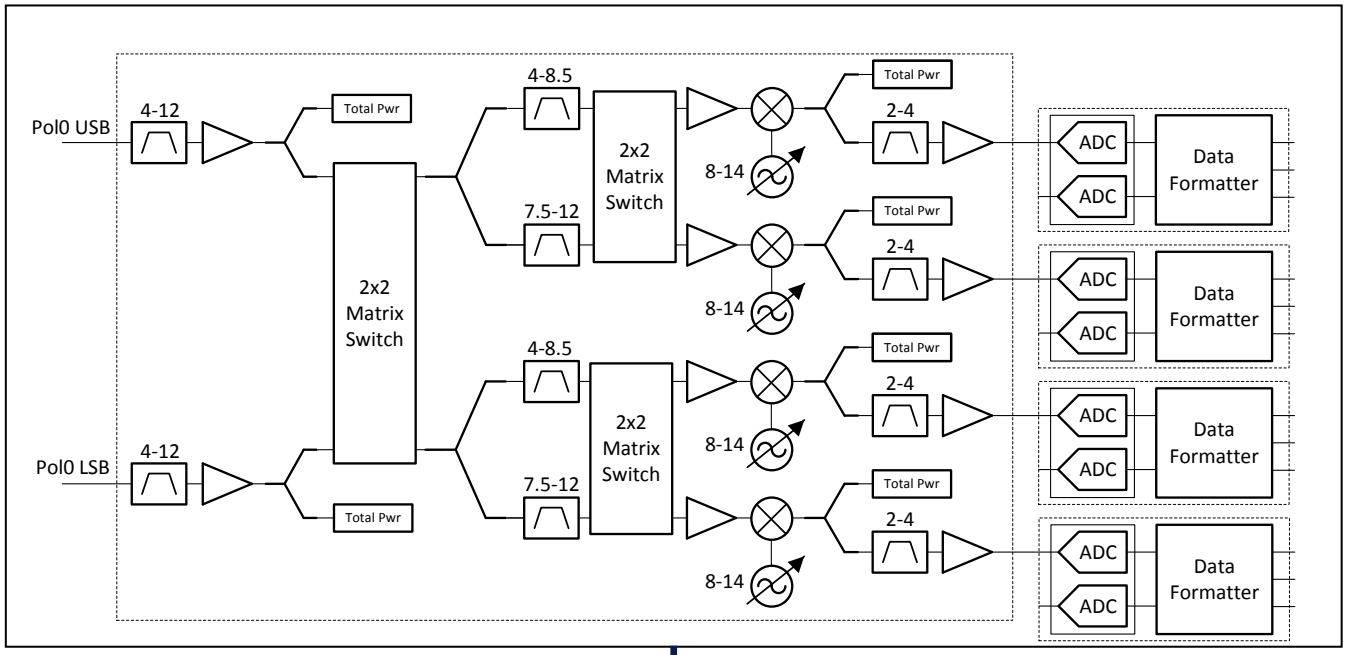
- Context of the study
- Digitizer upgrade
  - ASIC solution
  - COTS solution
- Correlator upgrade
- Future plans

- **Electronics group from LAB:**
  - delivered ~ 300 DiGitizer modules
  - delivered ~ 600 Tunable Filter Bank cards
  - involved in the DG, TFB and DG clock module corrective maintenance services with ESO
  - involved in a R&D study in the frame of the ESO 2013 Call for Proposal

- **"Very High Speed Digitization and Processing for Enhanced ALMA bandwidths"**
  - two year project including conceptual study, DSP modeling, ASIC design, COTS survey and evaluation
  - simplify current back-end
  - prepare back-end for future bandwidth broadening
  - compatibility with the baseline correlator

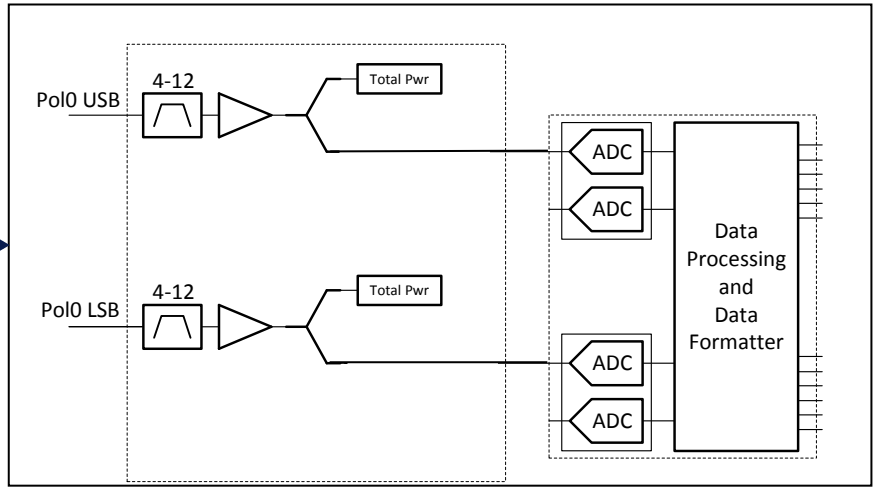



- **Front-End**
  - 2 polar x 8 GHz (4 – 12 GHz)
- **Back-End**
  - 2 polar x 4 x 2 GHz basebands (2 – 4 GHz) x 3 bits
- **Optic fiber**
  - 120 Gb/s (96 Gb/s + 8b/10b)
- **Correlator**
  - 2 GHz basebands → 32 x 62.5 MHz subbands, 125 MHz clock

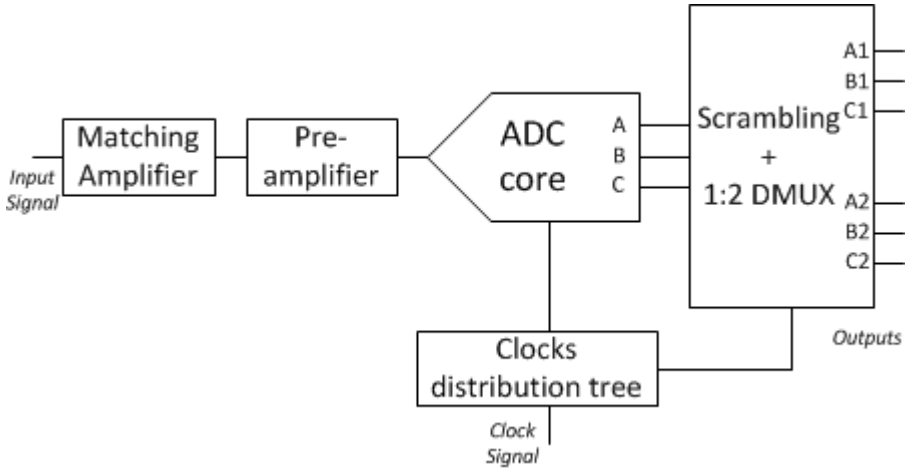



- Wider bandwidth
- Less dissipation
- Better reliability
- Faster calibration
- Higher versatility

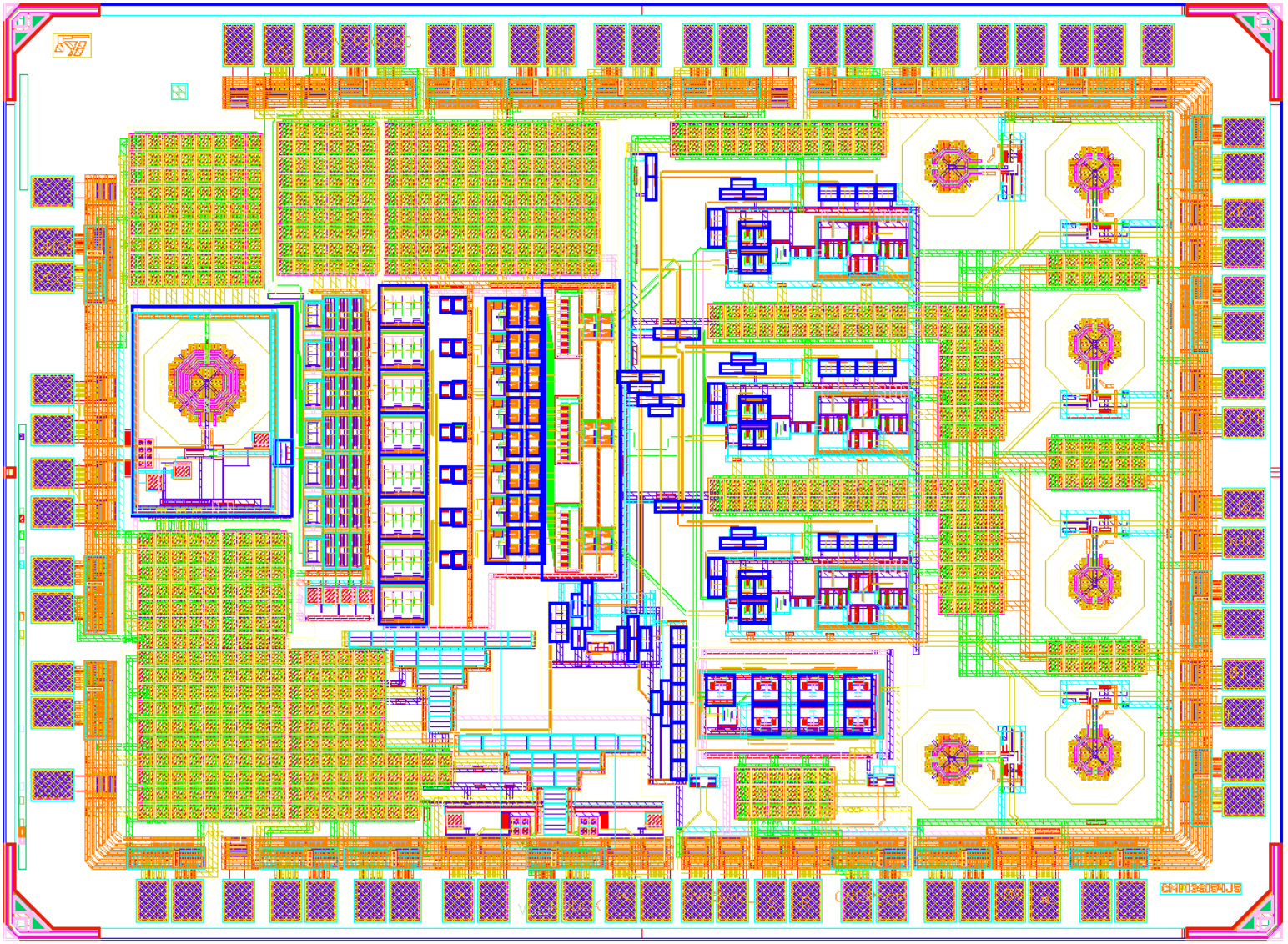
@4GSps → @24 GSps



- **BiCMOS9mw (130nm) from STmicroelectronics**
- **3 bit flash ADC core**
  - Analog front-end
  - Comparator stage
  - 2's complement encoding
- **Scrambling**
- **Demultiplexing**



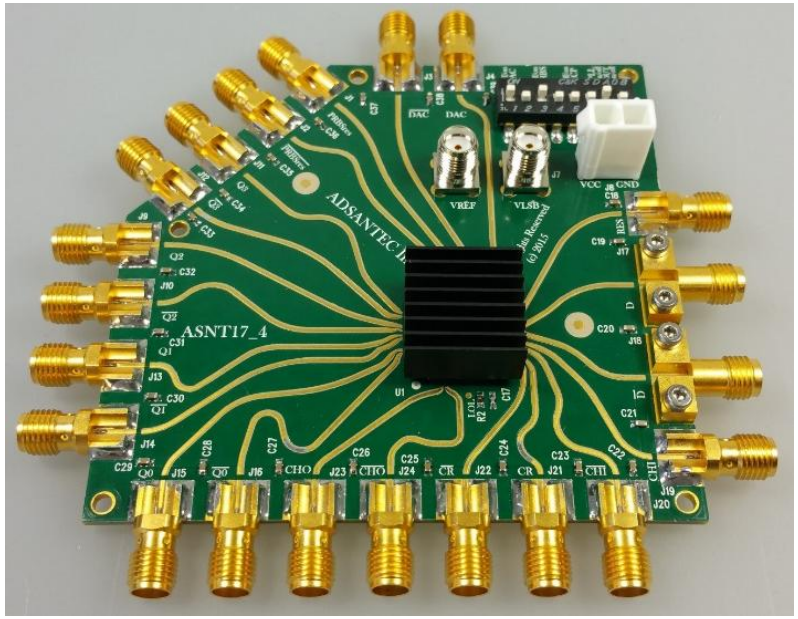

| | |
|---|---|
| **Analog Bandwidth at -3dB** | 18 GHz |
| **Sampling frequency** | 16 GHz |
| **Linearity (ENOB)** | > 2.5 |
| **Power** | 2.3 W |
| **Output frequency** | 8 Gbps |
| **Die size** | 5.5 $mm^2$ |

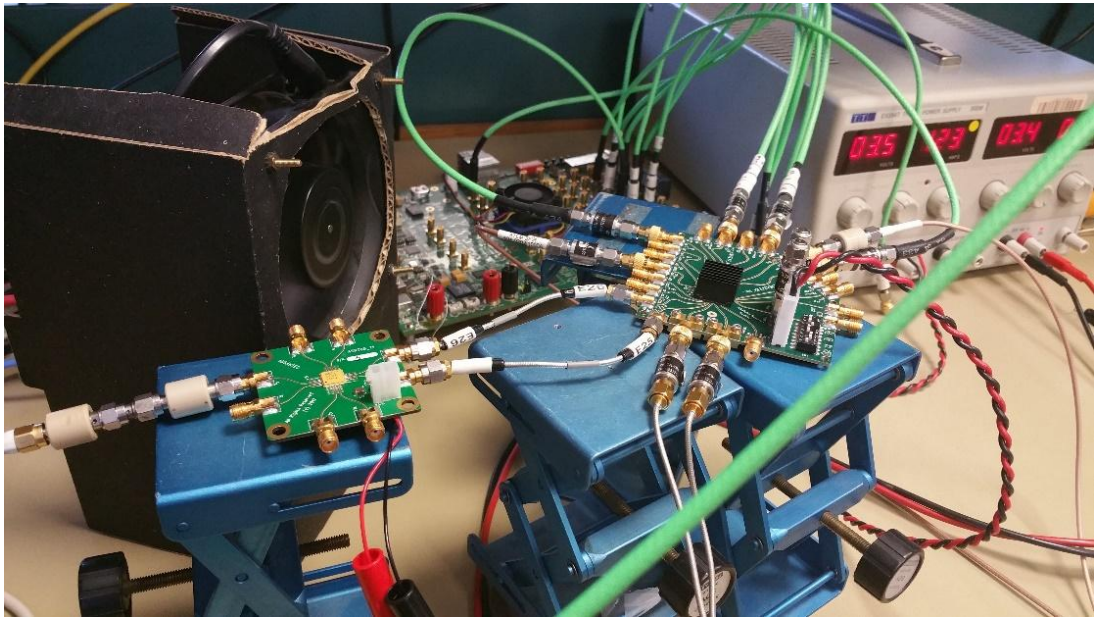


- **Survey, evaluation, prototyping**
- **ADC (IP and standalone devices)**

| GSps | GHz | Bits | Manufact. | W | Remarks |
|---|---|---|---|---|---|
| **15** | 20 | 4 | Adsantec | 4.3 | Flash, 4 high speed outputs. Data mixed with an internal PRBS. 1600€ |
| **26** | 20 | 3 | Hittite | 4.2 | Flash, each bit scrambled with external PRBS, internal 1:2 DMUX. 1100 € for 300 units |
| **25** | 24 | 4 | Alphacore | 0.42 | Flash, Data mixed with an internal PRBS generator. 2000-2500€. Q4 2016. |
| **32** | 30 | 6 | Micram | 10 | 2 x interleaved ADC cores at 16 GSps with internal 1:2 DMUX, each output scrambled with internal PRBS. 100k€ (prototyping phase) and 3k€ each (production). |
| **42-68** | 20 | 8 | Jariet | <1 | IP macro. Multi-interleaved channels. |

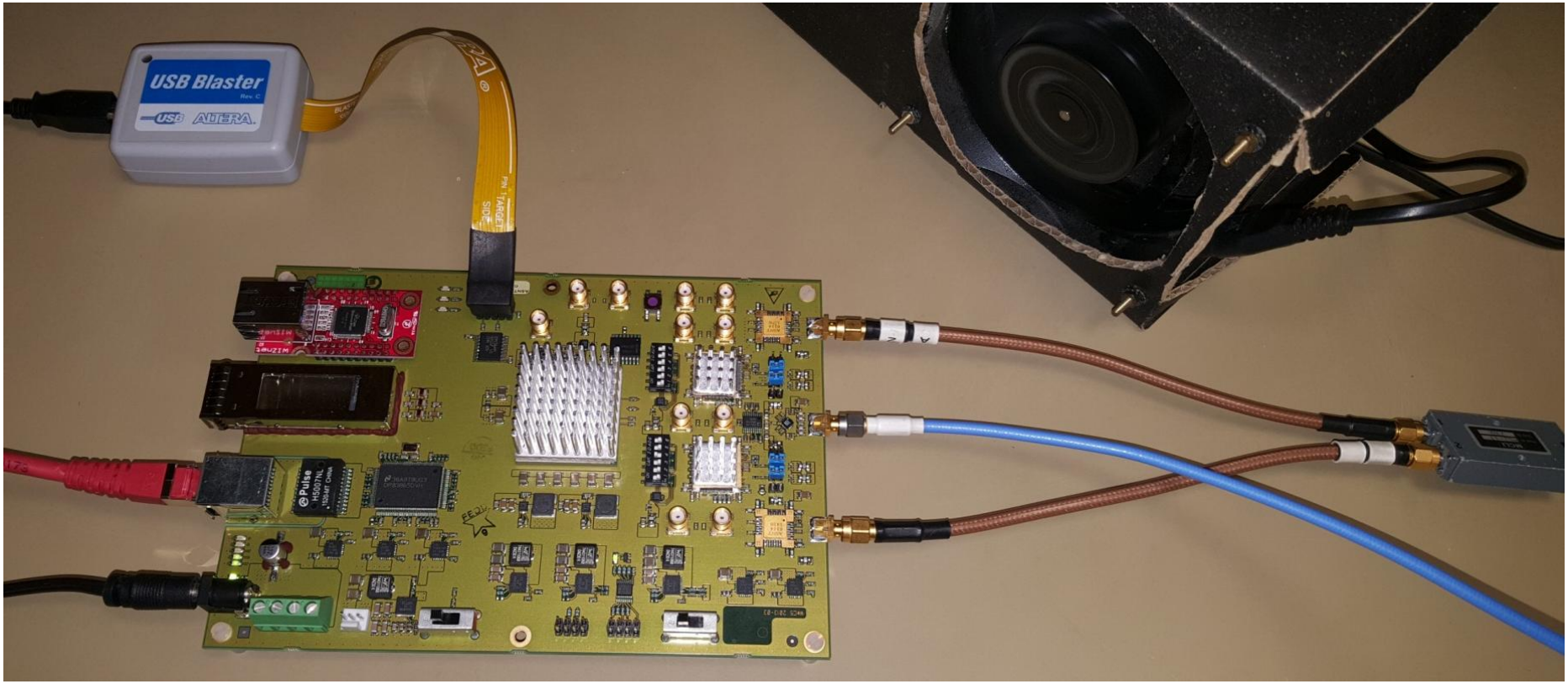
# 4-bit ADC from Adsantec



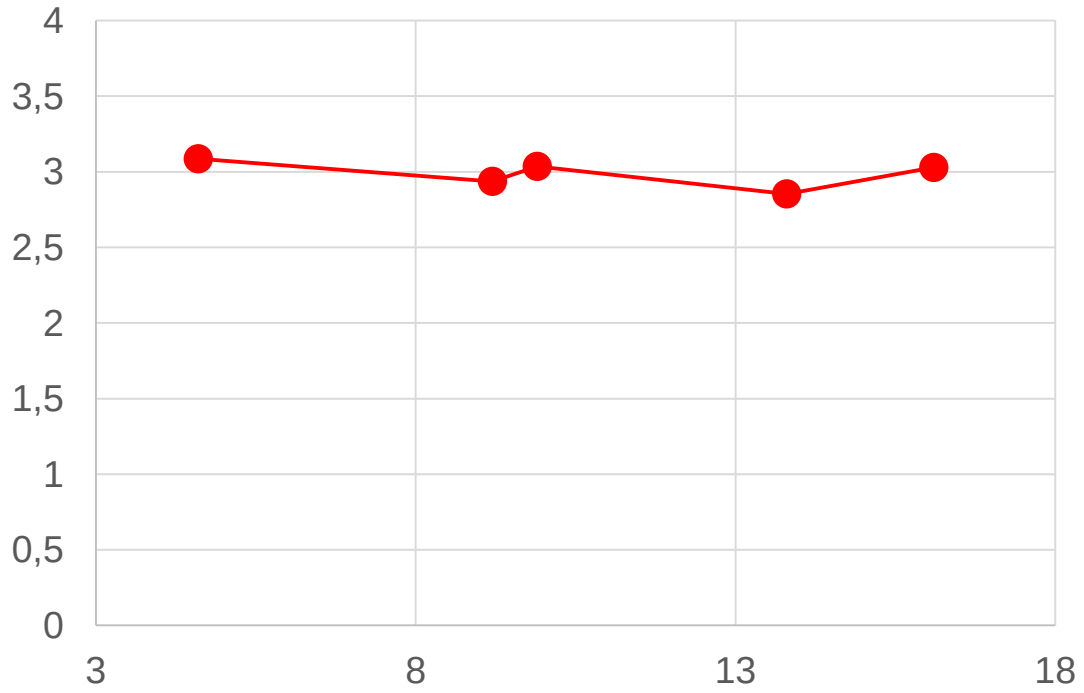



| Fin (GHz) | SFDR | SINAD | ENOB at 10 GSps |
|---|---|---|---|
| 7.9 | 28.8 dBc | 21.2 dB | 3.23 |
| 13.8 | 25.5 dBc | 19.6 dB | 2.97 |

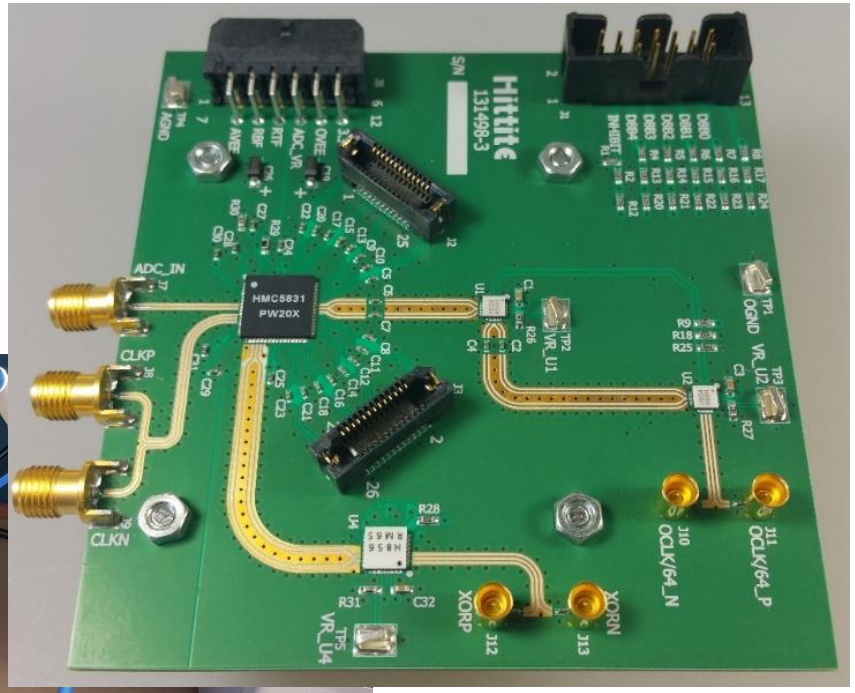
- **2 interleaved ADC from Adsantec:**
  - 2-channel interleaved ADC for 10 GSps sampling
  - Bandwidth > 10GHz
  - Under test

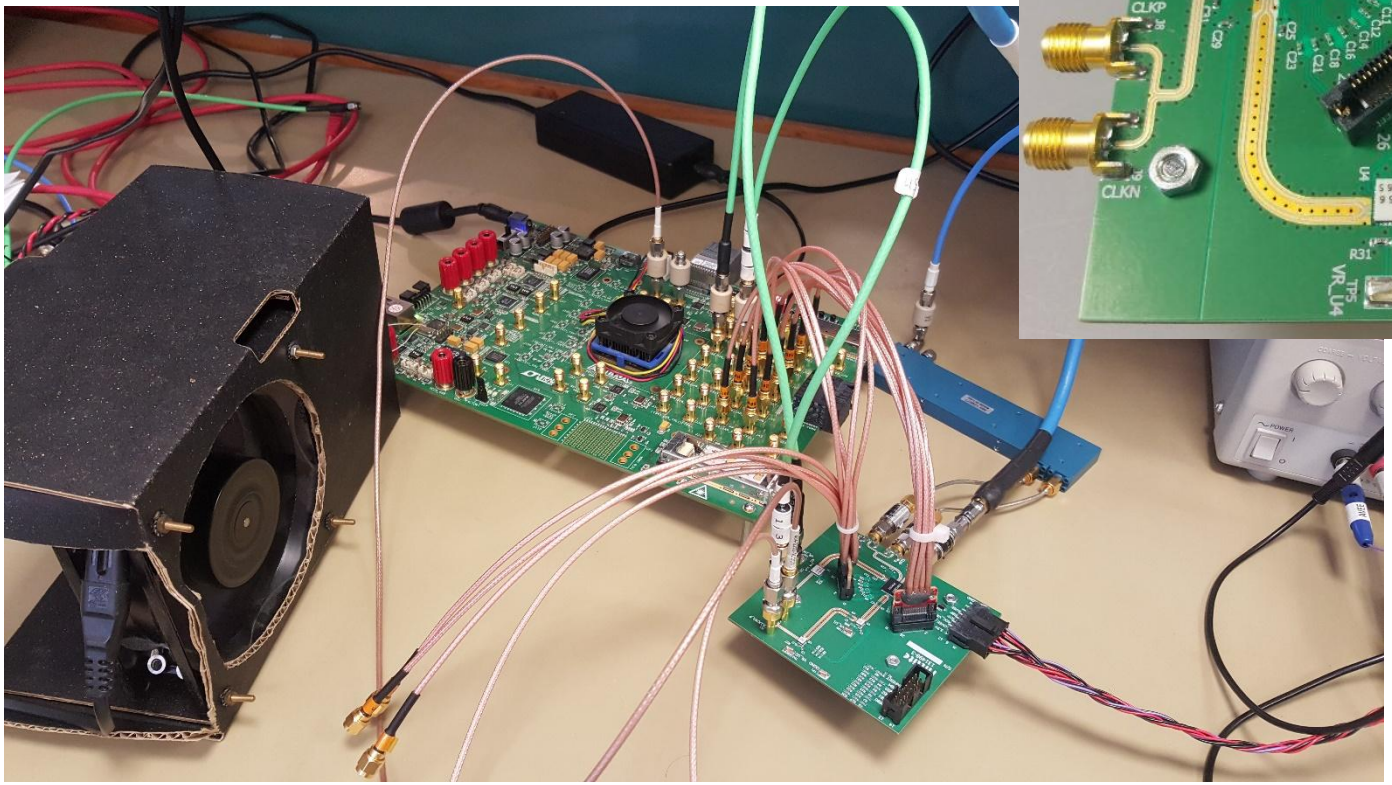


- **2 interleaved ADC from Adsantec:**
  - ENOB ≈ 3 at 10GSps
  - Offset and gain error compensation, clock skew error minimization for each input signal frequency



- **3-bit ADC from Hittite (ADI)**

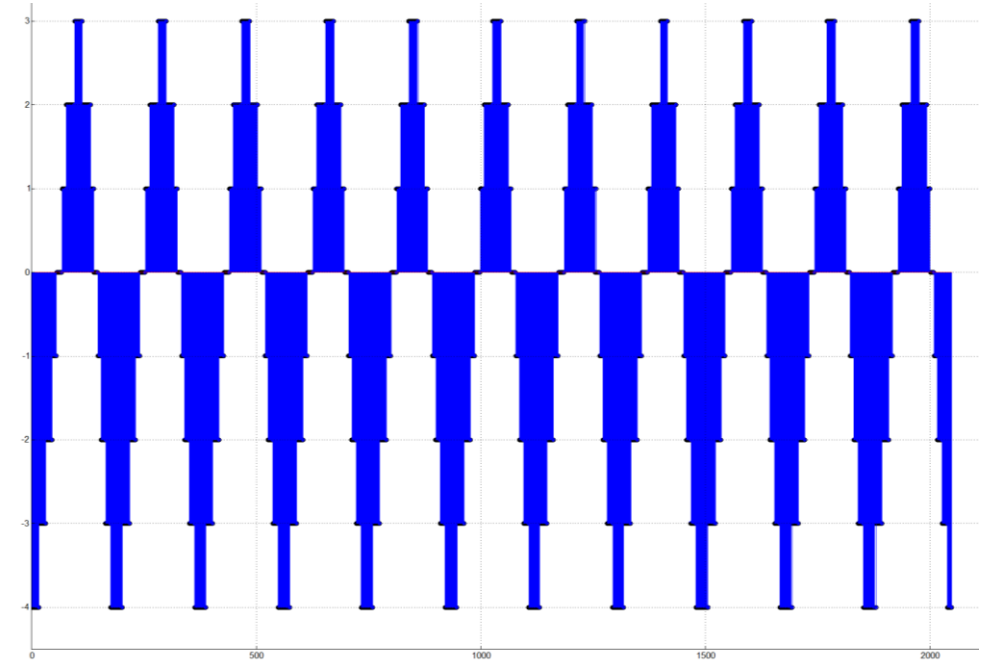


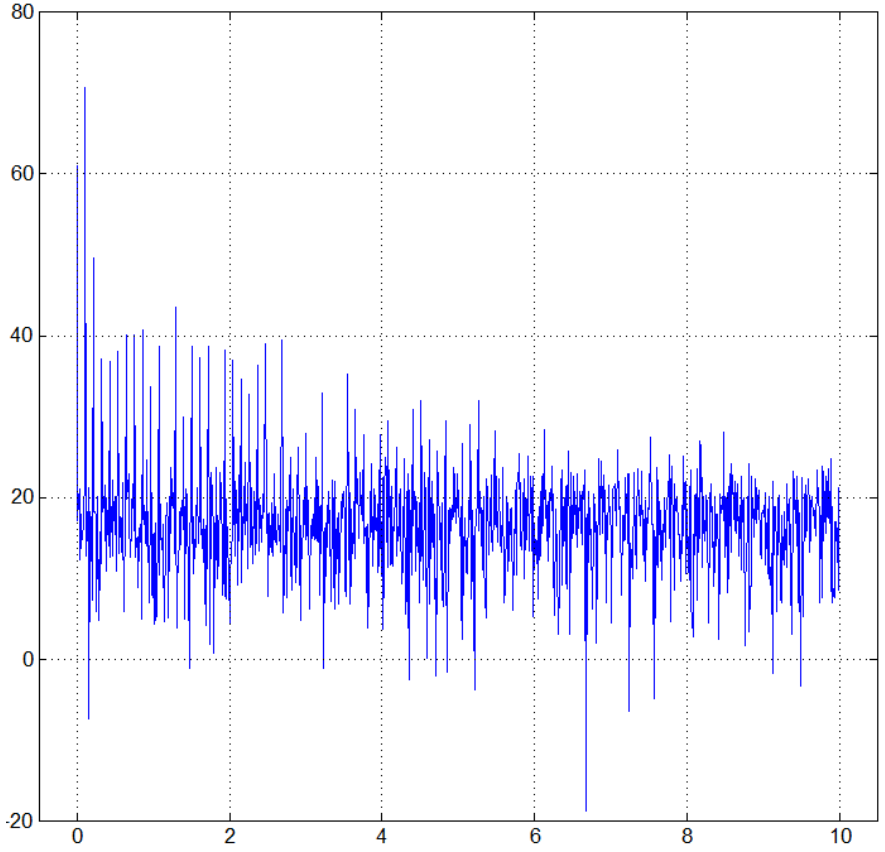
- **3-bit ADC from Hittite (ADI)**

2048 samples (no glitch)

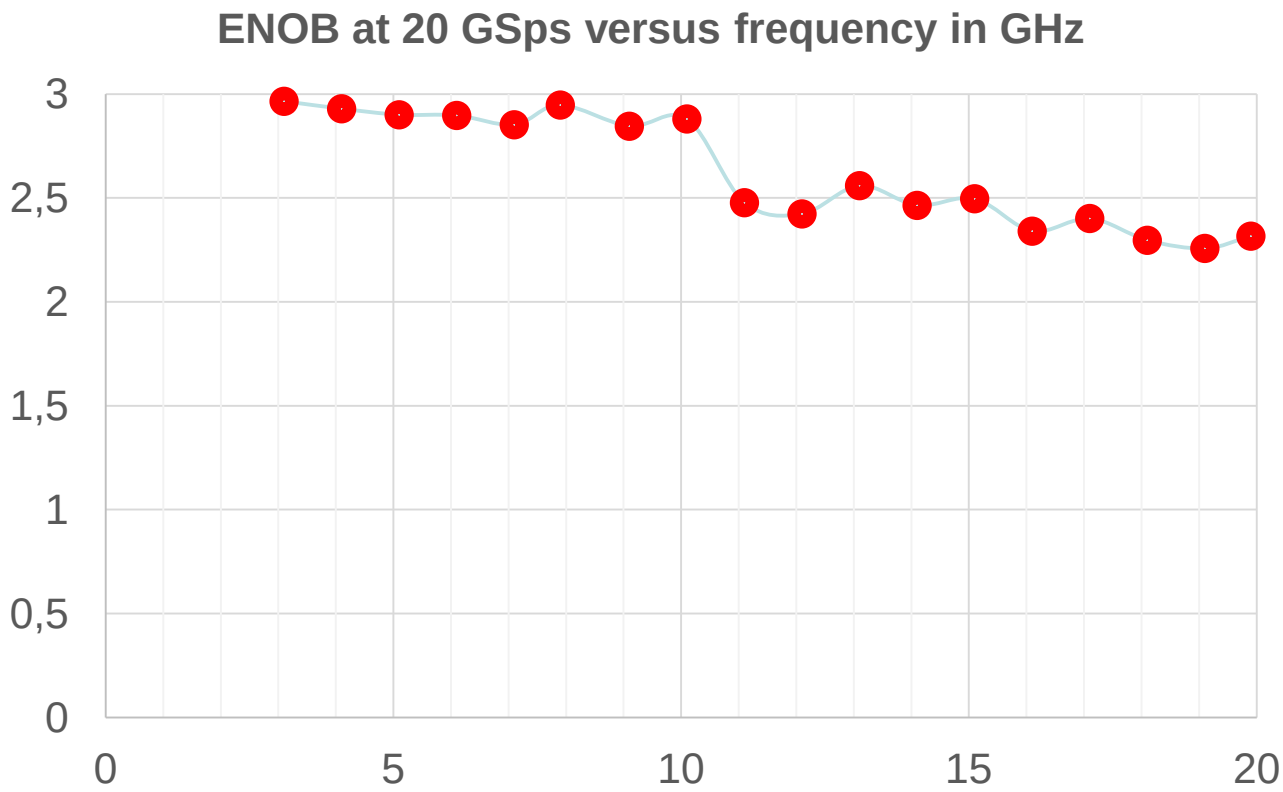
19.9 GHz at 20 GSps



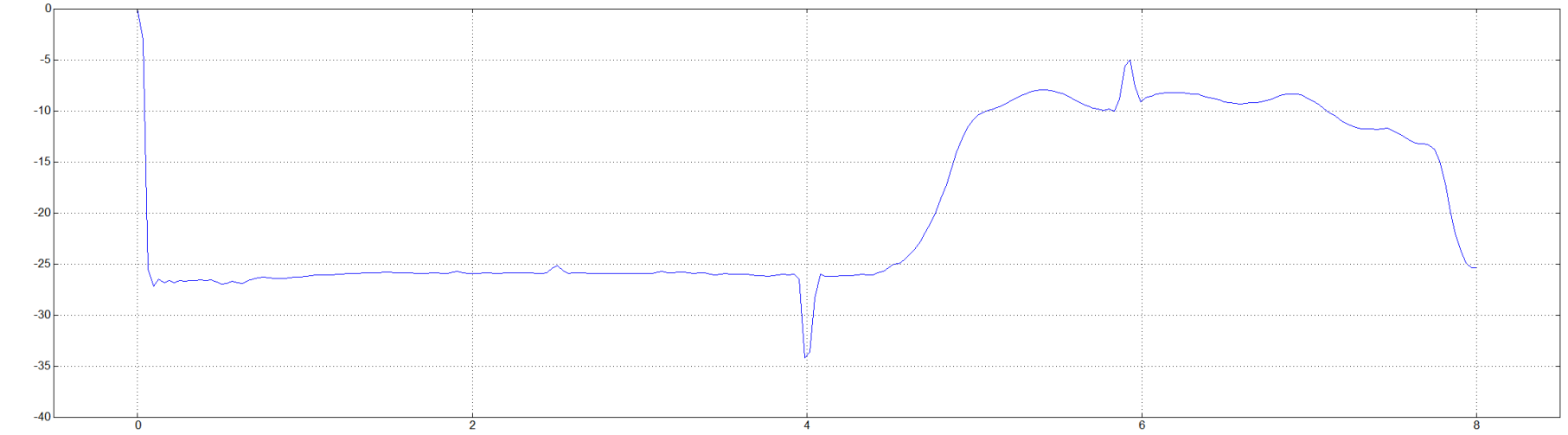
2048 samples FFT

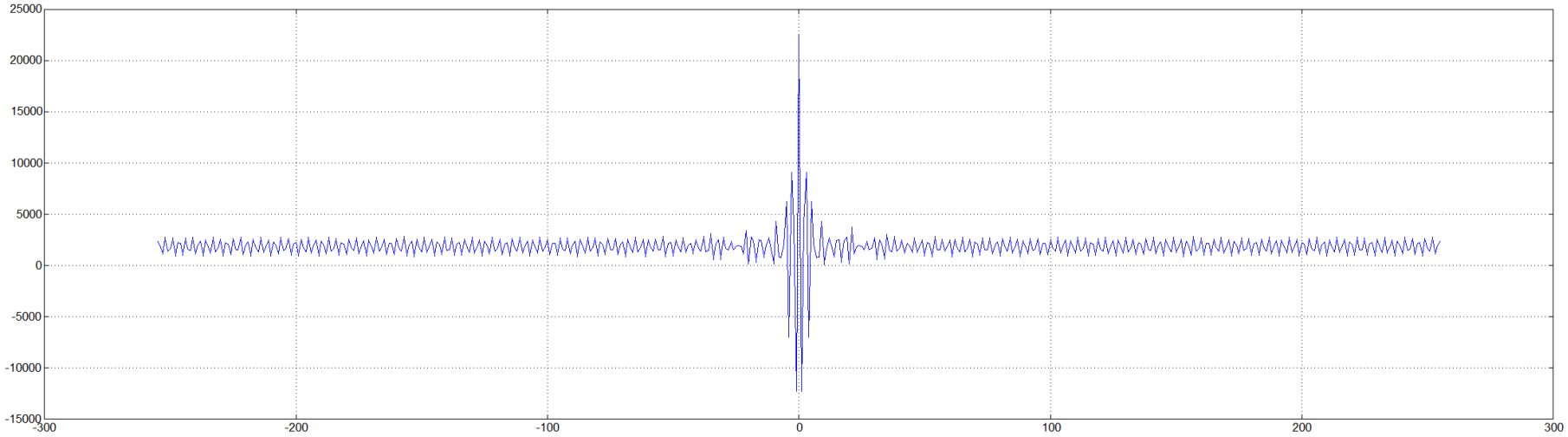


# 3-bit ADC from Hittite (ADI)



# 3-bit ADC from Hittite (ADI)



- **Spectral Resolution and Bandwidth Upgrade of the ALMA Correlator (R. Lacasse)**

- **Increase the 64-ant ALMA correlator bandwidth by a factor of 2**
- **Increase spectral resolution by a factor of 8**

- **Minimum cost**
- **Minimum effort**
- **Minimum disruption**
- **Minimum risk**
- **Fast time to operation**

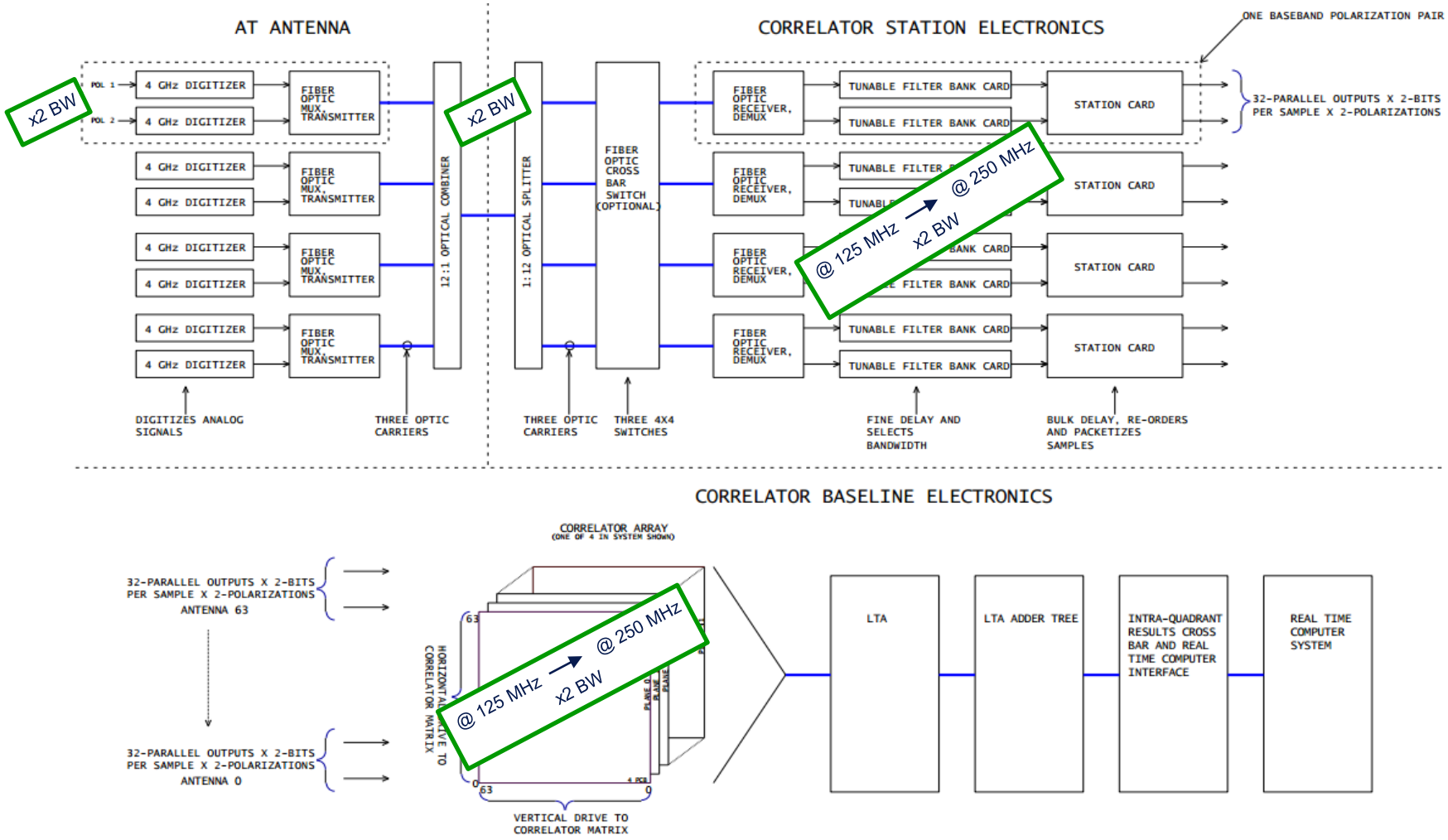
- **Interim correlator pending a software correlator?**

- **Same architecture (racks, bins, power, wire links etc.)**
- **Double the clock frequency for the DSP**

- **New DiGitizer module**
- **New optical transmission scheme**
  - Need to update DWDM
  - 40 channels sufficient for doubled BW and 4-bit transmission
- **New Tunable Filter Bank**
- **New correlator chip**
  - Lags x 32 → resolution x 8, correlator board / 4
  - Quotation on NA and UE sides
- **New Final Adder board**
- **New Correlator Data Processor interface**

- **Collaboration between NRAO and Bordeaux**
- **Development study documentation shared**
- **Webex session on April 27th 2016**
- **NRAO and Bordeaux possible contributions**
- **TFB options**

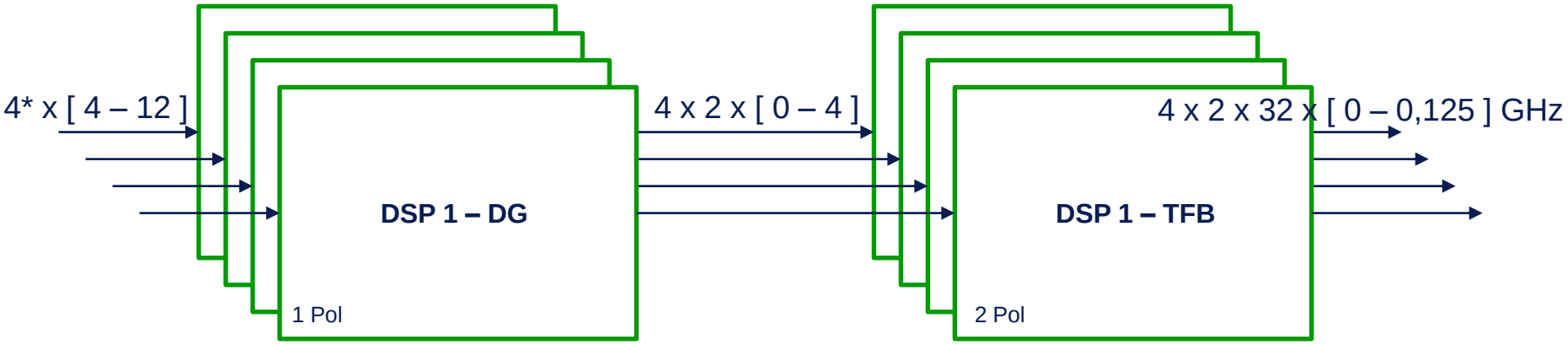
# Doubling the correlator bandwidth (BW)



# DSP 1

TFB BW = 4 GHz

- 2 stages for sub-band extraction

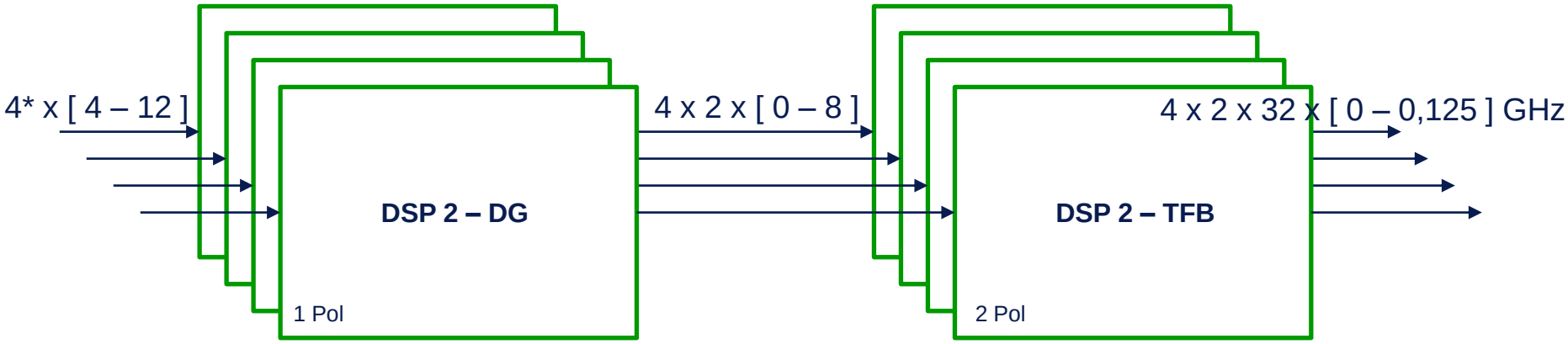



* *4 = Pol0 LSB – Pol0 USB – Pol1 LSB – Pol1 USB*

# DSP 2

TFB BW = 8 GHz

- 1 stage for sub-band extraction




* *4 = Pol0 LSB – Pol0 USB – Pol1 LSB – Pol1 USB*

# Suppressing analog IF stages & doubling correlator BW

| | Present configuration | New configuration |
|---|---|---|
| Digitizer | • 2 POL x 4 x [ 2 GHz ]<br>• 4 GSps<br>• 3 bits | • 2 POL x **2** x [ **12** GHz ]<br>• **24 GSps**<br>• 3 or **4 bits** |
| Optical fiber | • 2 POL x 4 x [ 2 GHz ]<br>• 10 Gbps<br>• 12 WL | • 2 POL x 4 x [ **4** GHz ] or [ **8** GHz ]<br>• 10 Gbps<br>• **24 or 48** WL (3b) or **32 or 64** WL (4b) |
| Correlator | • 2 POL x 4 x [ 32 x 62,5 MHz ]<br>• 125 MSps<br>• 2 bits | • 2 POL x 4 x [ 32 x **125** MHz ]<br>• **250 MSps**<br>• 2 bits |

- **2013 dev. study focused on digitizer at component level**
- **ASIC design, COTS survey and evaluation**
- **Final review and reports, end of 2016**

- **2016 proposal highly connected to NRAO correlator upgrade study**
- **From digitizer to TFB**
- **HW prototyping for on site validation**