RTC Workshop
Dec 5th, 2012

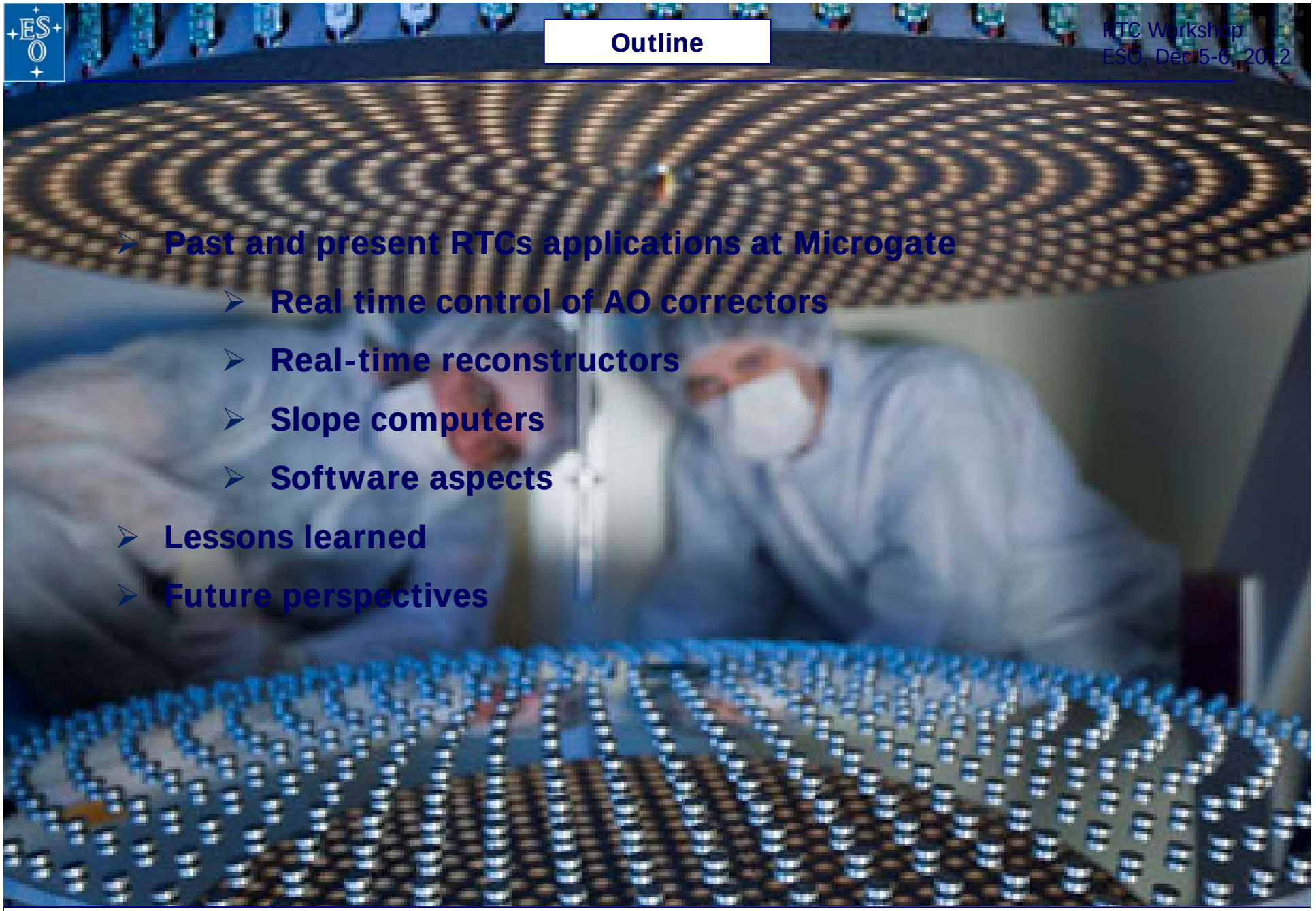
Present Microgate RTCs and perspectives

R. Biasi

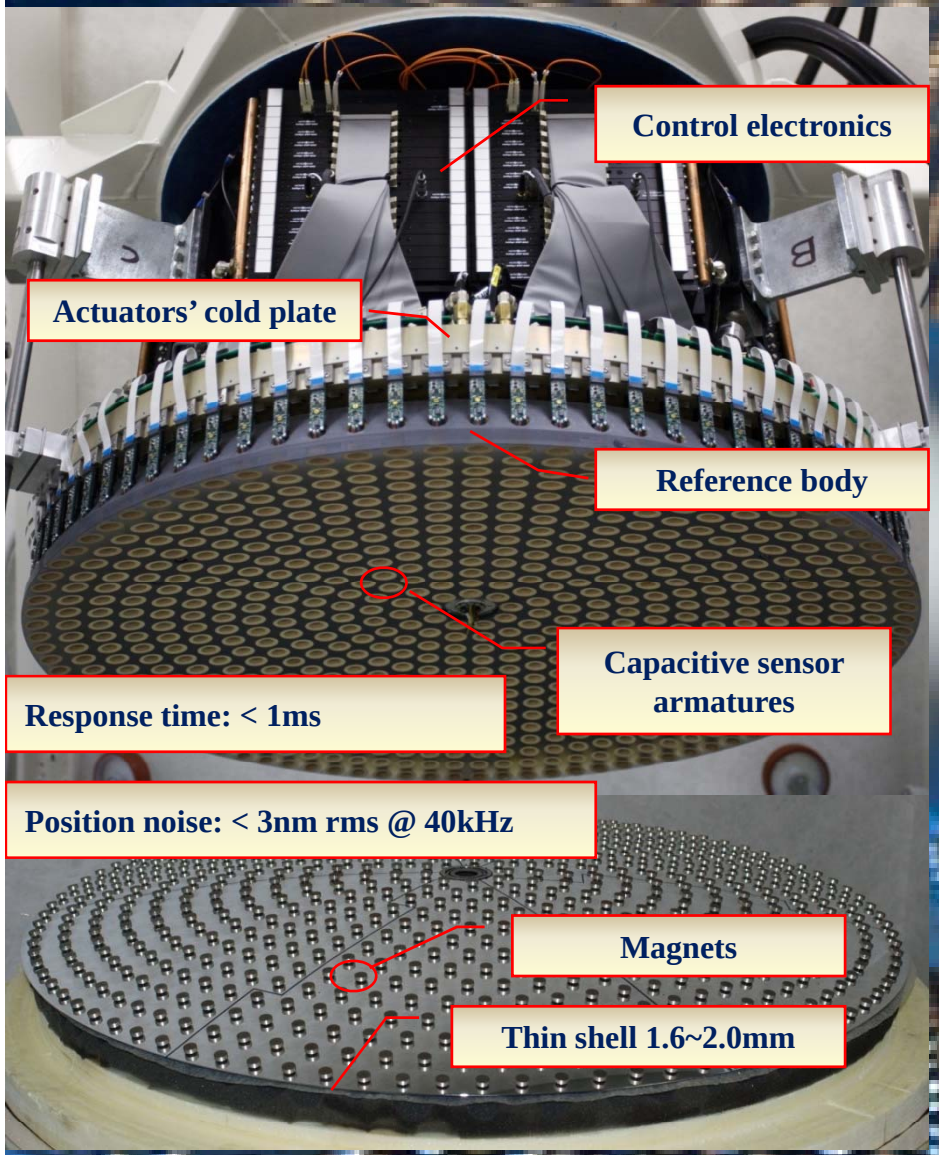
Microgate

Outline

- Past and present RTCs applications at Microgate
  - Real time control of AO correctors
  - Real-time reconstructors
  - Slope computers
  - Software aspects
- Lessons learned
- Future perspectives

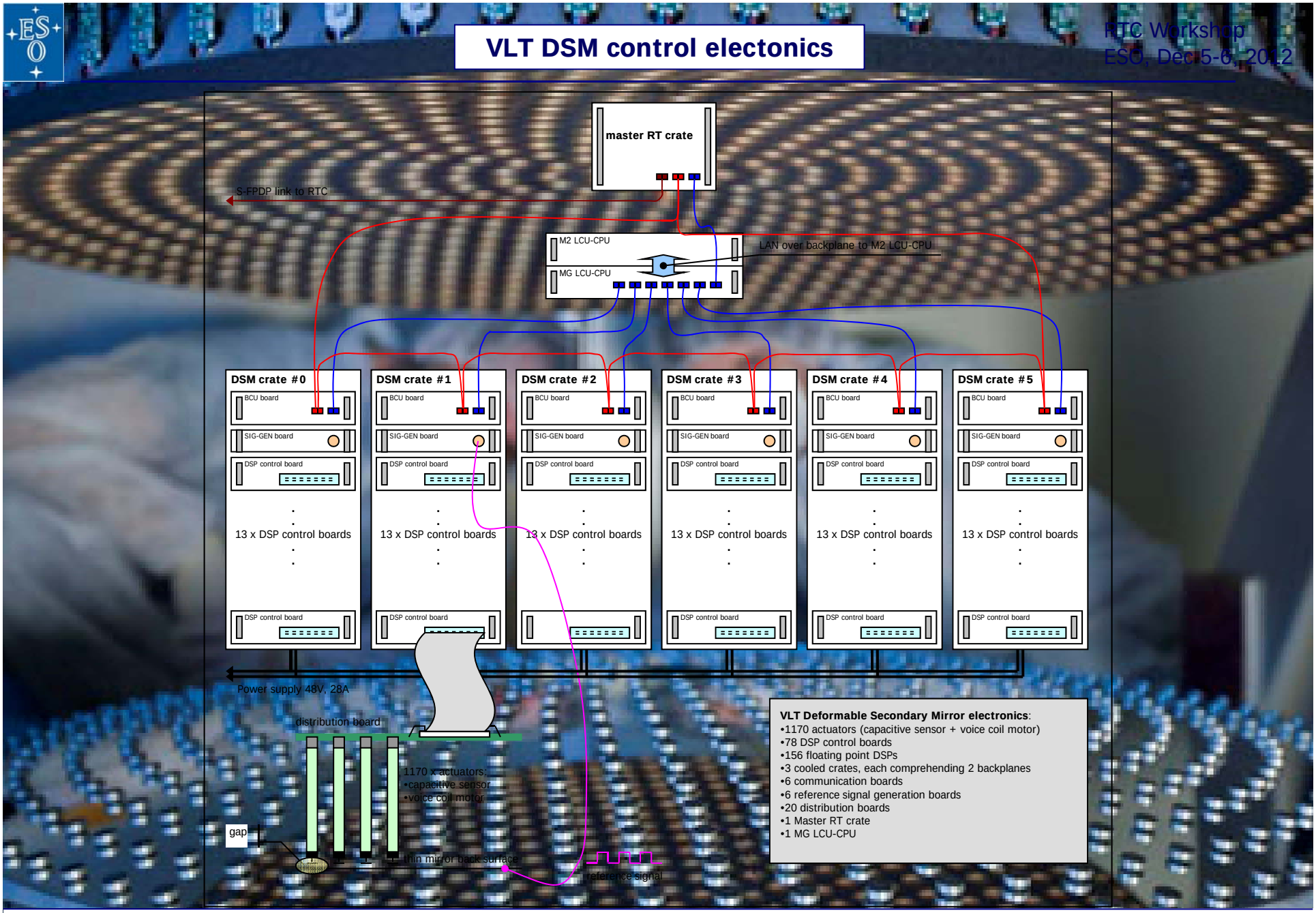


How it started / motivations



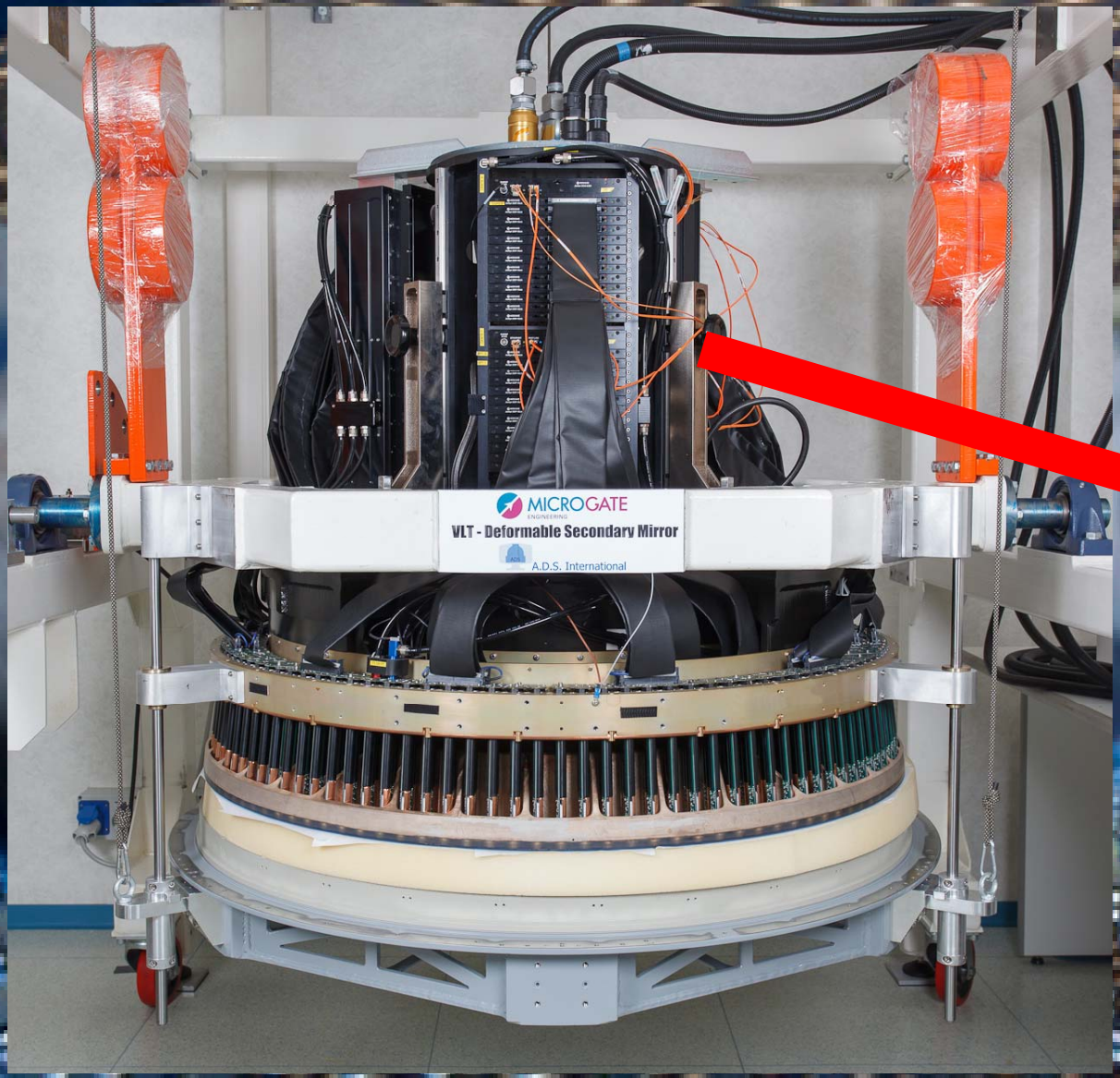
- Initially designed to control the **LBT Adaptive Secondary** units
- Motivations for a ***full custom design***:
  - co-existence of digital & analog electronics requirements (capacitive sensors, voice coil motors drivers)
  - dimensional constraints
  - cooling constraints
  - computational performance + diagnostics
  - need for a 'true parallel' machine
- **2003 design...**

VLT DSM control electonics



MICROGATE ENGINEERING

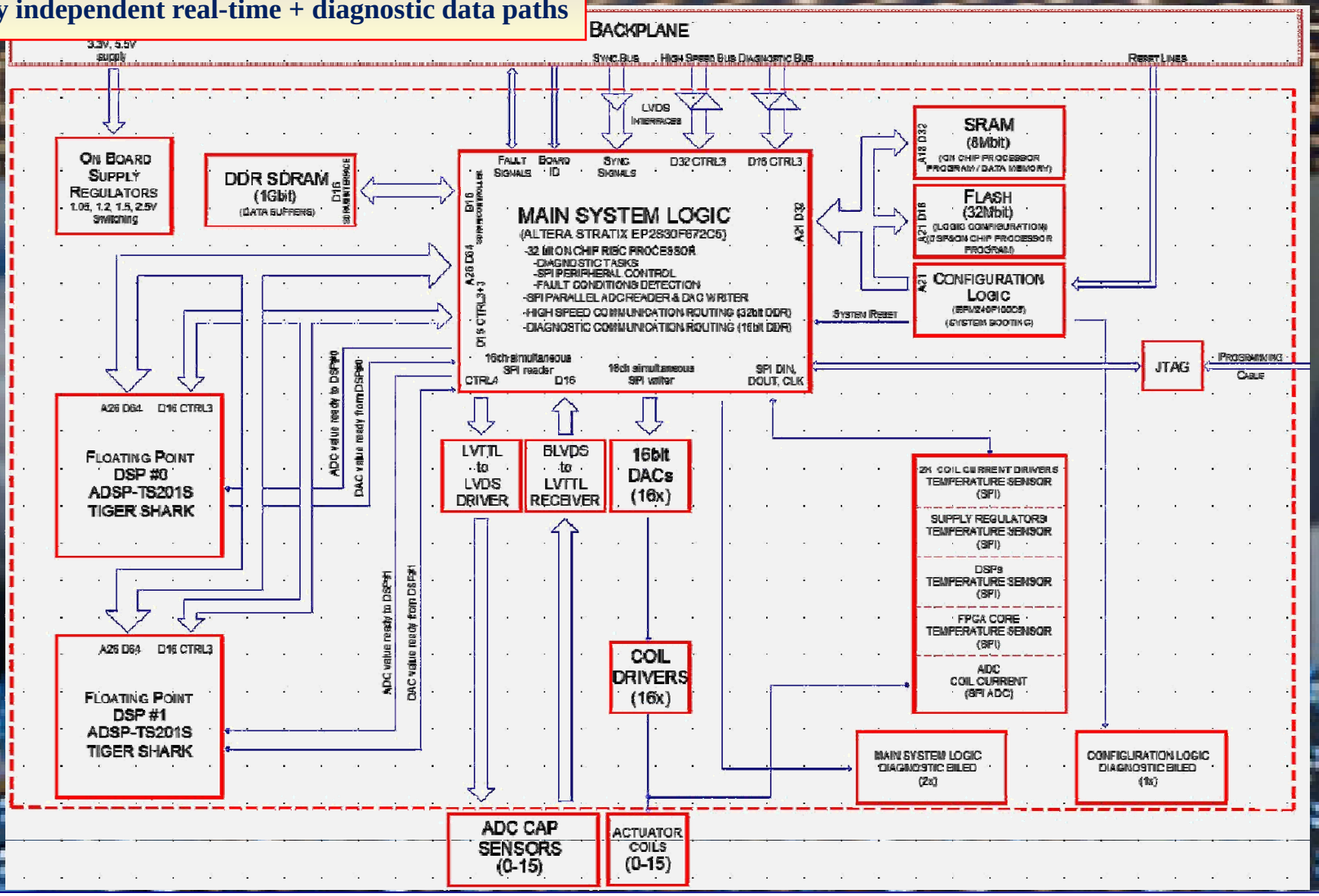
VLT DSM



MICROGATE
ENGINEERING

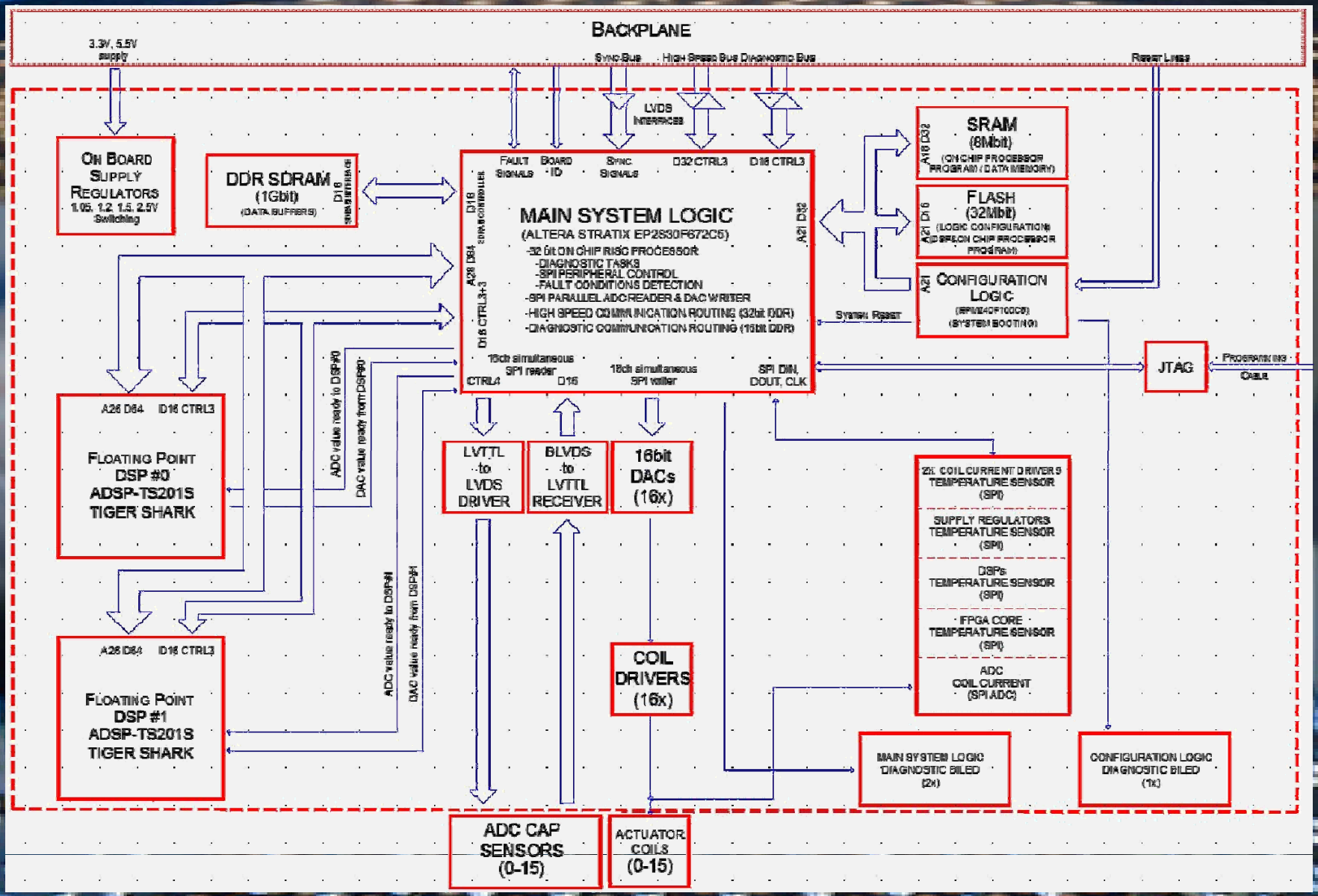
Main components: BCU

Fully independent real-time + diagnostic data paths



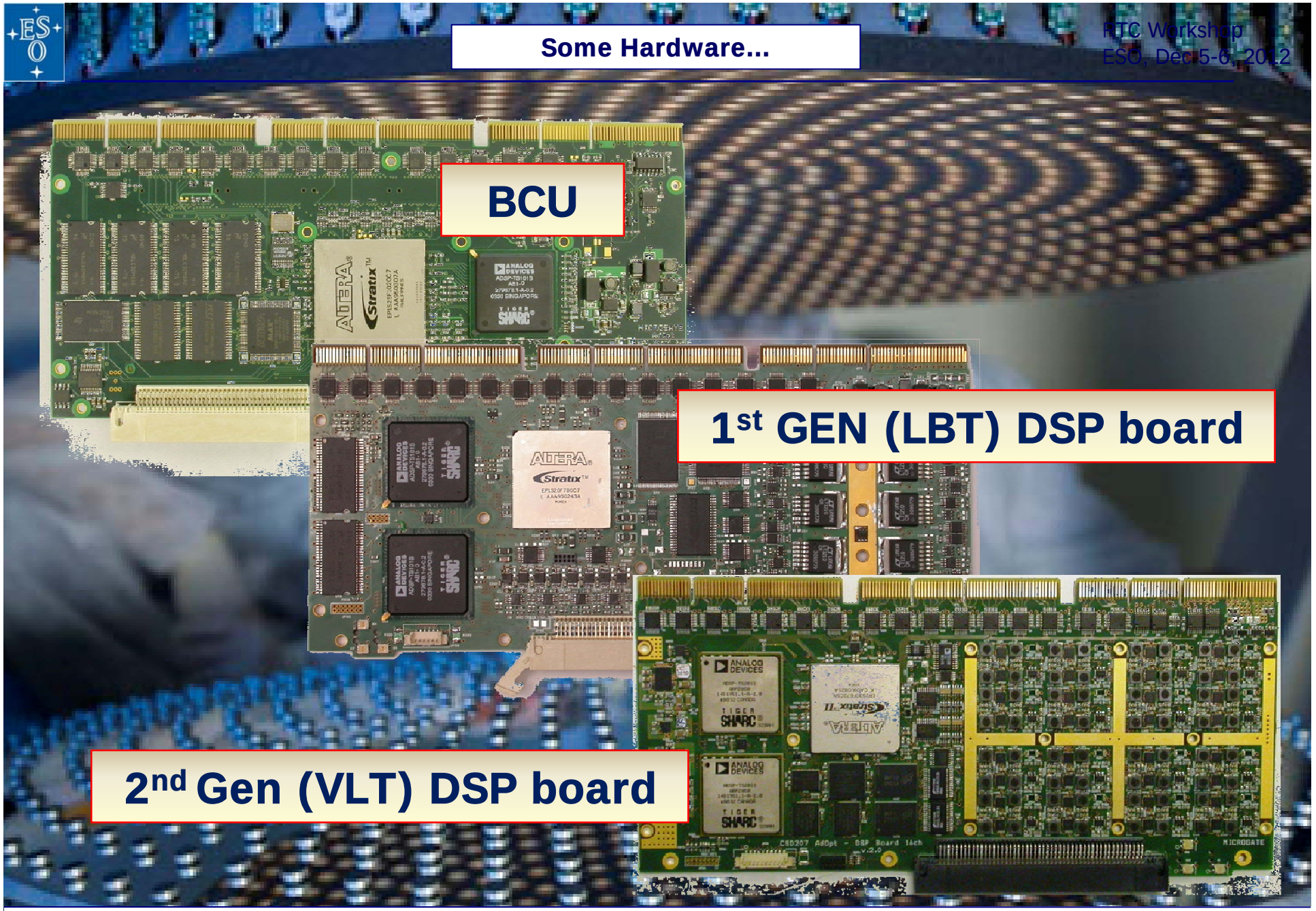
MICROGATE ENGINEERING

Main components: DSP control board



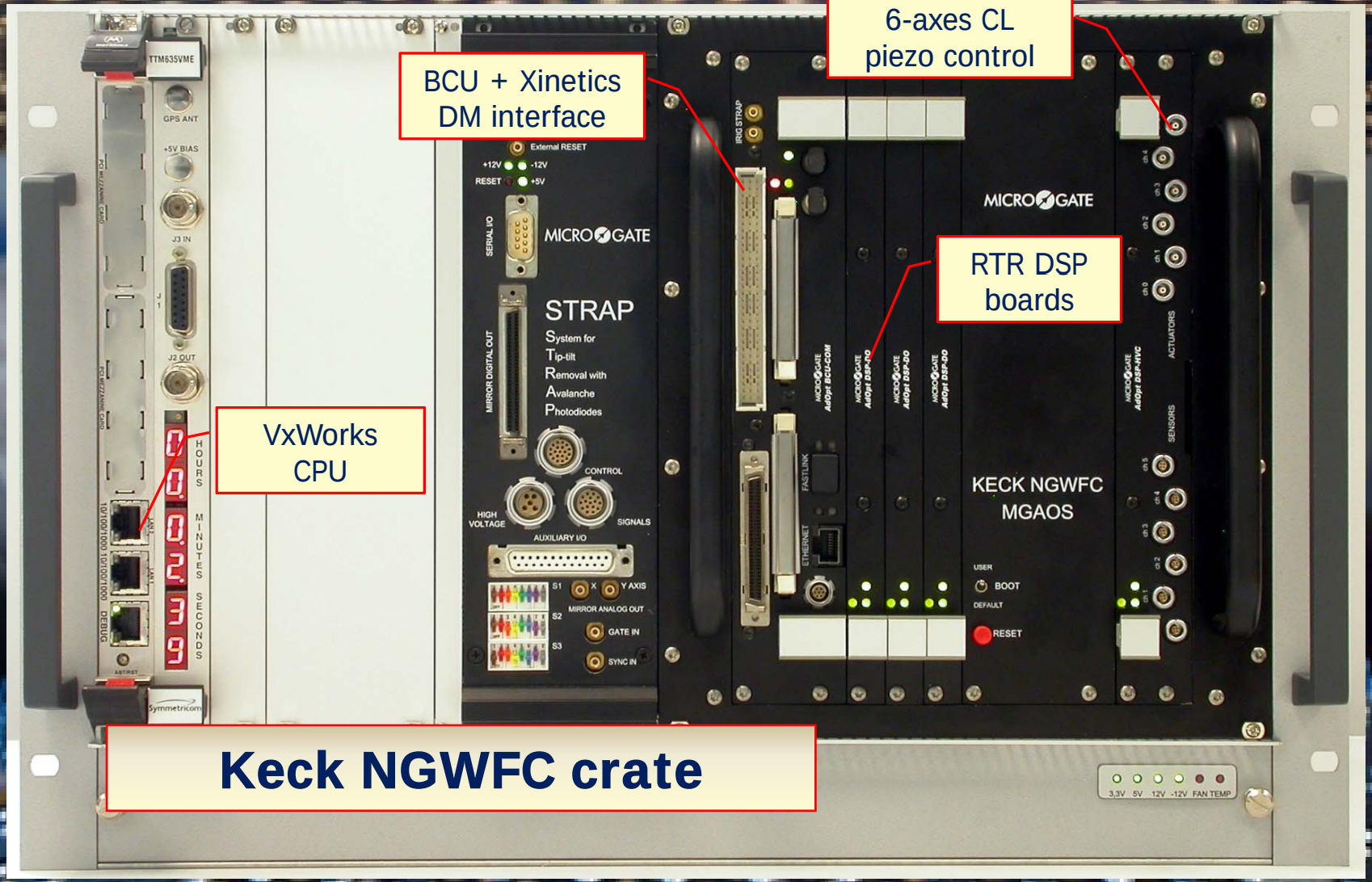
MICROGATE ENGINEERING

Some Hardware...



MICROGATE ENGINEERING

Some Hardware...



Modules Performances

BCU

- 500 MMAC/s floating point sustained
- FPGA for seamless interfacing to various protocols and sensors (S-FPDP, SciMeasure, Andor, Xinetics, ..)
- FPGA performs also hardware acceleration + housekeeping (NIOS)
- Gigabit Ethernet interface (copper or fiber) for diagnostic
- 4x fiber modules up to 2.5 Gbit/s each (FiberChannel, S-FPDP) for real time communication

DSP board

- 1 GMAC/s floating point sustained (LBT: 84 boards, 84 GMAC/s) – AD DSP TS101
- FPGA for data routing (DMA from/to DSPs, bulk memory access, NIOS embedded controller)

Gen 2 DSP board (VLT DSM)

- 2 GMAC/s floating point sustained (VLT: 78 boards, 156 GMAC/s) – AD DSP TS201
- FPGA for data routing (DMA from/to DSPs, bulk memory access, NIOS embedded controller)
- 16 controlled channels, capacitive sensors + voice coil motor

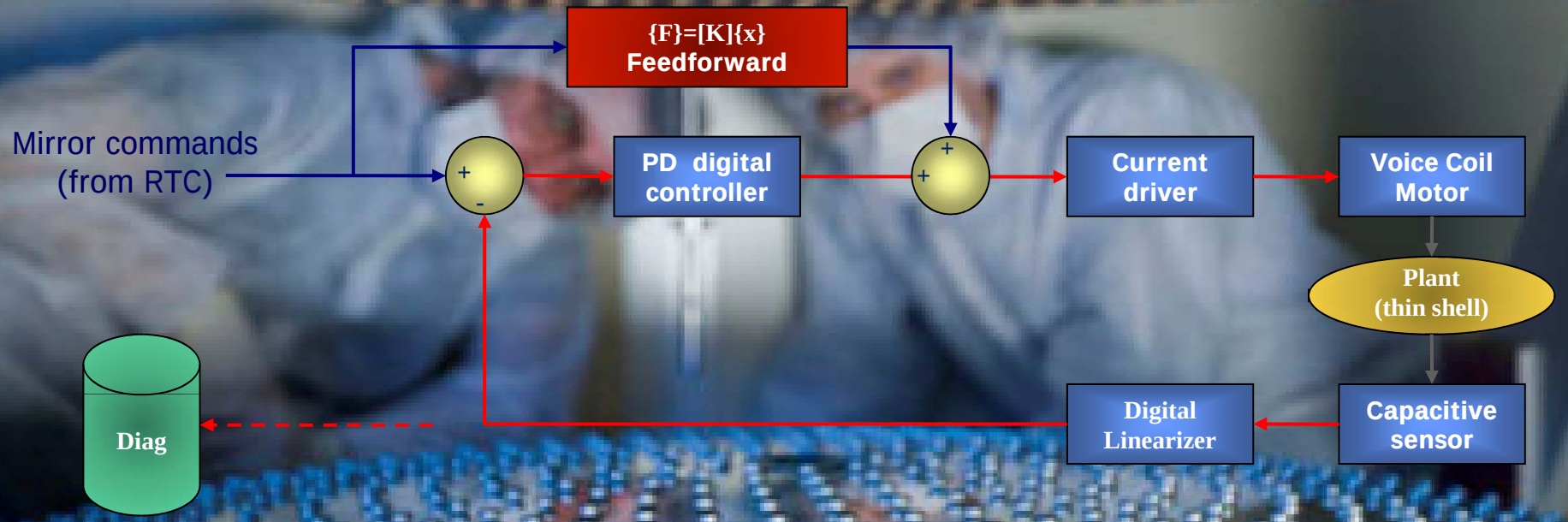
Backplane

- Up to 15 DSP boards + 1 BCU board per backplane
- Diagnostic bus: 2Gbit/s – Real-time bus: 4Gbit/s (BLVDS)

Main Applications

Contactless Deformable Mirror control

- Co-located control loop
- Global Feedforward
- Shell safety checks (modal forces, stroke, ...)



WFS loop frequency (~ 1kHz)

co-located loop frequency (~ 70kHz)

Co-located control typical computational time:
2.5µs (LBT: 4ch/DSP, VLT: 8ch/DSP)

Main Applications

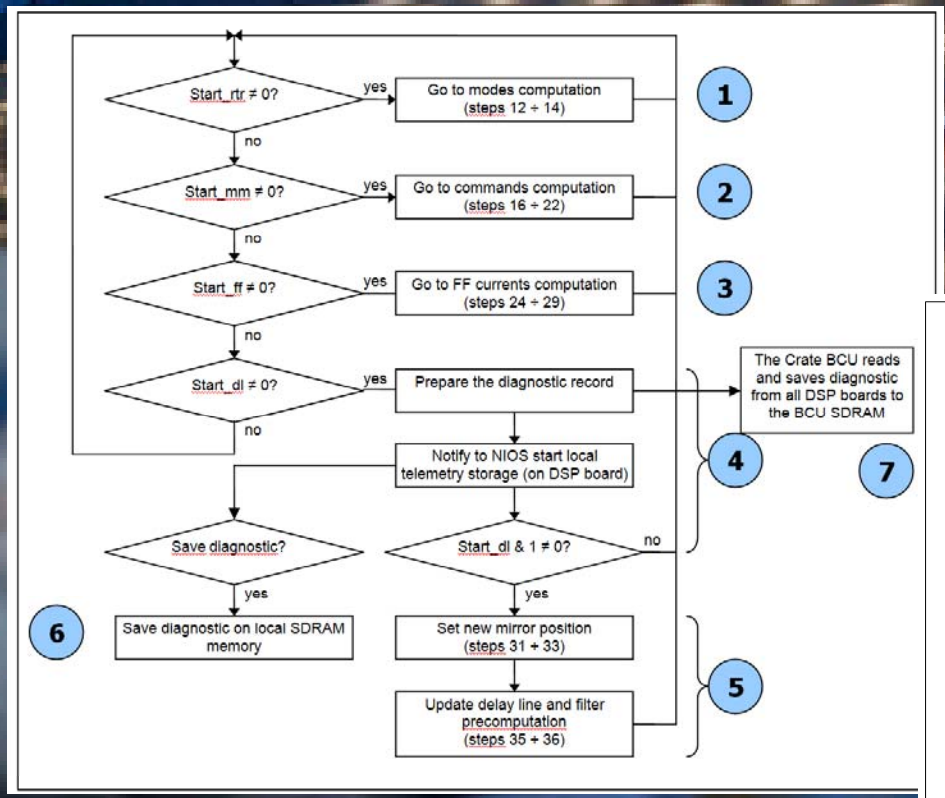
Real time reconstructor

- LBT + Magellan: RTR implemented in the same boards performing the mirror control
- Keck: dedicated boards for RTR only
- MMT Laser Guide Star Real Time Reconstructor

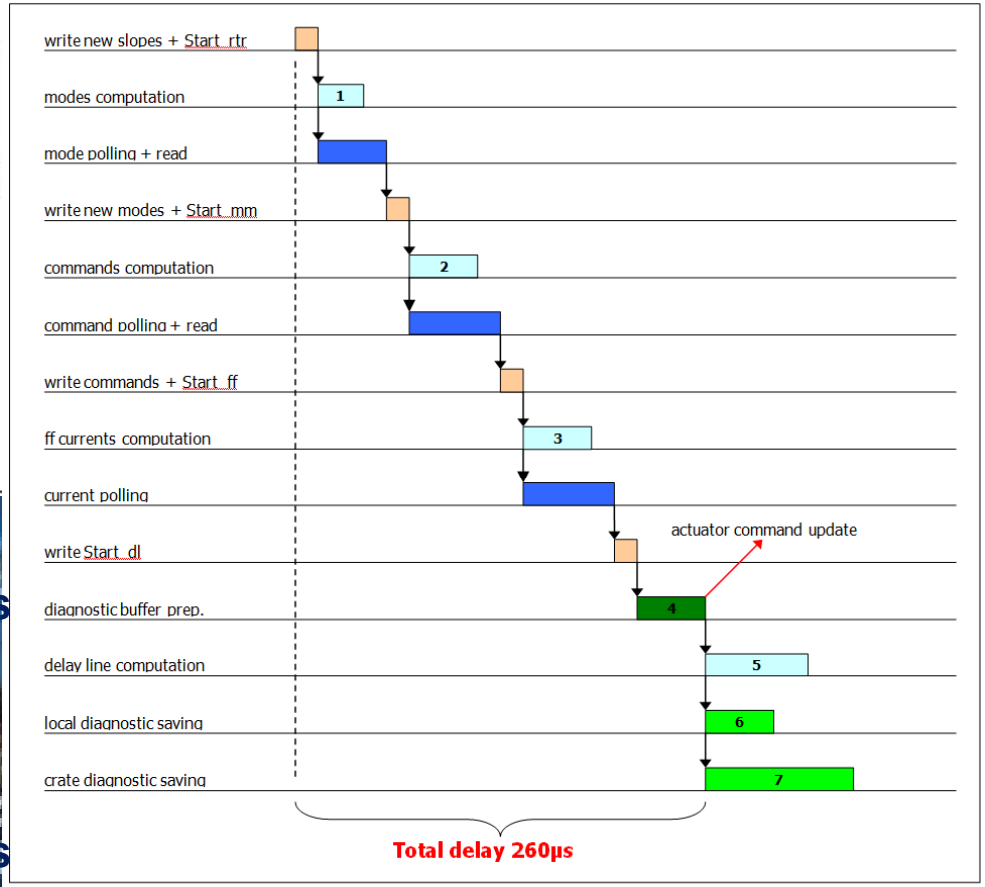
$$\{\Delta m\}_i = [B]_0\{S\}_i + \ldots [B]_n\{S\}_{i-n} - [A]_1\{\Delta m\}_{i-1} - \ldots [A]_m\{\Delta m\}_{i-m}$$
$$\{\Delta p\}_i = [m2p]\{\Delta m\}_i$$

- LBT: 3 zeros, 3 poles full state (672 d.o.f) MIMO filter

Main Applications



RTR Performances



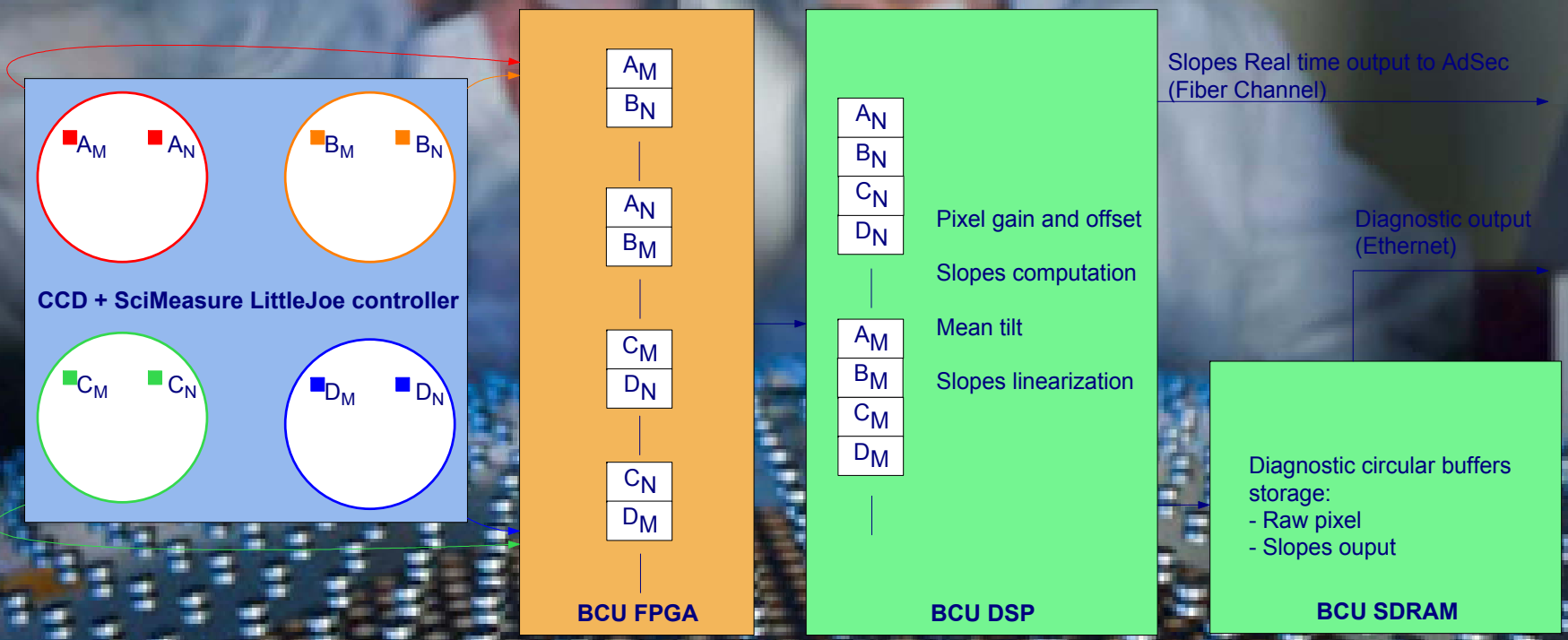
- **LBT**
  RTR + Global DM control + shell safety: **260µs**
- **Keck**
  RTR + TT & DM update: **110µs**
- **VLT**
  RTR + Global DM control + shell safety: **130µs**

MICROGATE ENGINEERING

Main Applications

Slope computers

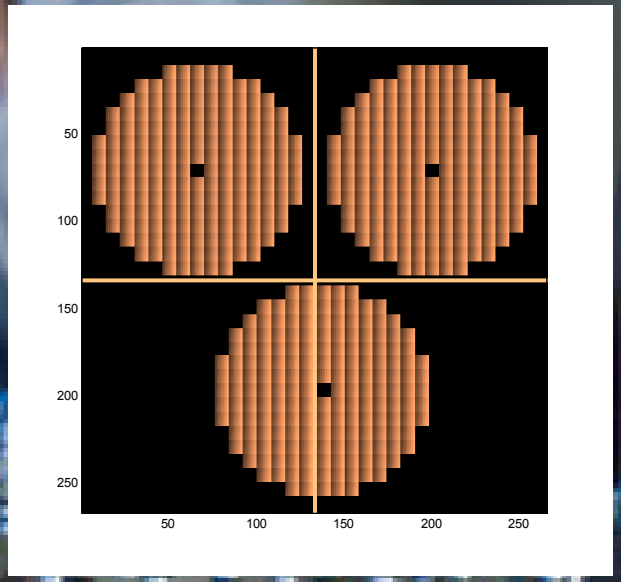
- Flexible system, can be configured for pyramid and SH wavefront sensors by reprogramming a LUT
- Pipelined operation: zero latency for all implemented cases, including pyramid
- Interfaced to several CCD controllers and CCDs: SciMeasure CCD39, CCDi56, CCD50, Andor, ...



Main Applications

Slope computer for the LBT ARGOS LGS system

- Includes 8 high speed, very low noise ADC acquisition channels (pnCCD)
- 3x SH implementation, 264x264 pixels, 3x200 8x8pixel subaps
- almost fully pipelined operation, 60µs latency after last pixel acquisition



MICROGATE ENGINEERING

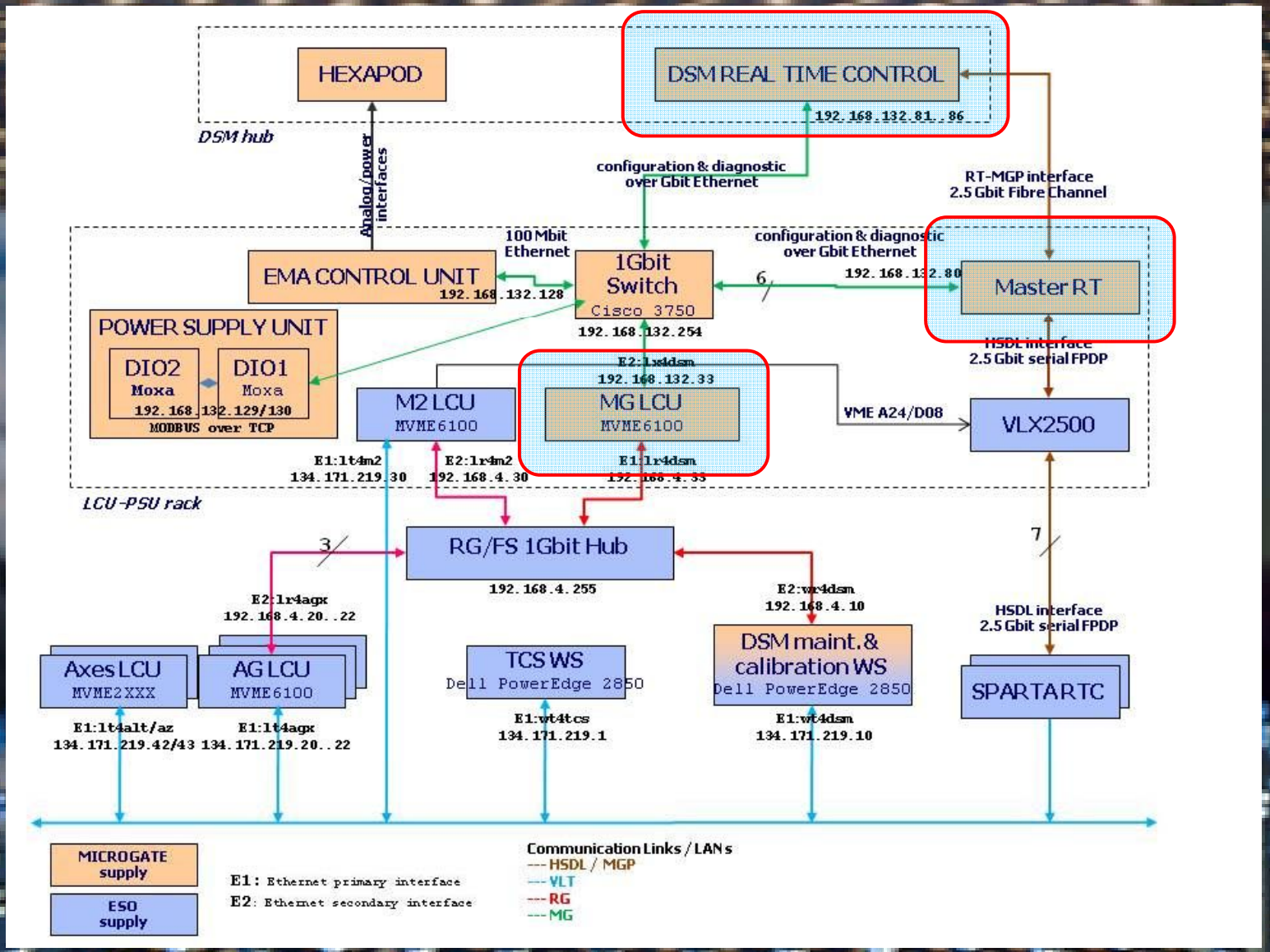
Software

- Hard real time DSP software runs without operating system (ISR + main loop)
- Synchronization through real-time communication
- One BCU acts as arbiter and controls 'data recirculation' for parallel processing
- Deterministic timing with extremely low jitter, sub-microsecond level
- Very efficient real-time diagnostic buffering system, implemented on hardware

- Real-time system 'hidden' behind a host machine interfaced by standard Ethernet
  LBT: Linux workstation (designed and implemented by INAF-Arcetri)
  Keck and VLT: single board computer running under VxWorks

- Low-level communication based on simple read-write protocol with direct access to all embedded devices (DSPs, FPGA, bulk memory)

Software

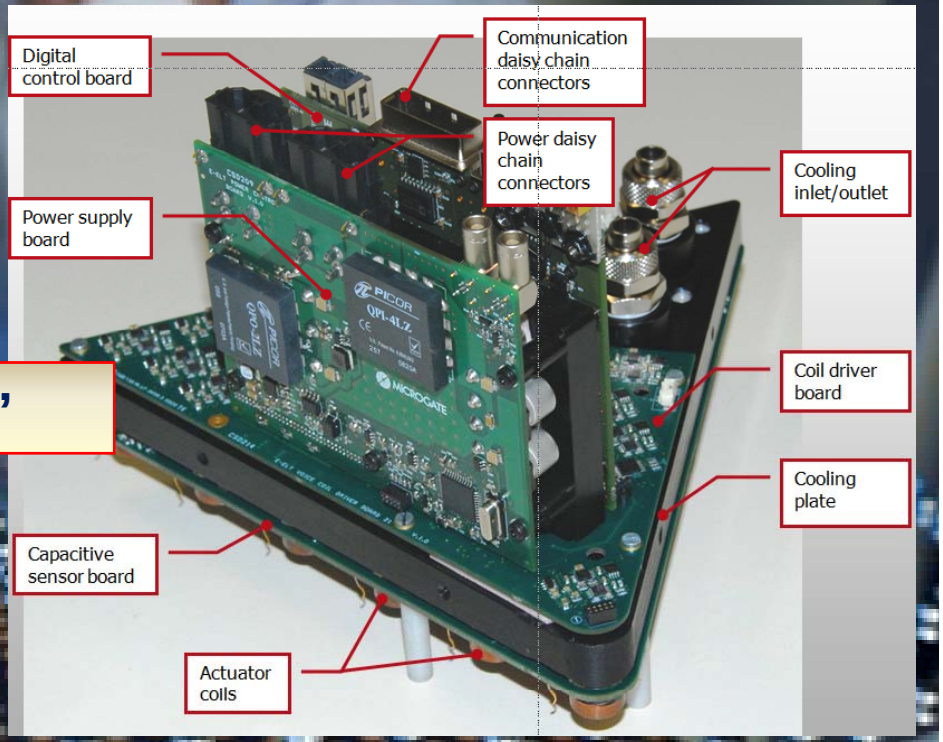

HEXAPOD
DSM REAL TIME CONTROL
192.168.132.81..86
DSM hub
Analog/power interfaces
configuration & diagnostic over Gbit Ethernet
RT-MGP interface 2.5 Gbit Fibre Channel
100 Mbit Ethernet
EMA CONTROL UNIT
192.168.132.128
1Gbit Switch
Cisco 3750
192.168.132.254
configuration & diagnostic over Gbit Ethernet
192.168.132.80
Master RT
POWER SUPPLY UNIT
DIO2
Moxa
192.168.132.129/130
MODBUS over TCP
DIO1
Moxa
E2:lx4dsm
192.168.132.33
HSDL interface 2.5 Gbit serial FPDP
M2 LCU
MVME6100
MG LCU
MVME6100
VME A24/D08
VLX2500
E1:lt4m2
134.171.219.30
E2:lr4m2
192.168.4.30
E1:lr4dsm
192.168.4.33
LCU-PSU rack
RG/FS 1Gbit Hub
192.168.4.255
E2:lr4agx
192.168.4.20..22
E2:wx4dsm
192.168.4.10
HSDL interface 2.5 Gbit serial FPDP
Axes LCU
MVME2XXX
AG LCU
MVME6100
TCS WS
Dell PowerEdge 2850
DSM maint.& calibration WS
Dell PowerEdge 2850
SPARTA RTC
E1:lt4alt/az
134.171.219.42/43
E1:lt4agx
134.171.219.20..22
E1:wt4tcs
134.171.219.1
E1:wt4dsm
134.171.219.10
MICROGATE supply
ESO supply
E1: Ethernet primary interface
E2: Ethernet secondary interface
Communication Links / LANs
HSDL / MGP
VLT
RG
MG

FPGA-only based control

E-ELT M4 deformable mirror control unit

- Line Replaceable Unit comprehending ~30 actuators, control electronics and supply
- Global control moved away from adaptive unit
  → on-board power minimized
- Simplified interfaces and harness (supply, data, cooling)
- Sound maintenance concept, maximize system availability
- **FPGA-based local control**
- Parallel/pipelined implementation
- Minimum latency, **~400ns** control loop computational delay, 36ch controlled by one single FPGA

E-ELT M4 'brick'



MICROGATE ENGINEERING

Lessons learned

- Positive experience with **dedicated electronics**
  (is it really custom? More than 500 MIC DSP boards produced...)
- COTS are not trouble-free and support over system lifetime can be an issue
- Expandability, true parallel architecture, **very efficient data recirculation** are mandatory for demanding processing application (real world is **never** just a **matrix-vector multiply**...)
- **Hardware acceleration** is appealing but **development/debugging time** shall not be underestimated (FPGA vs. DSP, HW vs. SW)
- Diagnostic/telemetry tasks shall be carefully evaluated – need for **independent paths for real-time and diagnostic communication**
- Importance of an abstraction layer to **hide the hardware complexity** and to define a clear interface to the other layers (e.g. VLT DSM with VLT TCS and SPARTA)

Perspectives

- The Contactless Deformable Mirror control electronics development remains an important niche for Microgate (it's not only real time processing...)
- For ELT-class DMs, with several thousands of actuators, it is more effective to de-localize the global DM control computation (motivations: on board dissipation, well defined modular design, maintainability, ...) → comparable problem and complexity of AO RTR
- We also intend to remain in the AO RTC field
- Therefore, we are about starting a development project (partially founded by ProvBZ), with the goal of implementing an acceleration hardware, hosted on standard PCs, with a flexible and modular software approach, and well aligned with the ELTs standard interfaces. Detailed workplan still under definition
- Project team:
  - Microgate
  - Politecnico di Milano – Dipartimento di Ingegneria Aerospaziale (prof. Morandini)
  - Industrial Mathematics Institute - Johannes Kepler University Linz (prof. Ramlau)

Conclusion