DMDE

Deformable Mirror Drive Electronics

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Summary

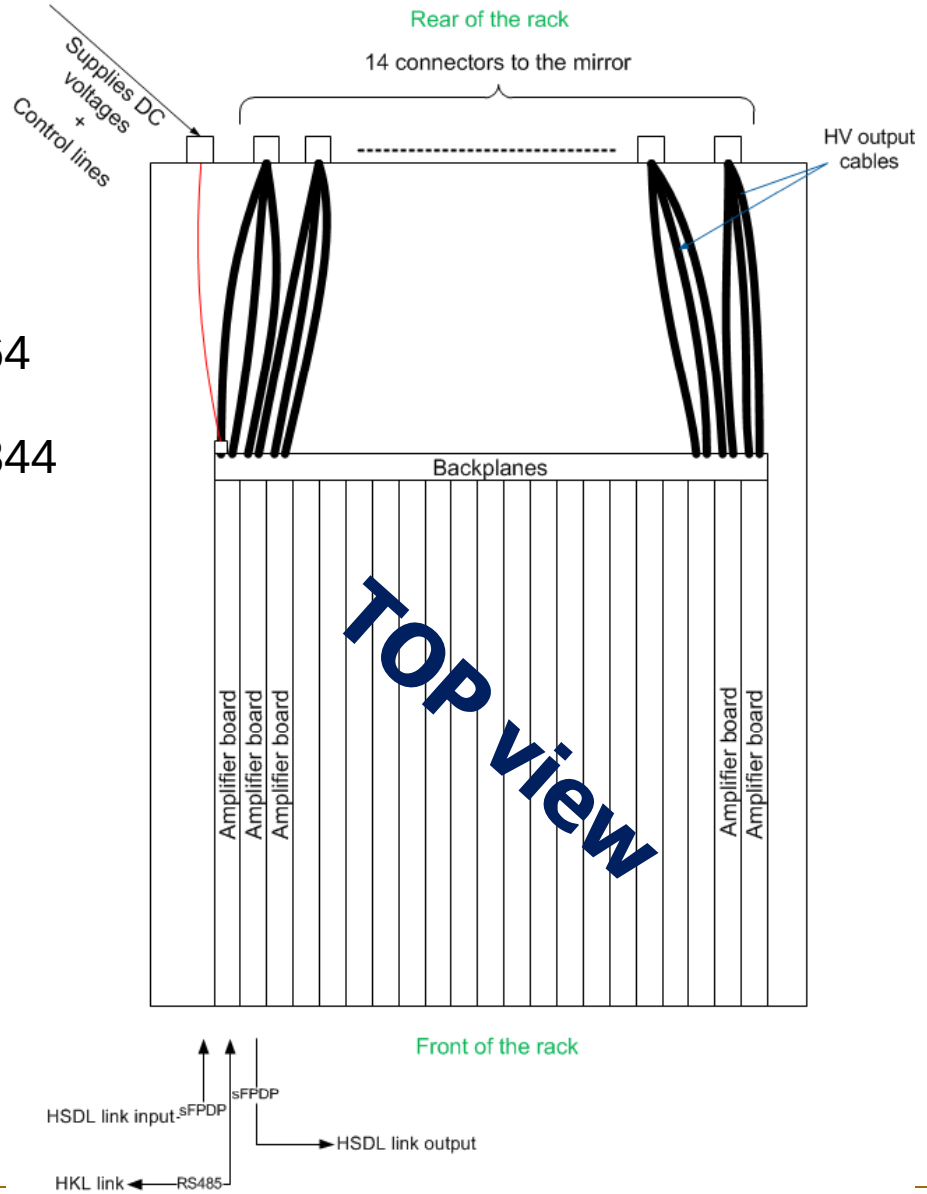
- Requirement
- Architecture
  - DMDE rack
  - Interfaces
  - Additional equipment
  - Multiple DMDE
- DMDE boards
  - Amplifier board
    - HV channel
  - Control unit board
    - Architecture
    - Features
  - Power consumption
- Exchange protocol
  - sFPDP link
  - House Keeping link
- Timing

Mains requirements

- Actuator drive voltage : -400V to +400V
- Actuator and cable capacitive load : up to 22nF
- Maximal slew rate : 100V/ms
- High speed real time commands link
- Low latency time response
- Drive a high number of actuators (up to 10000)

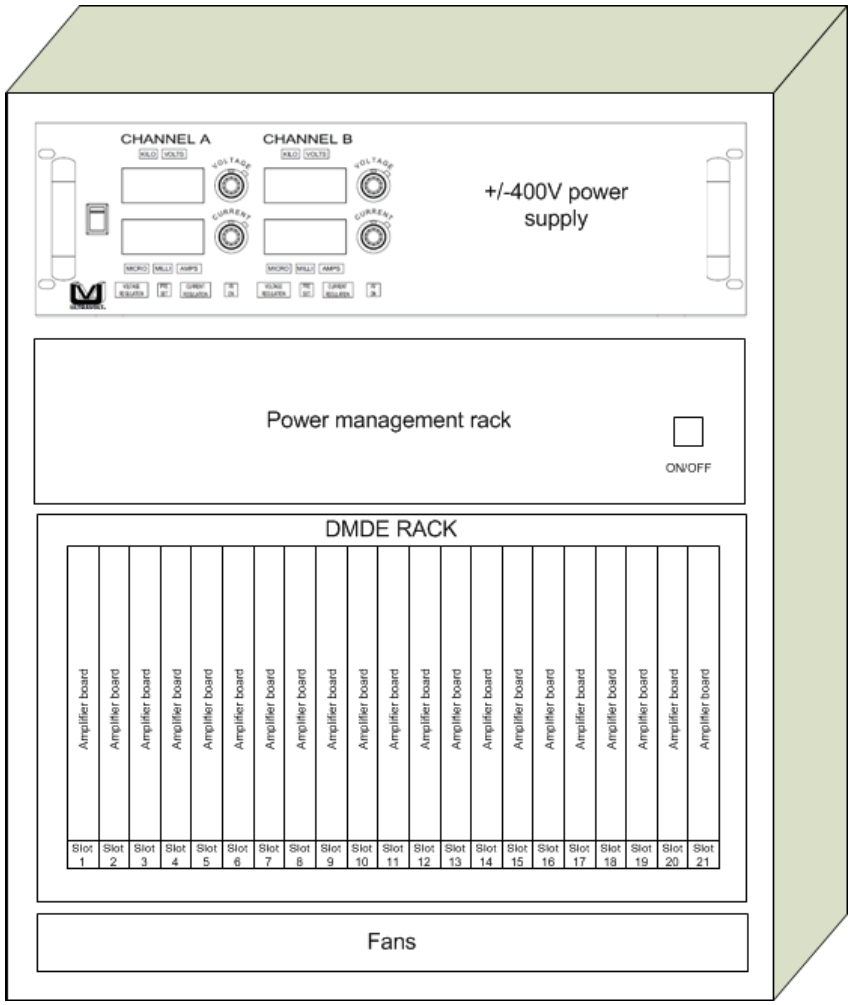
Architecture: DMDE rack

- DMDE rack:
  - 19” rack, 9U high, 600 mm depth
  - Include 21 amplifier boards with 64 HV amplifier channels
  - Total number of HV channels : 1344
- DMDE front rack interface:
  - High speed data link : sFPDP
  - Housekeeping Link : RS485
- DMDE rear rack interface:
  - 1 supplies voltage + control lines connector
  - 14 HV outputs connectors



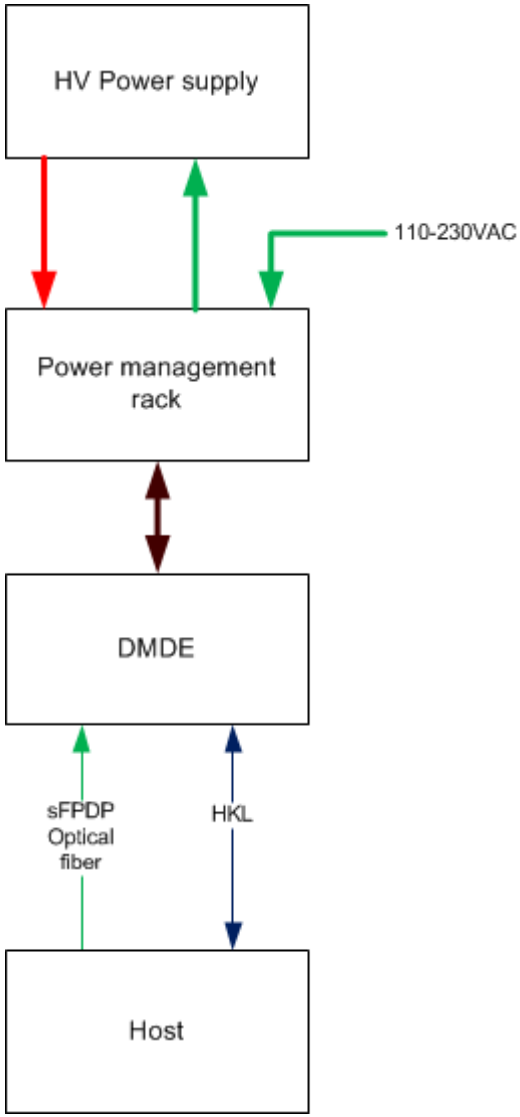
Architecture: Additional equipments

- Power rack management:
  - 19” rack, 3U high, 400 mm depth
  - Include the main power supplies required by the DMDE
  - Include security
- High voltage power supply:
  - OEM equipment on the shelves
  - Delivers +420V and -420V



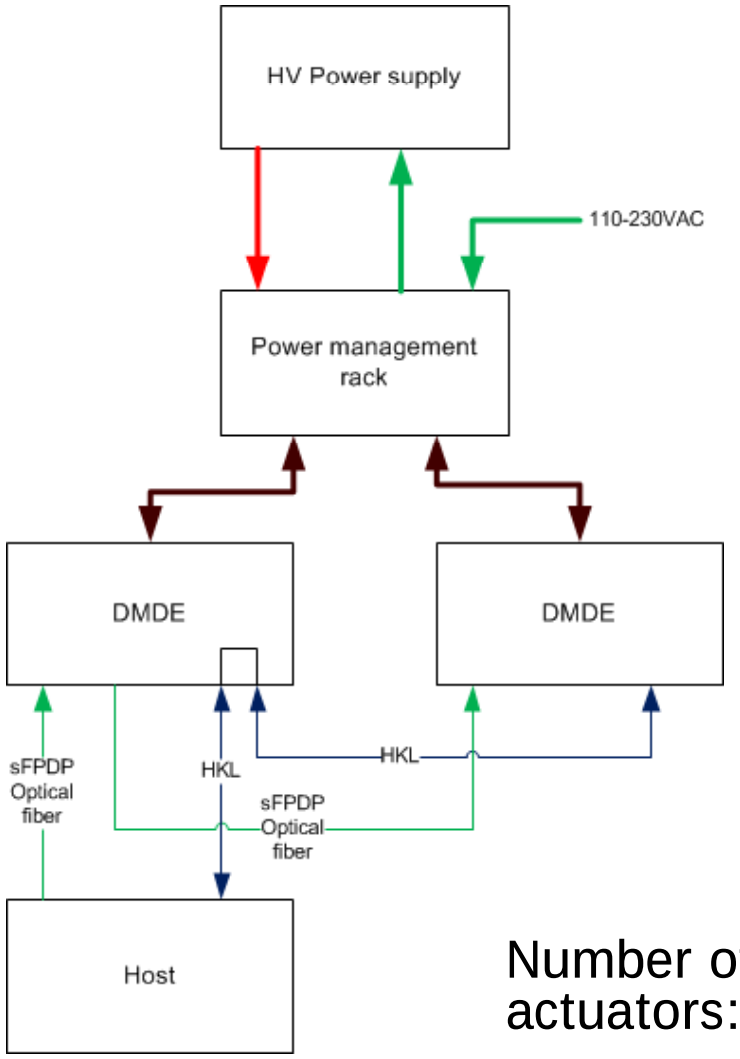
Architecture: capability of control

- Up to 8 DMDE can be used simultaneously ➔ 11104 actuators.
- sFPDP input link:
  - Provided by host computer
  - Can be chained between DMDE
- Housekeeping Link:
  - Provided by host computer
  - Can be chained between DMDE

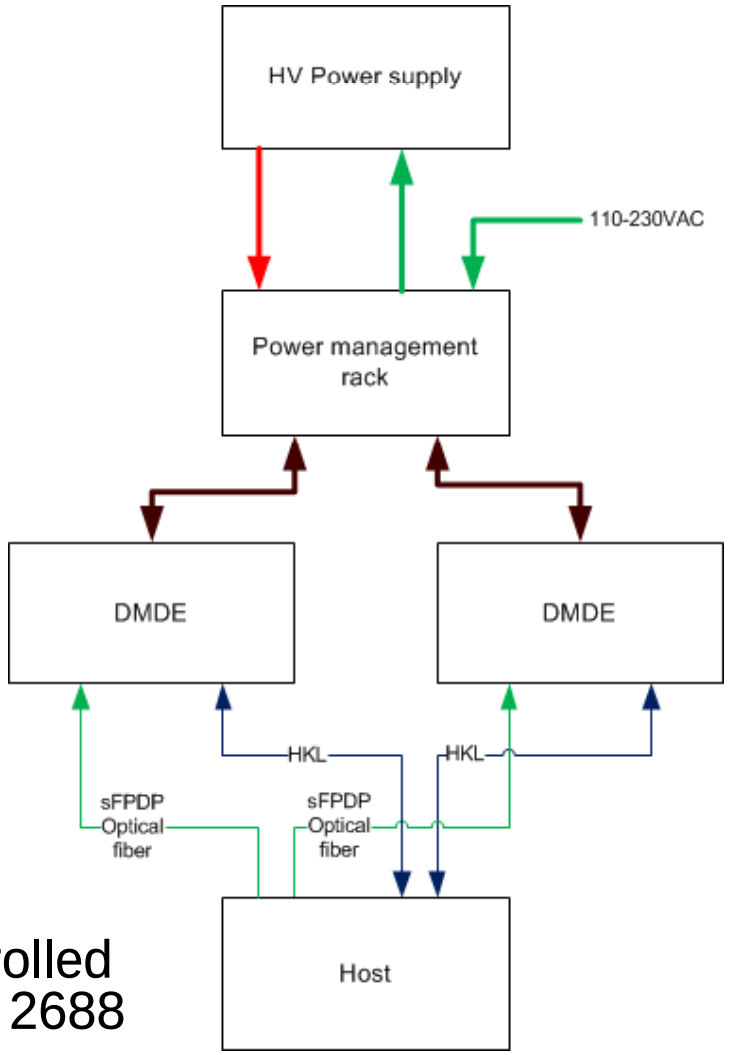


Architecture: 2 DMDEs

Host with 1 sFPDP link and 1 HKL

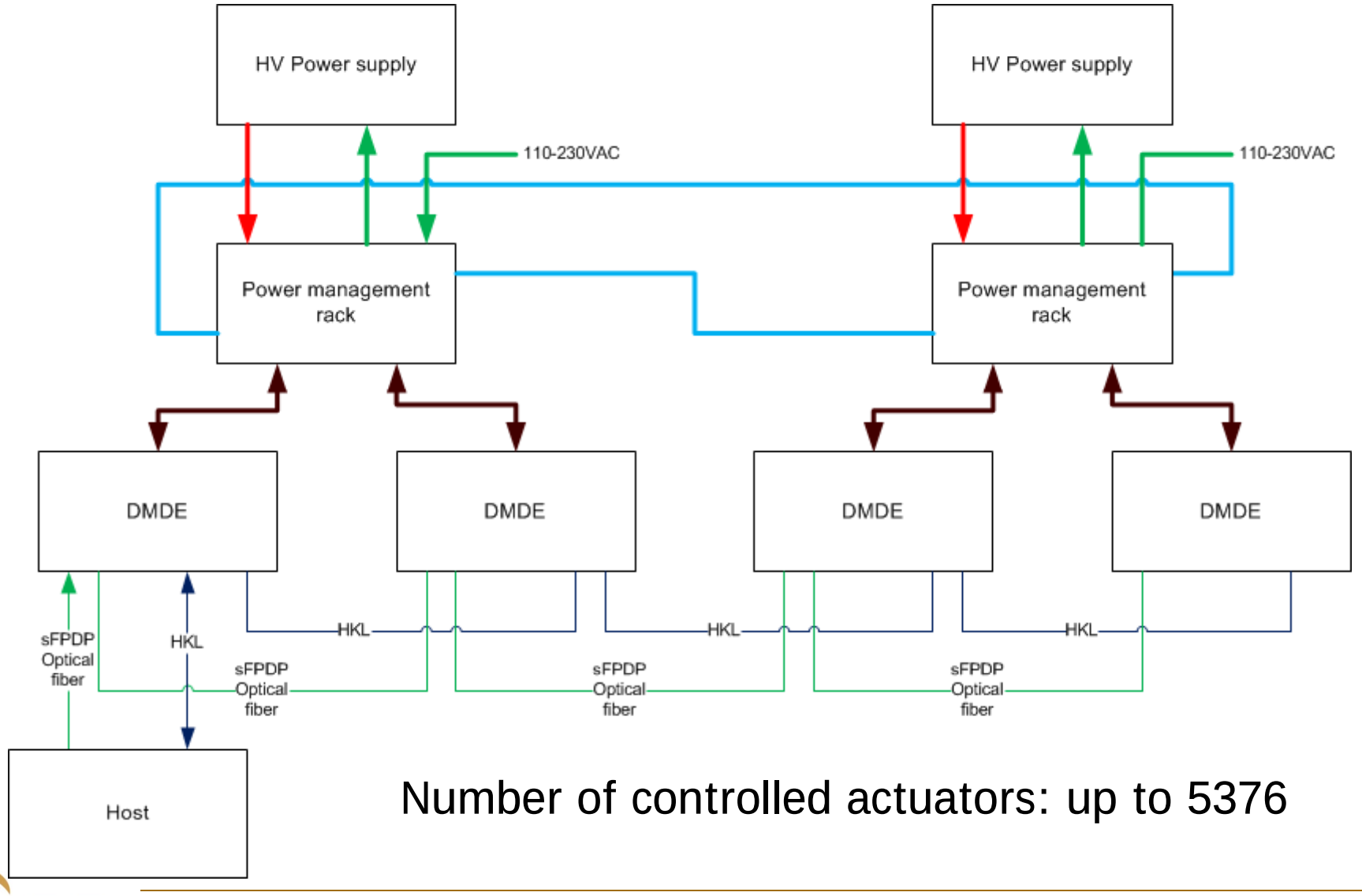


Host with 2 sFPDP link and 2 HKL



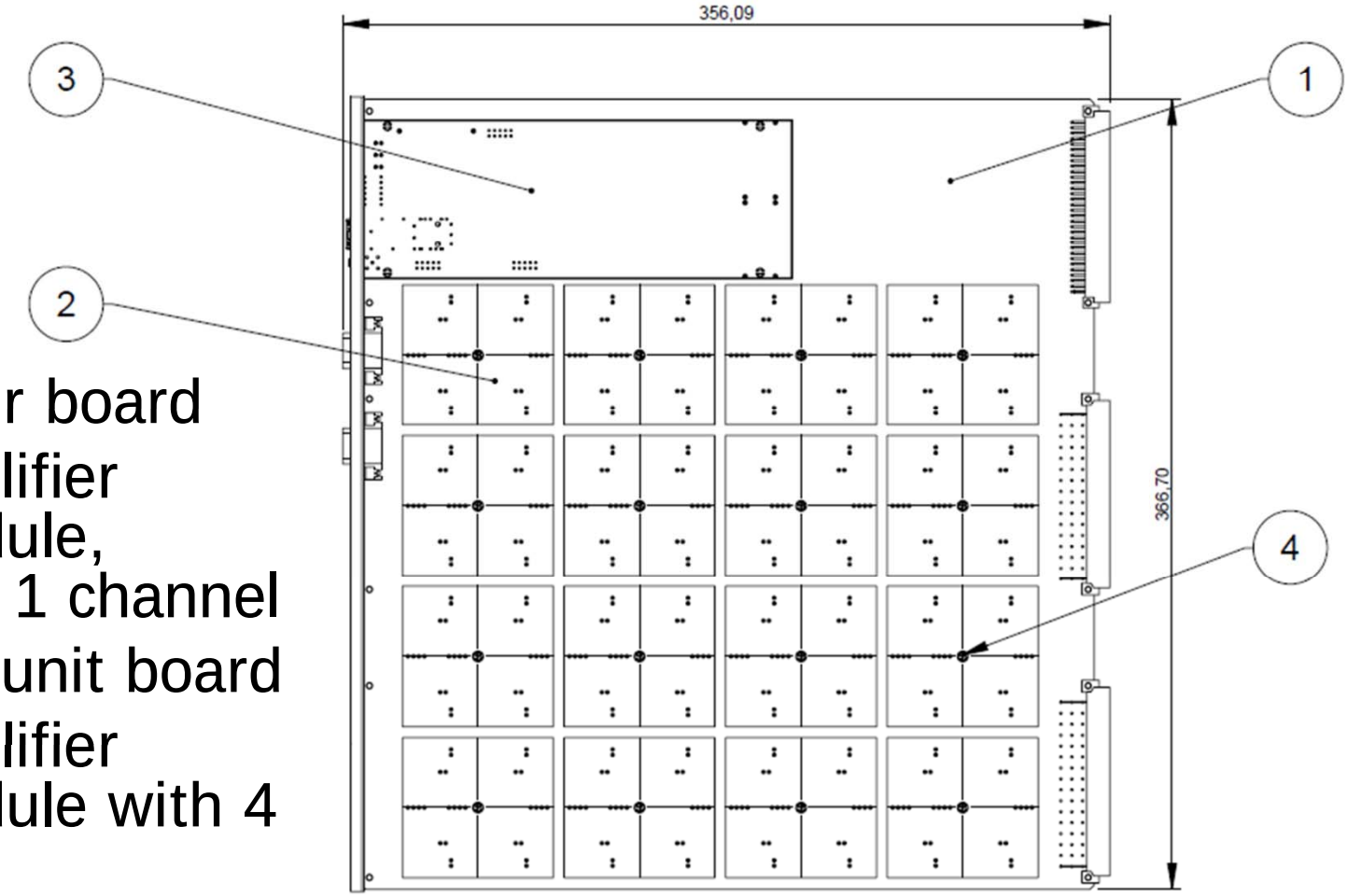
Number of controlled actuators: up to 2688

Architecture: 4 DMDEs



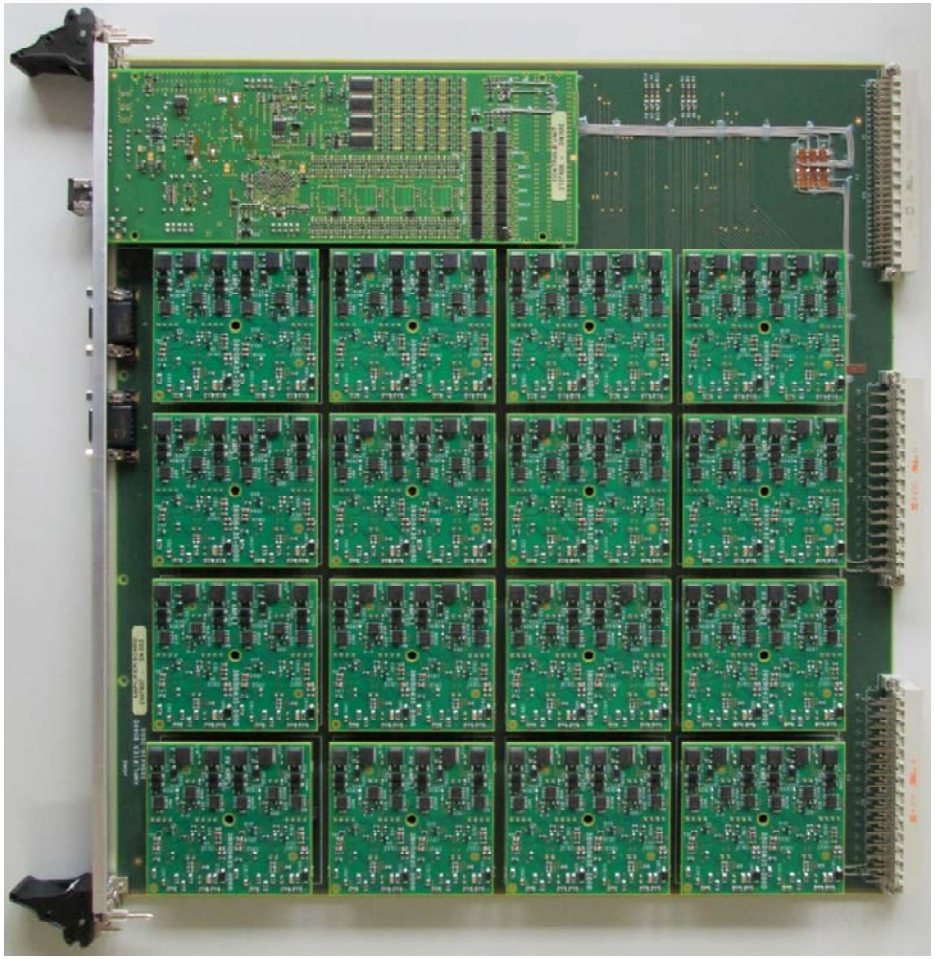
Number of controlled actuators: up to 5376

DMDE: amplifier board



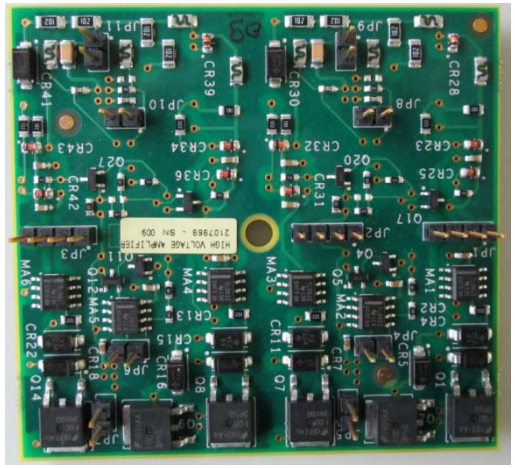
- 1: Amplifier board
- 2: HV amplifier board module, location of 1 channel
- 3: Control unit board
- 4: HV amplifier board module with 4 channels

DMDE: photos



Amplifier board equipped

Control unit board

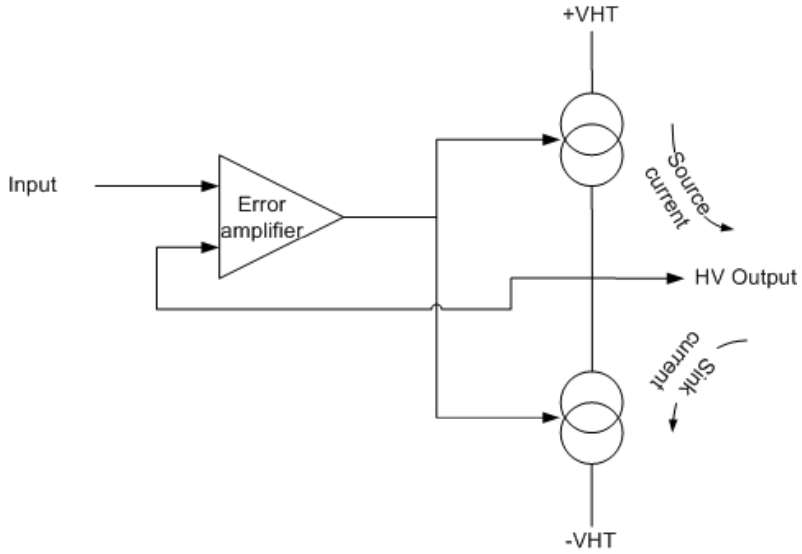


HV amplifier board module

DMDE: HV amplifier channel features

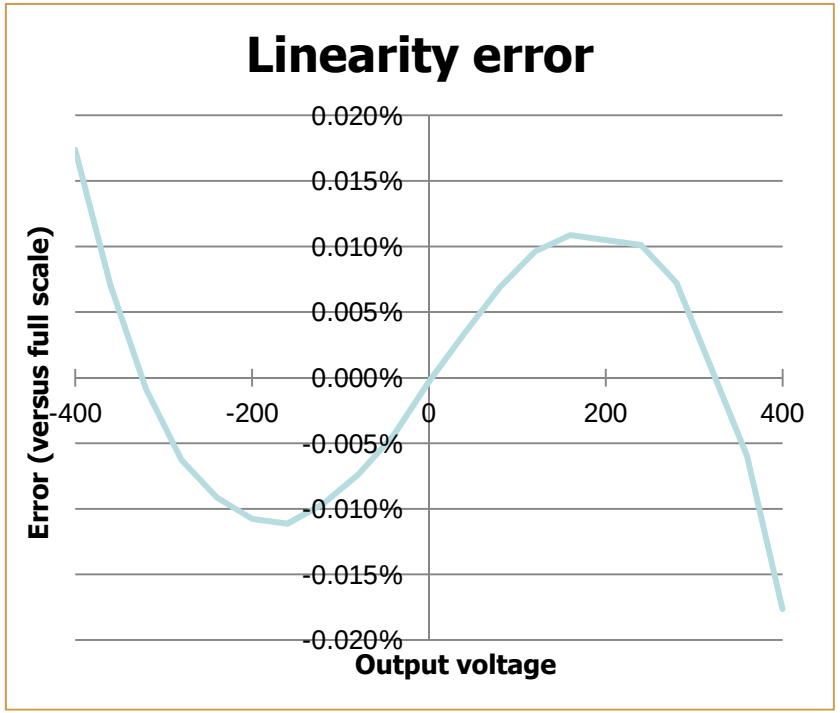
One source current generator and one sink current generator driven by one error amplifier.

- Output voltage: ±400V
- Output load: up to 25nF.
- Maximal output current ±10mA.
- Stable without load



DMDE: HV amplifier channel

- Low consumption:
  - 195mW at 22.5°C
  - 250mW at 50°C
- Accuracy:
  - Gain thermal stability: 35ppm/°C typ
  - Output voltage linearity error at 20°C: <0.02% of the full range
  - Offset: ±0.36V typ
  - Offset drift: ±3.4mV/°C typ
- Maximal output current ±10mA ➔ 450 V/ms with 22nF load
- Output noise: 30mV pkpk with a 22nF load
- Experimental bandwidth:
  - 4.7nF: 10kHz
  - 10nF: 4.7kHz
  - 22nF: 2kHz



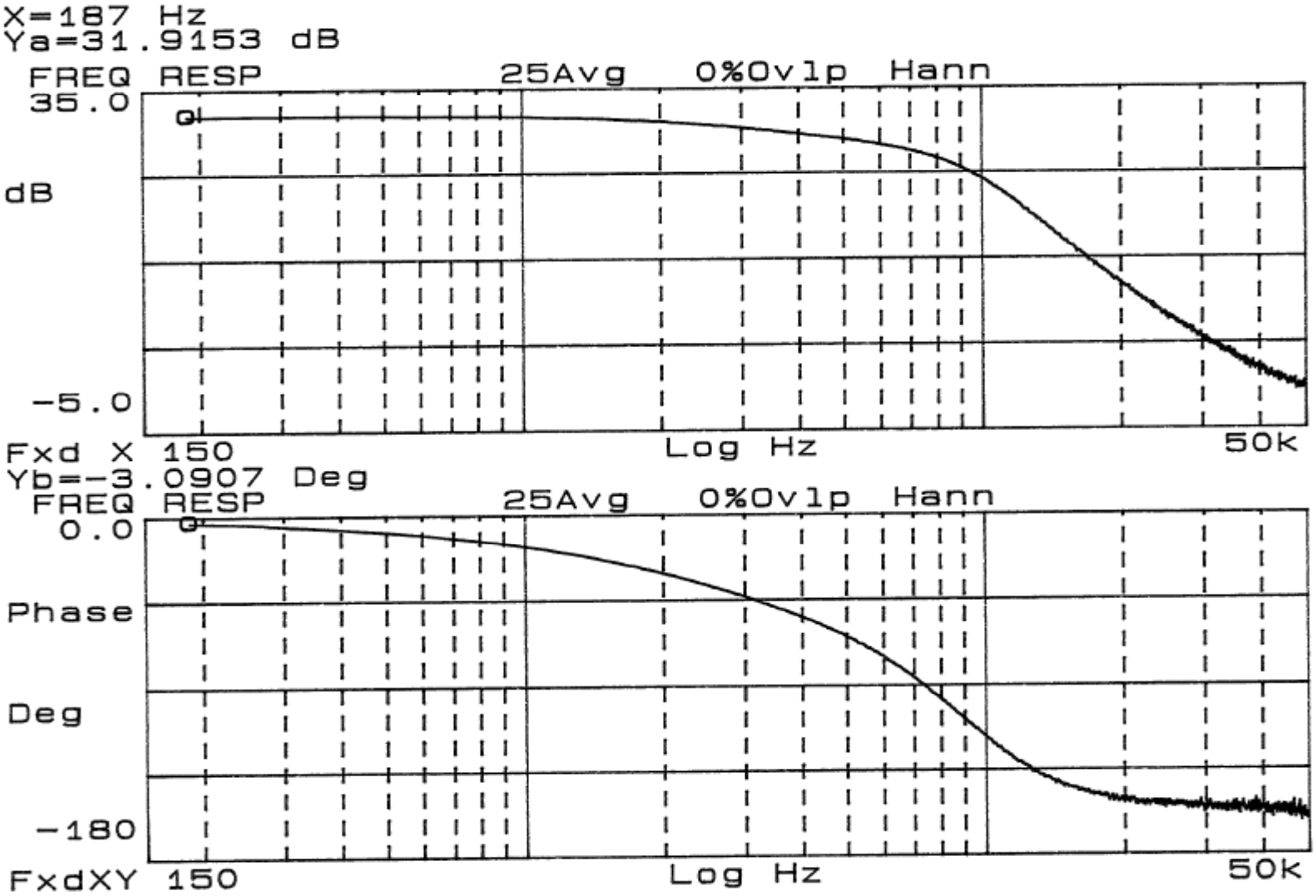
DMDE: HV amplifier channel

10KHz bandwidth with 4.7nF load

- The amplifier features are:

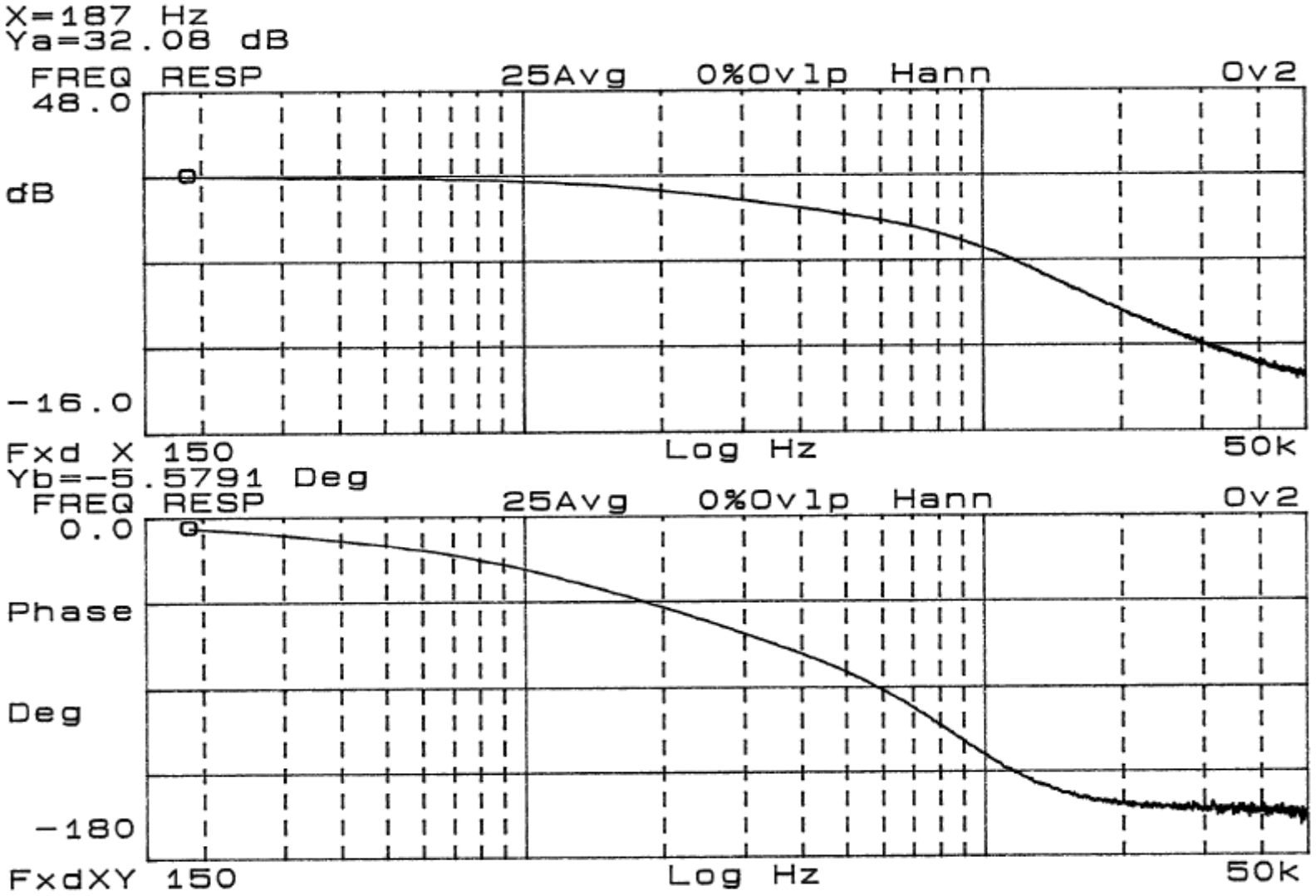
DMDE: HV amplifier channel

4.7kHz bandwidth with 10nF load



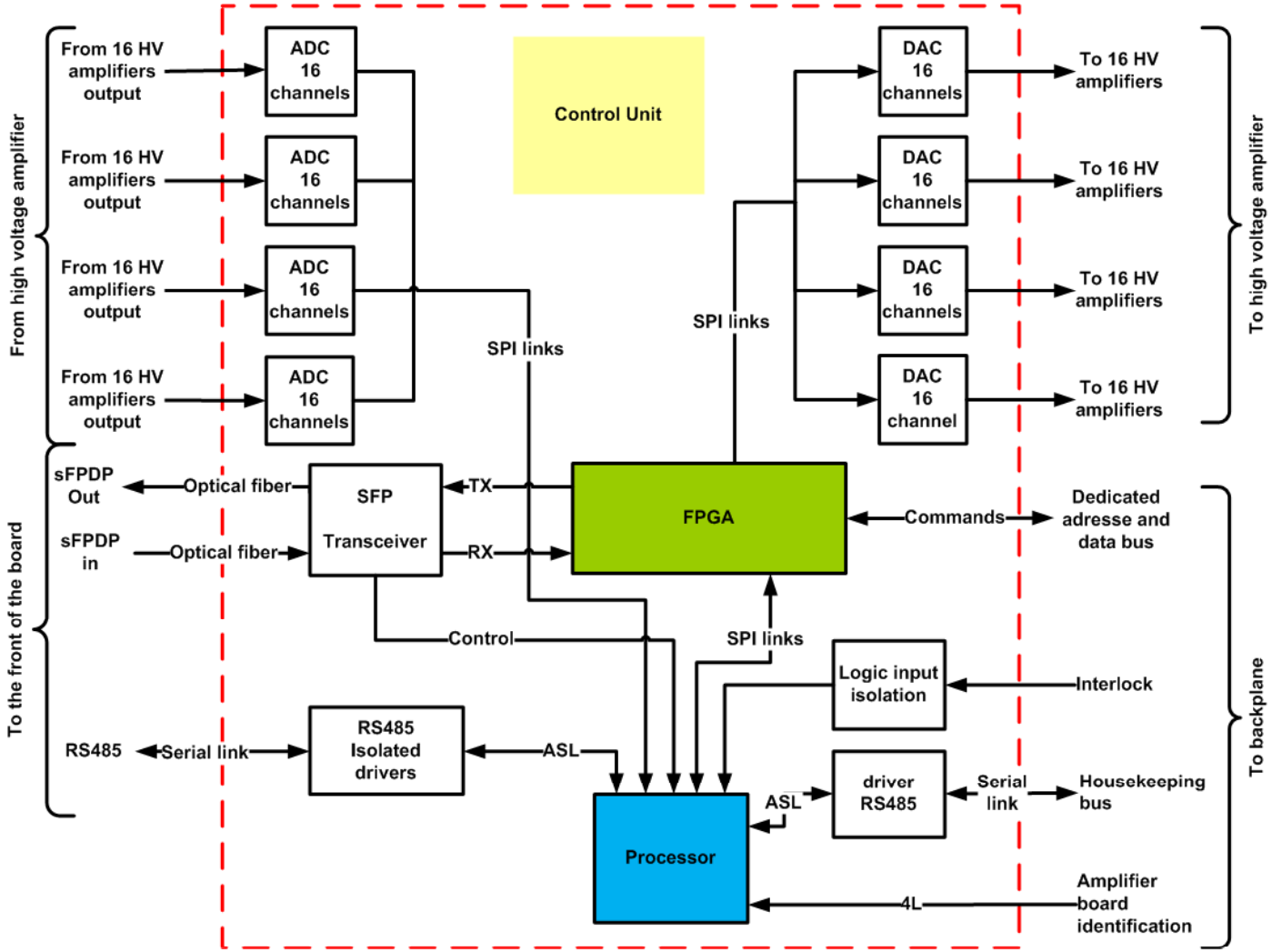
DMDE : HV amplifier channel

2kHz bandwidth with 22nF load



DMDE: Control unit board

- Main parts:
  - FPGA
  - *Processor*
  - *DAC*
  - *ADC*

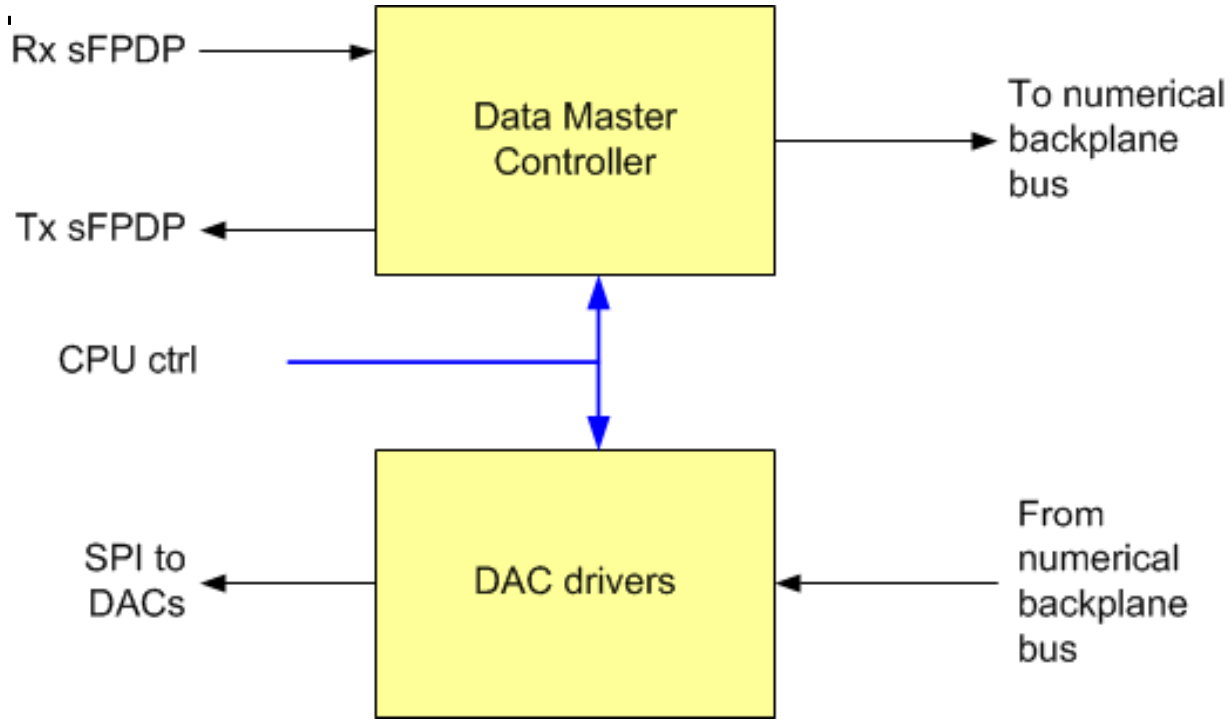


DMDE: Control unit board
Main features

- FPGA :
  - Connected to the sFPDP link if master
  - Process the commands sent by the sFPDP
  - Drive the DAC
- *Processor*
  - *In charge of the housekeeping*
  - *Data exchange by the serial link*
  - *Check the HV output by acquisition of the HV with the ADC*
  - *Manages the board as*
    - *slave (position 2 to 21 inside the rack)*
    - *or master (position 1 inside the rack)*
  - *Check the interlock security*
  - *Check all the power supplies*
- *DAC : 14 bits*
- *ADC : 12 bits*

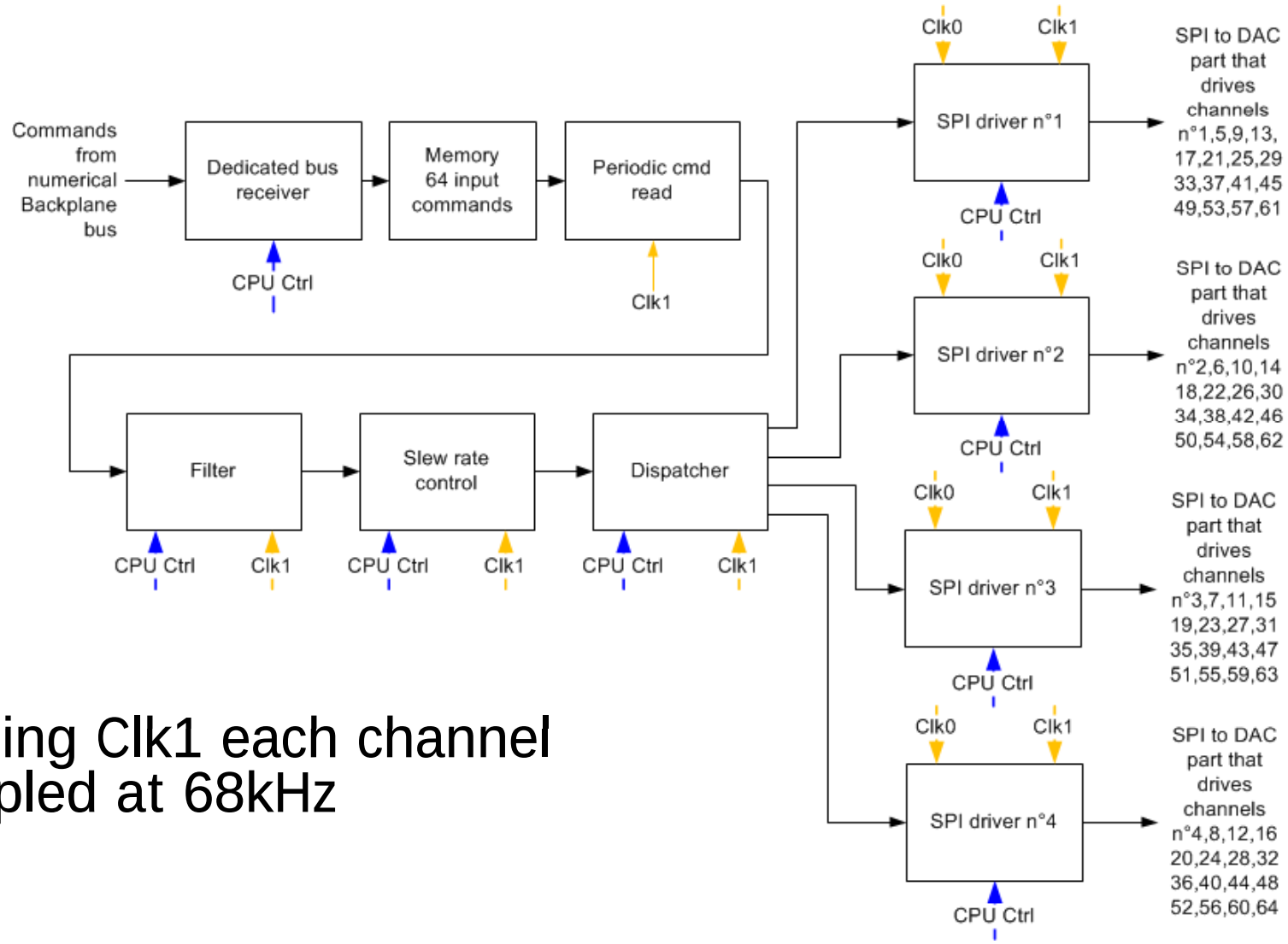
DMDE: Control unit board FPGA architecture

- FPGA :



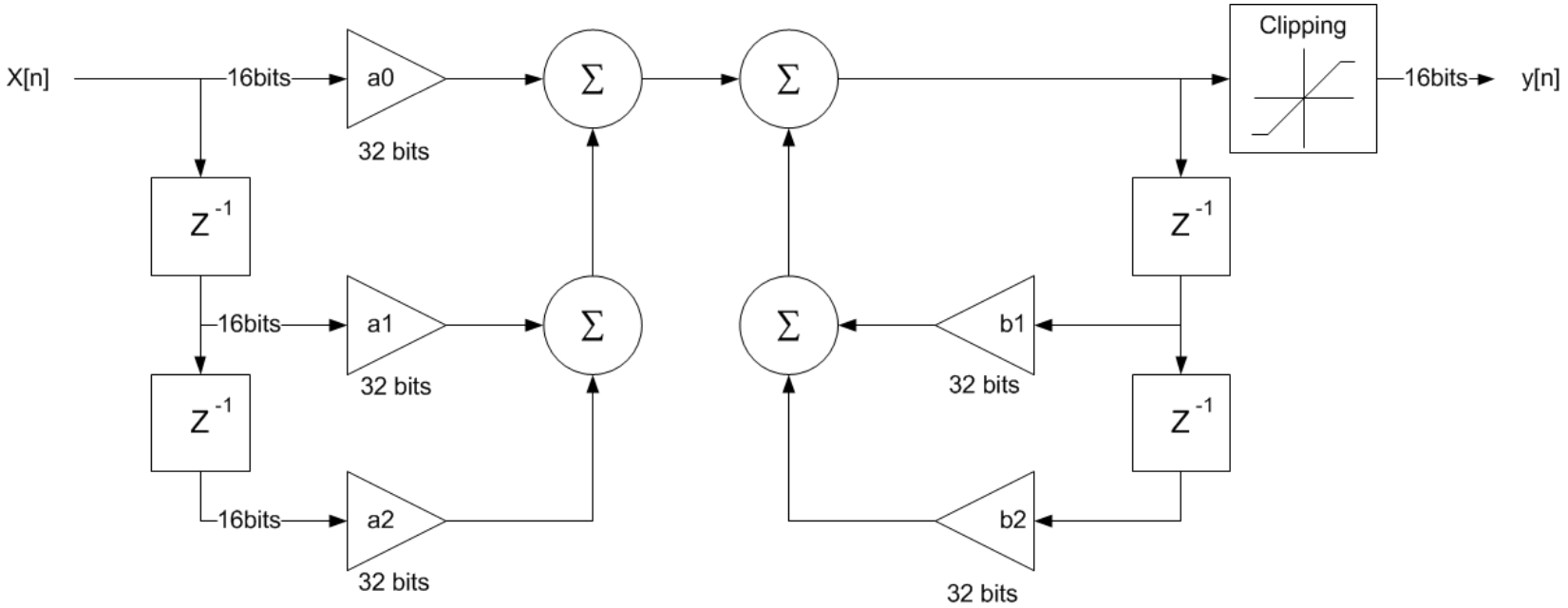
DMDE: Control unit board

FPGA DAC drivers



- According Clk1 each channel is sampled at 68kHz

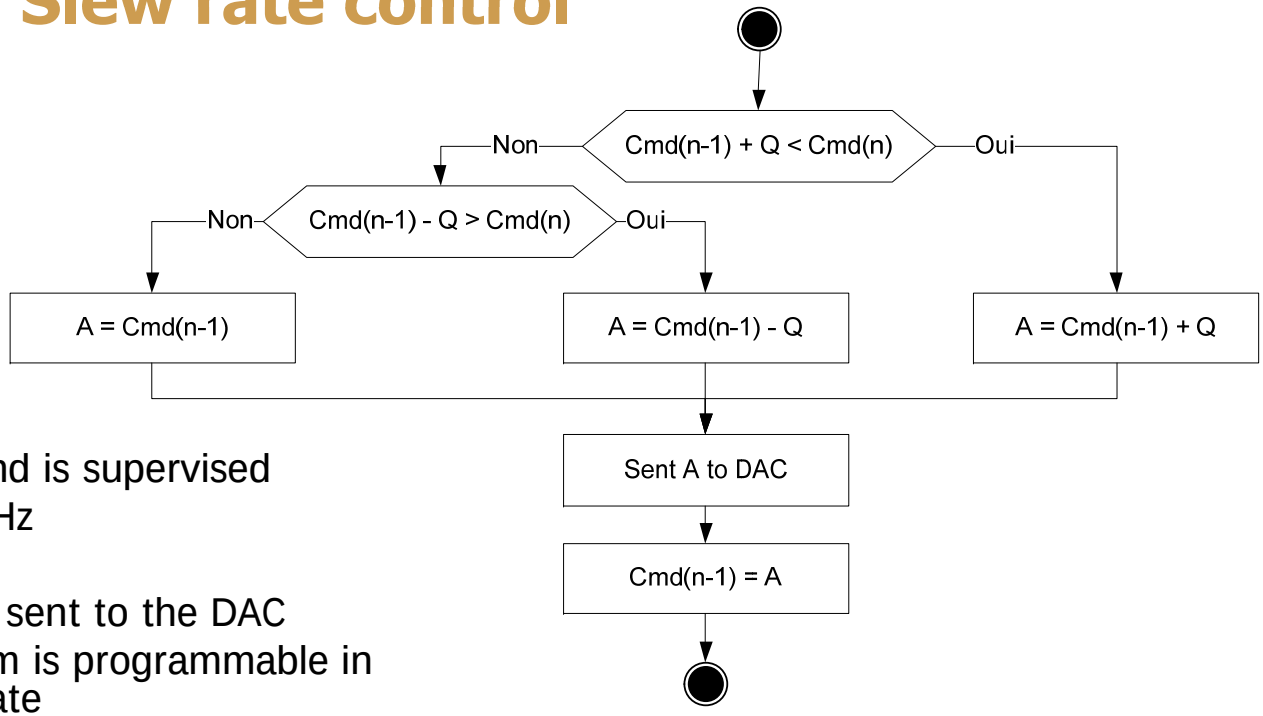
DMDE: Control unit board
Commands filter



- Sampling frequency: 68kHz
- The numerical filter is a first order or second order.
- This filter can be bypassed.
- The filter coefficients are the same for all the channels.
- High precision computation to get low cut-off frequency.

DMDE: Control unit board

Slew rate control



- Slew rate of each command is supervised
- Sampling frequency : 68kHz
- Cmd(n) : new command
- Cmd(n-1) : last command sent to the DAC
- Q : quantum, this quantum is programmable in order to adjust the slew rate
- Minimal slew rate value: 3.5V/ms

NOTICE

For CILAS mirror, the maximal slew rate value is clipped at the 100V/ms by the processor.

DMDE: Power consumption

- The consumption is given:
  - including one DMDE fully populated with 21 amplifier boards (1344 channel).
  - Including the high voltage power supply.

- **In standby (without dynamical commands):**

Estimated power consumption on main power supply 230 or 110VAC 50/60Hz :

520 (W)

- **For a worth case due to the following conditions:**
  - Load : 23.2 nF
  - Dynamic output voltage : 40Vrms noise, 100Hz bandwidth
  - 50°C (worth case)

Estimated power consumption on main power supply 230 or 110VAC 50/60Hz :

800 (W)

DMDE: sFPDP exchange Protocol

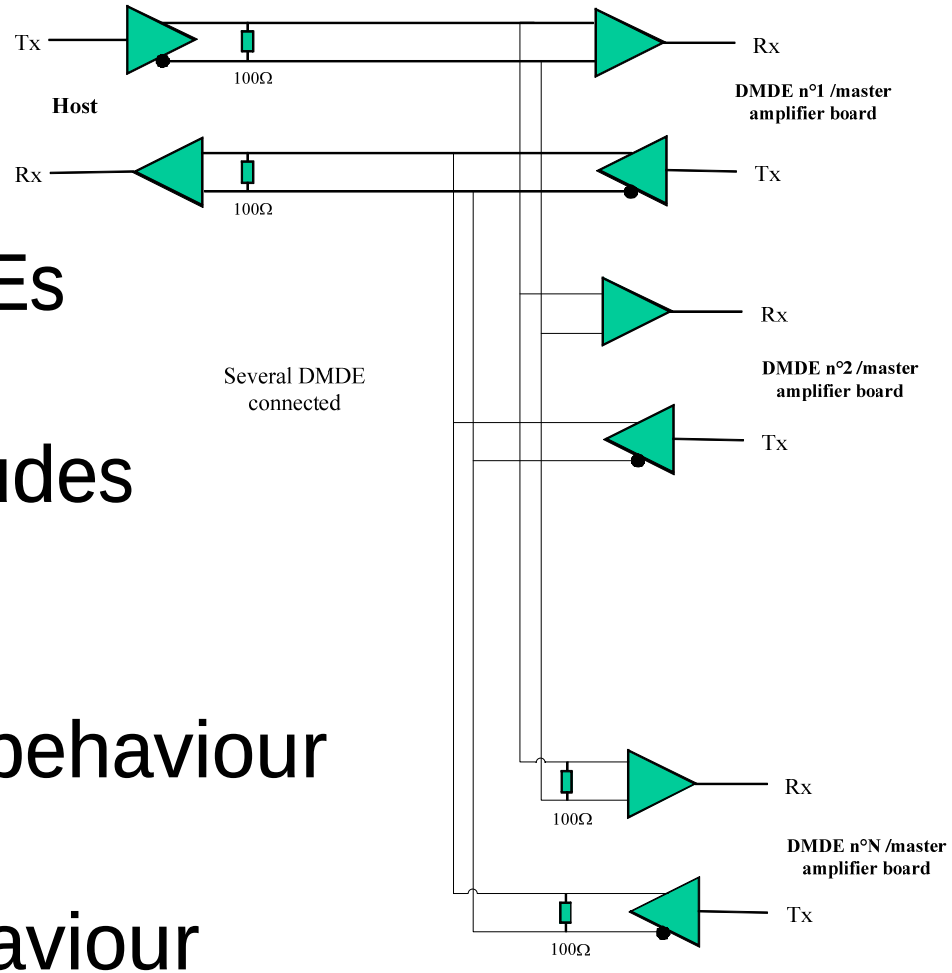
- sFPDP compatibility
  - Frame structure with :
    - Normal Data Frame
    - SYNC without Data Frame
    - SYNC with Data Frame
  - CRC is enabled
  - Copy loop mode activated (data transmitted to the next DMDE)
- Exchanged data between the host and the DMDE are packed inside messages
- Messages are packed in sFPDP frames
- All messages shall be ended with a SYNC

DMDE: sFPDP messages

Header	**32 bits word** **The 16 LSB bits give the first channel that will receive the first data.** **The 16 MSB bits give the number M of commands inside the message.**
Commands	**N*32 bits word** **This word contains the commands: Each word contains 2 commands. Inside a word, the first command is contained inside the 16 LSB bits and the second command is inside the 16 MSB bits.** **Each command is 16 bits signed integer (two's complement). Maximal value 0x7FFF gives +400V output.** **Minimal value 0x8000 gives -400V output.** **If M is even, N = M/2.** **If M is odd, N = (M+1)/2. Inside the last word the second command is not taken in account.**

DMDE: Housekeeping link Protocol

- RS488 physical link
- Address several DMDEs
- Header message includes
  DMDE number
- Configure the DMDE behaviour
- Check the DMDE behaviour



DMDE: Timing

- From first command sent by the host to the DAC update, three mains delays:
  - sFPDP transmission
  - Transmission on the backplane bus
  - Sampling and processing of the commands
- sFPDP transmission is done simultaneously with transmission on the backplane

DMDE: Timing

- **Example: let a DMDE rack fully populated (1344 commands)**
  -
- **sFPDP delay: Ts=10.9µs (data transmission) + 700ns (processing)**
- **Backplane delay: Tb=17.9 µs**
- **Commands sampling and processing delay: Tp**
  - **Maximal latency : 17,7µs**
  - **Minimal latency : 3,1µs**
  - **Mean latency : 10,4 µs**
- **DMDE timing ≈ 700ns + Tb + Tp**
  - **Maximal latency : 700ns + 17,9µs + 17.7 µs = 36.3µs**

DMDE: the scheduling and the future

- **End of development: December 2012**
- **GTC:**
  - **1 DMDE with 384 channels (for 373 act. DM)**
  - **Delivery of the first equipment end of march 2013**
- **NSO:**
  - **2 DMDE with 2048 channels (for ATST 1933 act. DM)**
  - **Delivery of the equipment in 2014**
- **Could fulfill the need for:**
  - **TMT (DM0 3125 actuators and DM11.2 4548 actuators)**
  - **ESO HODM (1377 actuators)**
  - **ESO future applications as MAORY (MCAO for the E-ELT)**

Thanks for your attention