Bulk Silicon CCDs, Point Spread Function and Photon Transfer Curves: CCD Testing Activities at ESO

Mark Downing[a] (mdowning@eso.org), Dietrich Baade[a], Sebastian Deiries[a], Paul Jorden[b]
[a]ESO, Karl-Schwarzschild-Strasse 2, 85748 Garching bei München, Germany;
[b]e2v technologies,106 Waterhouse Lane, Chelmsford, Essex, CM1 2QU, United Kingdom.

ABSTRACT

This paper reports on various testing activities at ESO which include: the measured performance of a new Bulk 70 µm thick prototype e2v CCD with high red response, results of point spread function (PSF) measurements, and photon transfer curve non-linearity measurements. Various technology CCDs from standard silicon, deep depletion, and bulk silicon have been tested.

e2v technologies has prototyped a 2kx4k 15µm CCD in bulk silicon which is a plug-in replacement for the very successful range of CCD44-82 CCDs. The CCD44-82 is used extensively on ESO telescopes and at other observatories. Measurements of parameters such as read noise, linearity, dark current, quantum efficiency, photon response non-uniformity and fringing, charge transfer efficiency and PSF show that this device is a true competitor to the existing range of silicon technology devices especially where good response in the "red" and low fringing are important.

Results of measurements of PSF of several CCDs of differing thicknesses are presented along with techniques to improve the PSF.

Non-linearity of the photon transfer curve observed on recent CCDs was reported at the 2006 Orlando SPIE conference. Results of more accurate follow up measurements are presented in this paper that show some very interesting features.

1. INTRODUCTION

The e2v technologies back-illuminated 2kx4k 15µm CCD44-82 (Figure 1) has been successfully used for over a decade at ESO's La Silla Paranal Observatory, and installed in numerous (> 10) ESO instruments and used at many other international observatories. The CCD44-82 is available in a range of options including: a) 16 µm thick standard (100 ohm-cm) or 40 µm thick deep depletion (1500 ohm-cm) silicon, b) full-frame or frame transfer architecture, c) a suite of different Anti-Reflective (AR) coatings including single layer coatings optimized for Broadband, UV, Midband, and the Red and custom coatings such as 2-layer[1] and Graded[2][3].

To add to this range, e2v has recently fabricated a number of engineering and science grade prototypes in 70 µm thick Bulk (3000 ohm-cm) silicon. The Bulk silicon CCD44-82 offers higher red response and lower fringing than previous silicon technologies and thus is very interesting not only for new designs, but for upgrading the performance of existing instruments. As the Bulk CCD44-82 is pin and mechanically compatible with previous silicon variants, upgrades are simple plug and play requiring no mechanical modification or rewiring of cryostats, and no modification to

controllers. The Bulk CCD44-82 uses the same standard clock and bias voltage settings and timing patterns as previous devices. It is therefore possible to improve observing efficiency in the "red" without major cost in manpower, controller, instrument down time, or schedule risk.

e2v is developing much thicker silicon CCDs (Figure 2, and Figure 3 for QE comparison) termed high-Rho out of the same bulk silicon. To obtain reasonable PSF performance, they will require an active substrate biasing. The high-Rho CCDs being thicker should offer even higher red response and lower fringing, however, will require existing cryostat wiring and controller to be modified to accommodate the substrate biasing. The device design also differs from that of the CCD44.

e2v loaned ESO one engineering and one science grade Bulk CCD44-82 for test and evaluation. The objective was to verify the already good performance reported by e2v and to evaluate the trades between using the Bulk CCD compared to the other silicon technologies. Section 2 reports on the measured results of read noise, linearity, dark current, quantum efficiency, photon response non-uniformity, fringing, and charge transfer efficiency. Section 3 compares the PSF measurements of different silicon technologies. Section 4 examines the results of photon transfer curve measurements and well depths.

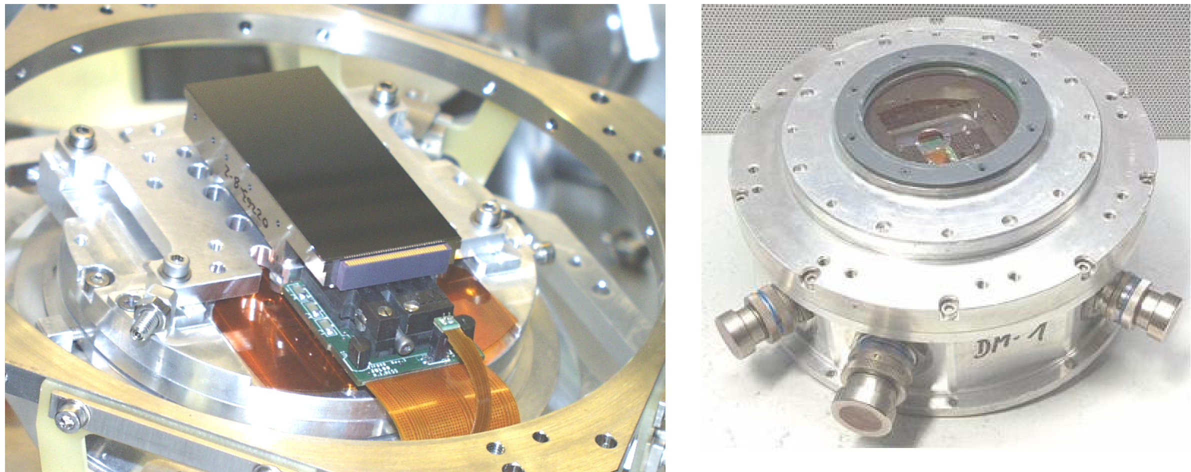


Figure 1: Left: Photograph of an e2v CCD44-82 CCD mounted inside an ESO detector head. Right: Photograph of a standard ESO Detector Head used to test the Bulk CCD.

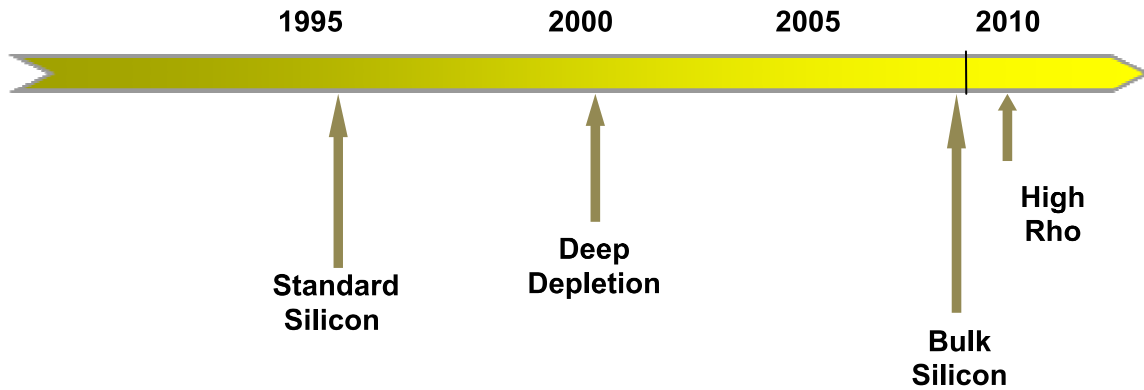


Figure 2: Development timeline of the e2v CCD44-82.

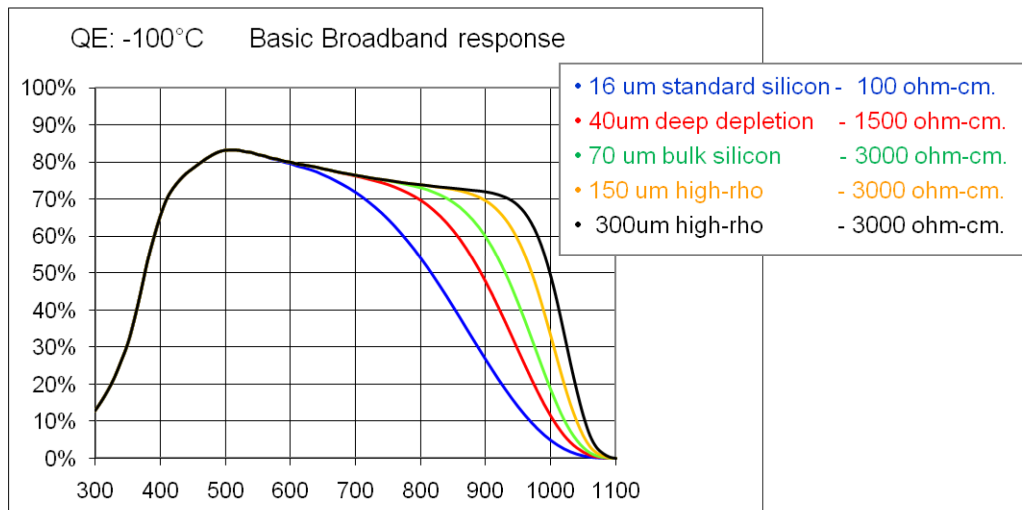


Figure 3: Predicted QE curves of CCDs made from 16 µm Standard, 40 µm Deep Depletion, 70 µm Bulk silicon, and 150 µm and 300 µm high rho silicon. Assumptions used were e2v basic broadband AR coating and -100ºC.

2. BULK CCD RESULTS

The measurements were performed using the FIERA controller on the ESO ODT Test Bench[5]. The ODT Test Bench has an excellent uniform flat field (~ 1% over 10cm x 10cm area) and stability of illumination to enable measurements to be easily carried out to a high degree of accuracy.

The results of testing the Bulk CCD are summarized in Table 1. The main thing to note is the performance is as good as the other family members of Standard silicon and Deep Depletion. Noise is < 2.5e- rms at 50kpix/sec and increases to 4e- rms at 225kpix/sec. Linearity is excellent at < ± 0.2% over signal range of 500e- to 100ke-. Dark current of < 0.2 e-/pixel/hour at -120 ºC is extremely low and as such difficult to measure accurately.

Table 1: *Summary of results of testing the Bulk CCD44-82.*

Parameter	Results (-120 ºC)	Comment
Device	Bulk Silicon Science	
Serial Number	07382-24-01	
Type Number	CCD44-82	Extensively used at ESO
Pixel Size	15µm	
Number of Pixels	2048 x 4096	
Noise (50 kpix/s)	< 2.5 e- rms	Gain of 0.6 e-/ADU
Noise (225 kpix/s)	< 4 e- rms	Gain of 1.6 e-/ADU
Linearity (500e- to 100 ke-)	< ± 0.2%	Photon Transfer Curve method - not fully optimized
Dark Current (e-/pixel/hour)	< 0.2	Limited by extraneous sources and not CCD
Cosmic hit event rate (events/min/cm^2)	3.0	
Vertical CTE	0. 9999991	Measured by Extended Pixel Edge Response (EPER)
Horizontal CTE	0. 999996	

The measured QE (Figure 4) agrees well with that reported by e2v in their test report, but exhibits the typical small discrepancies between ESO and e2v; i.e. ESO reporting a slightly higher QE in the blue and lower QE in the red. The methods used (calibrated diode comparison) by both ESO and e2v to measure the QE requires the gain to be known precisely. It has previously been reported[4] that one has to be careful when using the photon transfer curve method to measure gain. Observed non-linearities in photon transfer curve results in the calculated gain (slope of the photon transfer curve) varying with signal level (Figure 5a). It was recommended in [4] to use binning to improve the accuracy in calculating the gain. As the non-linearity was found to be proportional to the signal level in the image area, by using binning the signal in the image area can be kept small while still exercising the sense node, output amplifier and video chain to reasonable signal levels. For the Bulk CCD measurement, 4x4 binning was used which results in a calculated gain that varies little with signal level (Figure 5b).

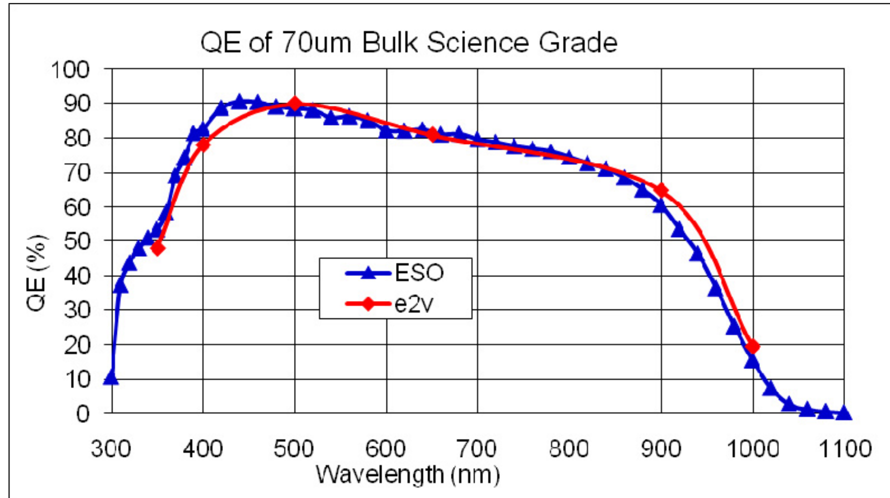


Figure 4: Comparison of the QE of the Bulk CCD44-82 measured by e2v and ESO. Results show good agreement.

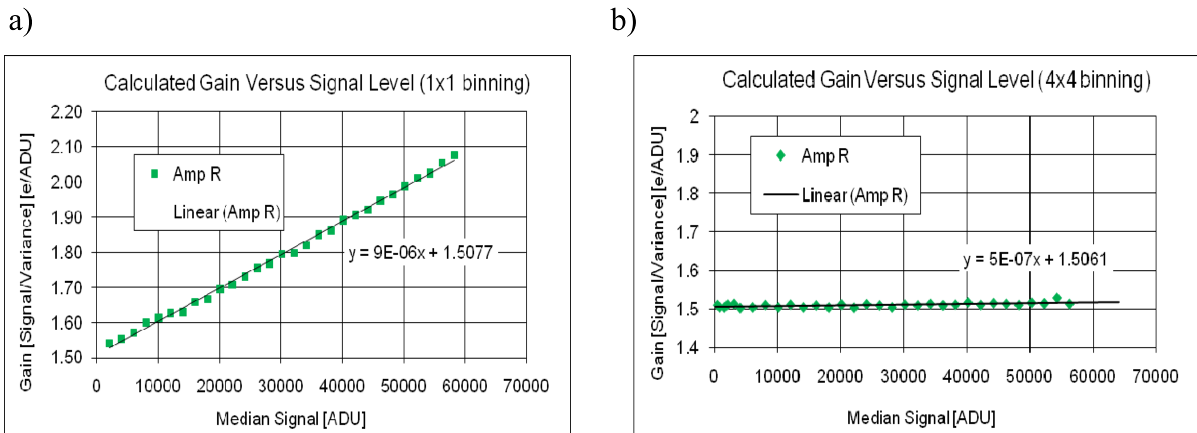


Figure 5: Calculated gain (the slope of photon transfer curve) at a) 1x1 and b) 4x4 binning. Note how the gain calculated using 1x1 binning varies with signal level. With 4x4 binning, the gain is almost constant with signal level and thus can be much more accurately determined. The correct gain is 1.5e/ADU.

The plot (Figure 6) of measured (bandwidth 7nm) Photon Response Non-Uniformity (PRNU) versus wavelength clearly shows the other great advantage of thicker silicon CCDs. At wavelengths > 700nm, the PRNU due to fringing is much less for the 40µm Deep Depletion and 70µm Bulk CCD than the 16µm Standard Silicon CCD. Comparison of flat field images at 900nm (Figure 7) shows how fringing reduces in amplitude and increases in spatial frequency as the silicon thickness increases. In the case of the Bulk CCD (Figure 7c), fringing is hardly noticeable at the illumination bandwidth of 7nm. Also it is observed in Figure 6 that at wavelengths < 400nm, the PRNU of the Bulk CCD is worse than the other silicon devices. Comparison of flat field images at 350nm (Figure 8) shows that the higher PRNU is due to uneven device thinning and less optimal laser annealing. These features are due to the one off manufacturing of these technology demonstrators and not a

fundamental limit. More care in future productions should yield devices with as good blue PRNU as their thinner cousins.

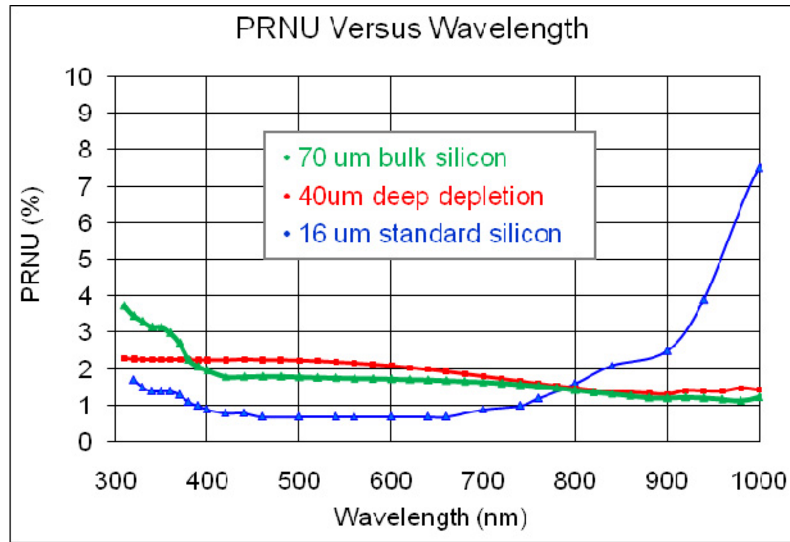


Figure 6: Comparison of the measured PRNU (bandwidth 7nm) of the 70 µm Bulk CCD to that of 16 µm Standard Silicon and 40 µm Deep Depletion CCD44-82.

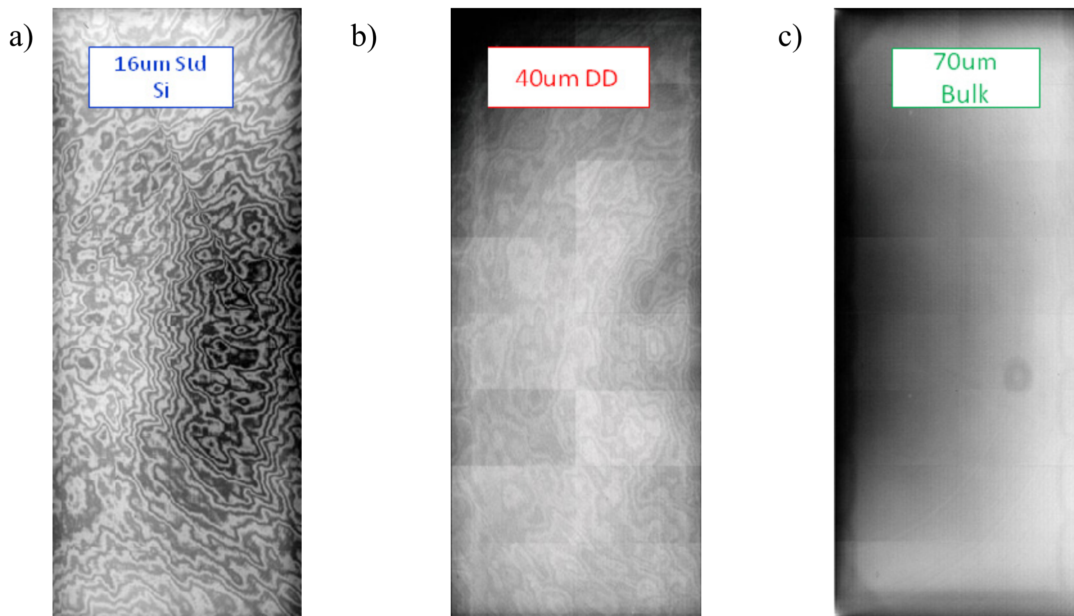


Figure 7: Comparison of flat field images(5 – 95% histogram scaling) taken with a) 16 µm Standard, b) 40 µm Deep Depletion, c) 70 µm Bulk silicon CCDs when illuminated by 900nm (7nm bandwidth) light. Note how fringing reduces in amplitude and increases in spatial frequency as the silicon thickness increases. Fringing is not noticeable in the case of the Bulk CCD at the illuminated bandwidth of 7nm.

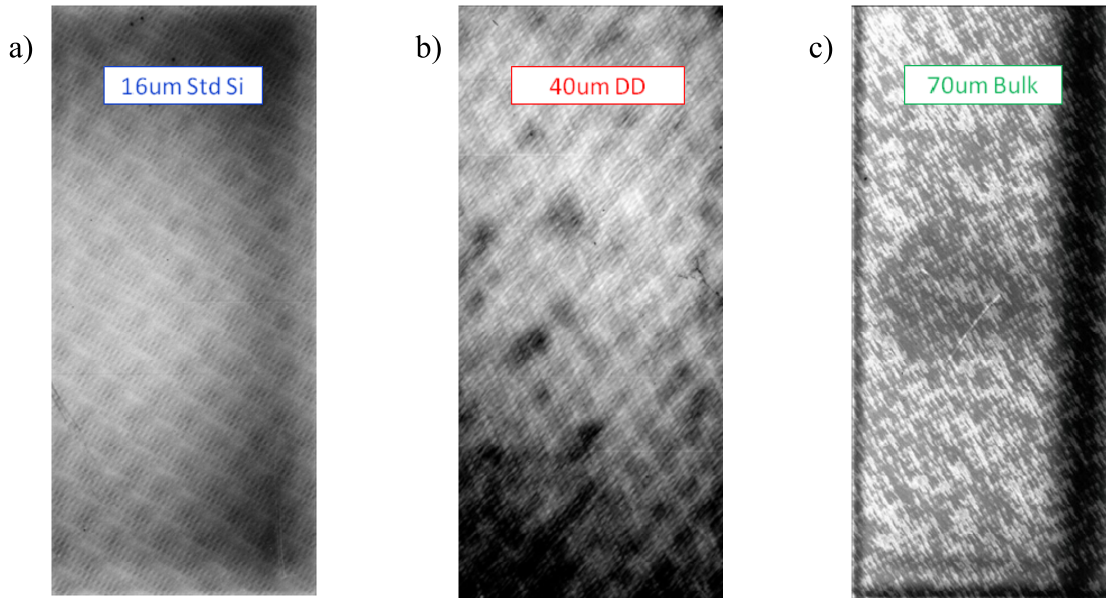


Figure 8: Comparison of flat field images(5 – 95% histogram scaling) taken with a) 16 µm Standard, b) 40 µm Deep Depletion, c) 70 µm Bulk silicon CCDs when illuminated by 350nm (7nm bandwidth) light. At shorter wavelengths (< 400 nm), the PRNU of Bulk CCD is a little worse due to uneven device thinning and less optimal laser annealing.

Cosmetically, at -120ºC, the Bulk CCD is very good (Table 2) with a very low number of dark and hot pixels and two column traps (Figure 9). -120ºC is the typical temperature at which ESO operates the CCD44-82s at its observatories[1].

Table 2: Summary of results of cosmetic testing of the Bulk CCD at -120ºC.

Blemish	Specification	Number
Hot pixel	> 100e-/pixel in one hour Dark	14
Hot Column	> 100 bad pixels in one hour Dark	0
Trap	> 200e-	2
Dark pixel	< 50% response	112
Dark Column	> 100 dark pixels	0

[1] http://www.eso.org/public/astronomy/teles-instr/

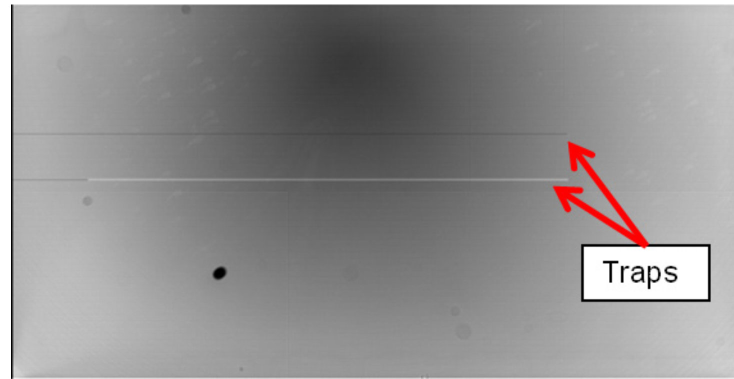


Figure 9: 600 nm (7nm bandwidth) flat field image of bulk CCDs showing the two column traps.

Table 3: *Variation with temperature of the average dark current and the number of hot pixels in a one hour Dark. Note that at < -120ºC, hot pixels are not a problem and the device is of excellent scientific quality. Above -120ºC, the number of hot pixels increase dramatically and start to dominate the average dark current.*

Temperature (ºC)	Average Dark Current (e-/pix/hr)	Number of Hot Pixels (> 100e-/pix/hr)	Comments
-120	0.2	14	
-100	5.5	160500	Hot pixels dominate average dark current
-80	310	661025	

At warmer temperatures (Table 3), the number and intensity of hot pixels increase rapidly. At -120ºC, one hour dark images (Figure 10c) have a sprinkling of warm pixels affecting a mixture of single and multiple pixels and very few hot pixels. At -100ºC (Figure 10b), a large number of hot pixels are visible while at -80ºC, hot pixels are a dominant feature along with trails of bleeding charge. At both -80ºC and -100ºC, hot pixels dominate the calculation of the average dark current.

The hot pixels are believed to be due to impurities in the silicon. This explanation is consistent with the following observations. There is a mixture of single and multiple hot pixels. Impurities are evenly distributed throughout the silicon bulk. Dark current generated by impurities in or close to the potential well will be collected in a single pixel. Impurities closer to the backside and outside the depleted region have farther to travel and have a greater probability to be collected in more than one pixel. The number and intensity of many of the hot pixels increase with the collection phase voltage (Figure 11, and Figure 12). Increasing the collection phase voltage, Vc, increases the strength and extent of the electric field (see Section 3 for more complete discussion) thus drawing more of the electrons into the pixel potential well especially those whose generation site is closer to the backside. Below each image in Figure 11 is a pixel value table middled on an interesting, but not unique hot pixel. Note how this hot pixel evolves with Vc: at Vc of -2V, the hot pixel is barely visible, while at

Vc of 8V, the hot pixel is very bright. This pixel is thought to be close to the backside and in the undepleted region when Vc is -2V, but at the edge of the depleted region at Vc is 2V.

Bulk silicon is much more prone to impurities than previous silicon technologies. Normal epitaxial silicon (on its lower resistivity substrate) benefits from a gettering effect during processing that significantly reduces impurities. Bulk silicon does not have this advantage.

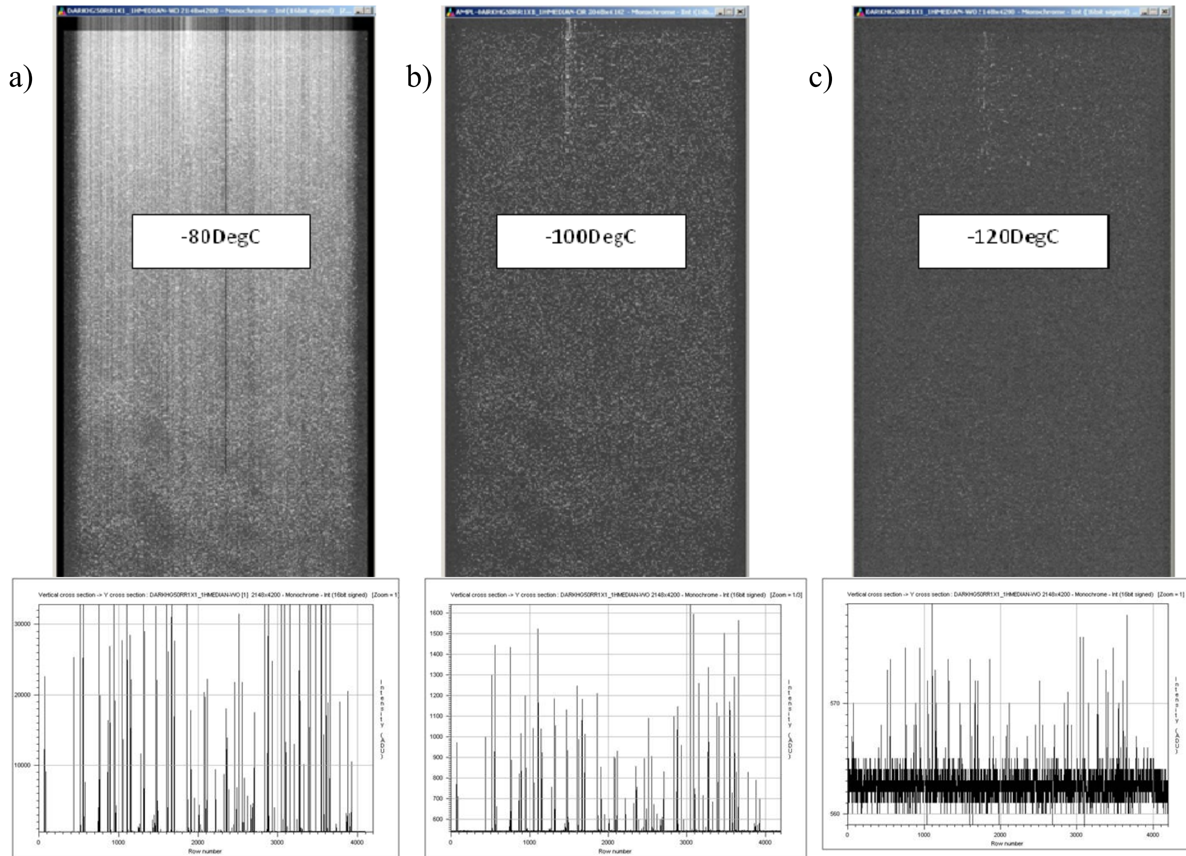
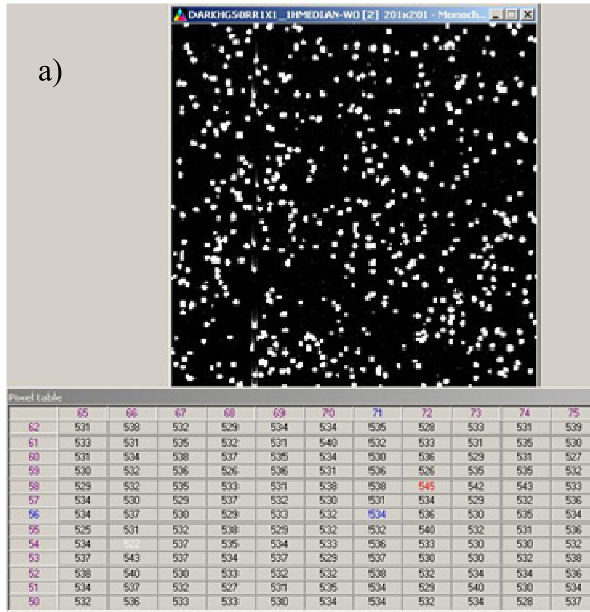
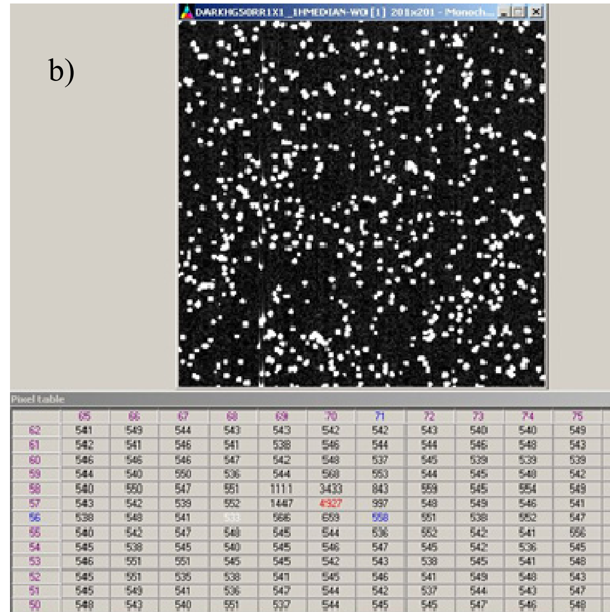


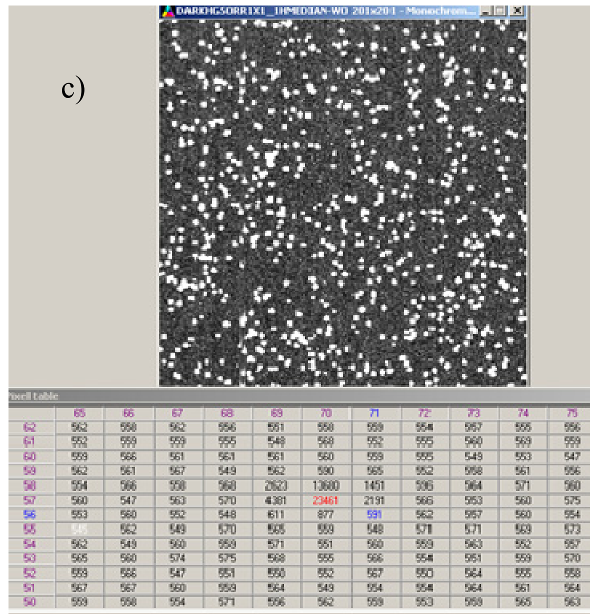
Figure 10: Top: One hour dark images at a) -80ºC, b) -100ºC, and c) -120ºC. At the bottom are column plots of each image at a randomly chosen (x=600 out of 2098) row. Note the very different Y-scaling of these plots. Conversion gain is 1e-/ADU. At -120ºC, only a sprinkling of warm pixels are visible and very few hot pixels. At -100ºC, a large number of hot pixels are visible. At -80ºC, hot pixels are a dominant feature including trails of bleeding charge.



Vc=-2V, Vb=-8V



Vc=2V, Vb=-8V



Vc=8V, Vb=-8V

Figure 11: Subimages of one hour darks at collection phase voltage (Vc) of a) -2V, b) +2V, c) +8V; all with barrier phase (Vb) set at -8V. Careful inspection of the images show the number and intensity of many of the hot pixels increase with the collection phase voltage. Below each image is a pixel value table middled on an interesting, but not unique hot pixel located at [70, 57]. Note how the hot pixel evolves with Vc; at -2V the hot pixel is barely visible, while at 8V, the hot pixel is very bright. Conversion gain is 1e-/ADU.

Table 4: Variation in one hour Dark of the average dark current and the number of hot pixels with the collection phase voltage. Note that the number and intensity of hot pixels increase with collection phase voltage.

Collection Phase Voltage (V)	Barrier Phase Voltage (V)	Average Dark Current [e/pix/hr]	Number of Hot Pixels (> 100e-)
-2	-8	250	538128
2	-8	310	661025
8	-8	350	702139

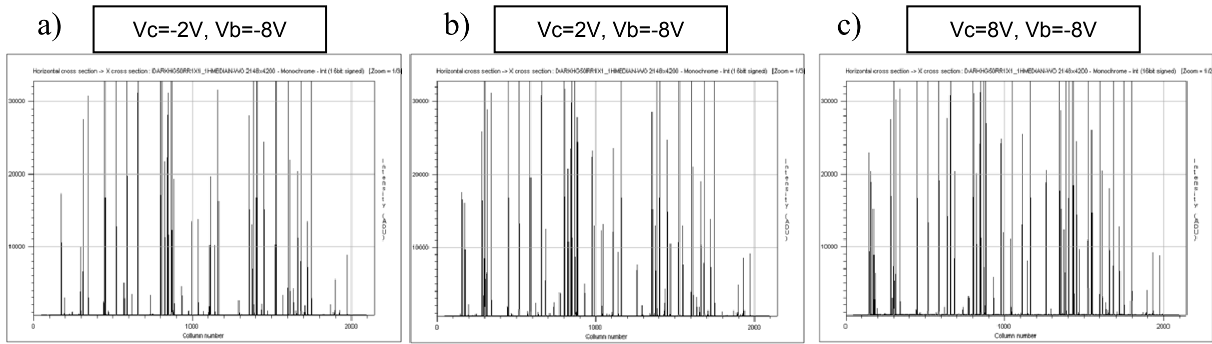


Figure 12: Row plot of randomly chosen column (3200) of one hour Dark at collection phase voltage (Vc) of a) -2V, b) +2V, c) +8V; all with barrier phase (Vb) set at -8V. Note how the number and intensity of many of the hot pixels increase with the collection phase voltage. Conversion gain is 1e-/ADU.

Note that at -120ºC and below, hot pixels and dark current are not an issue and the device has as good performance in this respect as any of the previous silicon technologies.

Careful inspection of the spatial density of hot pixels across the CCD reveals an interesting phenomenon. The pixels around the complete periphery (Figure 13) of the CCD (strip of ~ 70 pixels wide) contain very few if any hot pixels. This effect is currently under investigation at e2v with the hope of applying the benefit more widely.

The effect of cosmic-ray events becomes worse as the device thickness is increased. The thicker the device, the more chance that a cosmic ray will affect more than a single pixel (Figure 14). In 16 µm standard silicon, the cosmic ray event affects mostly single pixels (Figure 14a) and is easily cleaned by image processing. In 40 µm deep depletion silicon, there is a mixture of single and multiple pixel events (Figure 14b). With bulk silicon, there are mostly multiple pixel events (Figure 14c) and cosmic ray events are much more difficult to clean. In addition, the number of cosmic ray events scales with the device thickness. The hit event rate of 70µm Bulk CCD was measured to be ~ 3.0

events/min/cm². This agrees in device thickness ratio (70µm/40µm) when compared to the hit event rate of ~ 1.8 events/min/cm² of the 40µm Deep Depletion CCD.

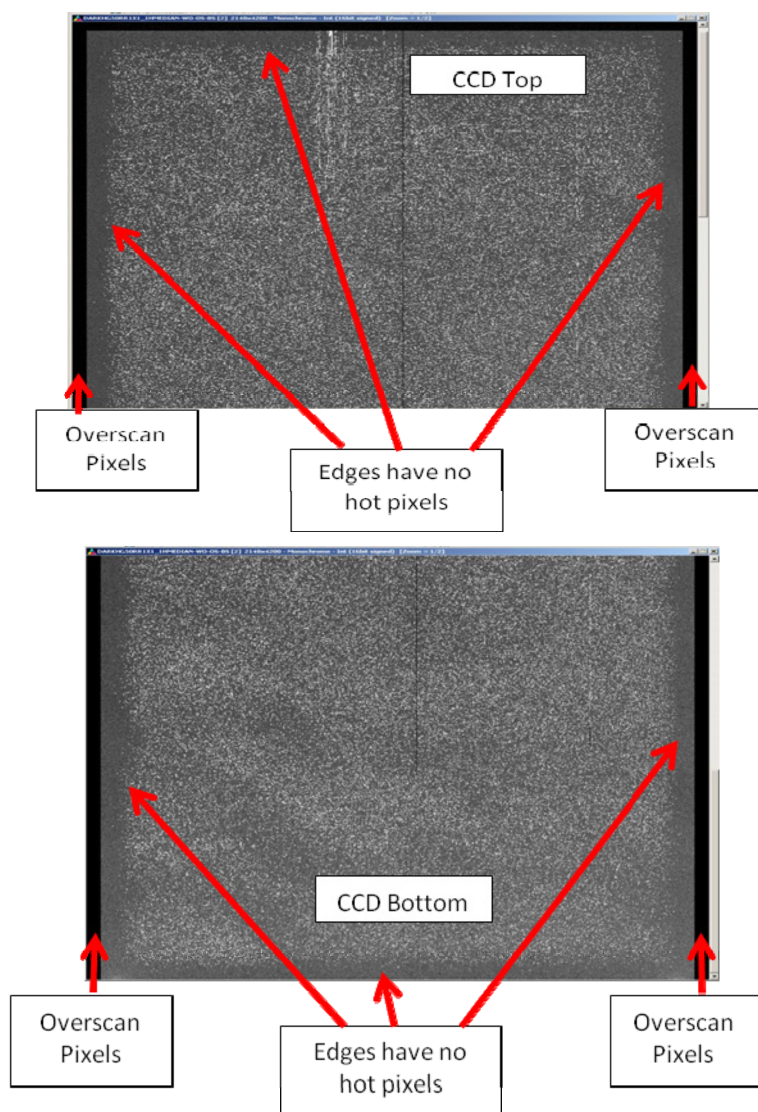


Figure 13: Blown-up top and bottom of one hour dark image at -80ºC. Note the picture frame around the image area where there are very few hot pixels.

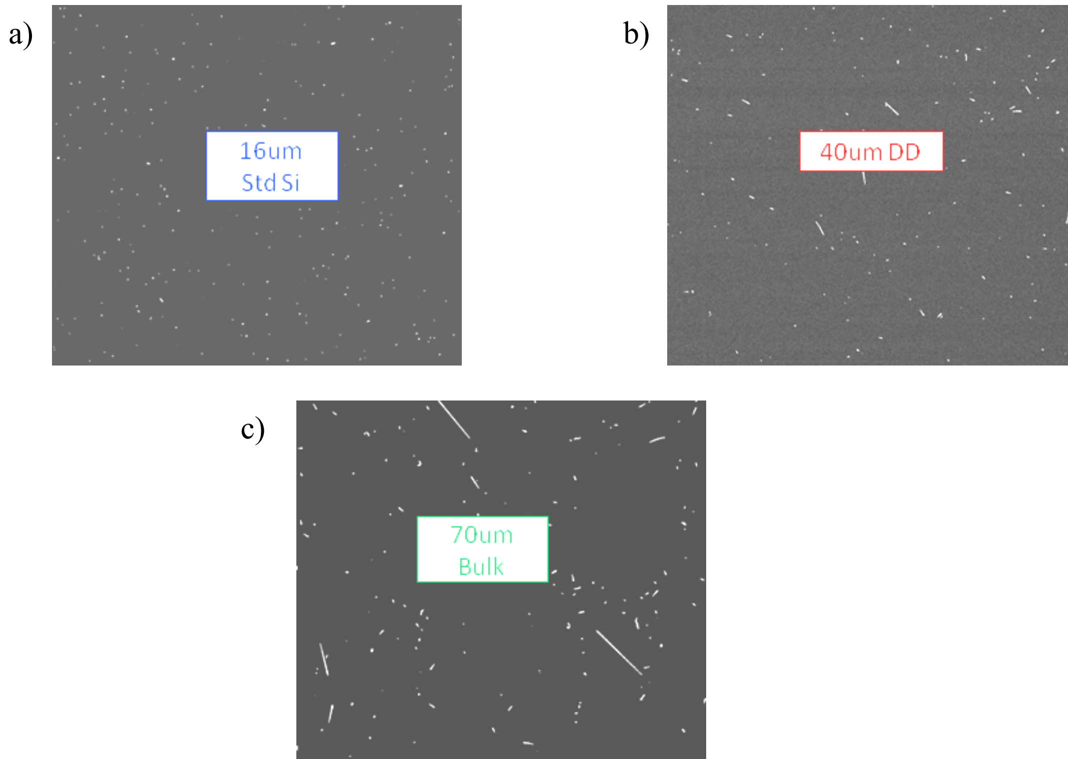


Figure 14: Sub-images of raw one hour darks at -120ºC showing cosmic ray events. Note that for a) 16 µm Standard Silicon most cosmic ray events affect a single pixel, for b) 40 µm Deep Depletion there is a mix of single and multiple pixel events, and for c) 70 µm Bulk CCD most are multiple pixel events.

3. POINT SPREAD FUNCTION (PSF)

The quality of spatial performance, the PSF, depends (Figure 15) on: a) The thickness of the undepleted region (X_{UNDEP}) at the back of the CCD. b) The strength of the electric field to draw the photo-generated electrons into the potential well. The strength of the electric field is proportional to the difference between the collection phase voltage (***Vc***) and the substrate voltage (***Vsub***), and inversely proportional to the device thickness (X_{THICK}). c) The wavelength and depth of penetration of the photon; blue photons are in general absorbed nearer the silicon surface and have farther to travel to reach the potential well, while red photons penetrate on the average deeper into the silicon and have far less to travel to reach the potential well.

PSF can thus be improved by increasing the extent (i.e. reduce the undepleted region at back of CCD) and strength of the electric field. There are three possible ways to achieve this: 1) increase the collection phase voltage (***Vc***), 2) decrease the substrate voltage (***Vsub***), and 3) increase the number of collection phases (2 for 3 phase device or 3 for 4 phase device).

The PSF is measured at ESO by scanning a small light spot into a small sub-region of pixels (Figure 16), the edge of which acts like a virtual knife edge (for further details of technique consult [6]). The test setup (Figure 17) consists of a pin-point projector installed on a XYZ micrometric stage that projects a < 2 µm diffraction-limited spot onto the CCD. The variation of charge in the sub-region

versus scan position is then recorded. The charge in the sub-region is then normalized to the total charge read out on the detector (Figure 18a). A Gaussian fit (Figure 18b) is performed on the derivative (w.r.t. position) of the measured charge and the FWHM determined.

The results of PSF versus wavelength as the collection phase voltages is varied are plotted in Figure 19. The results of the following CCDs are presented: a) e2v 16 µm Standard Silicon CCD44-82, b) e2v 40 µm Deep Depletion CCD44-82, c) MIT/LL[2] 40 µm HiRes[3] CCID-20, and d) e2v 70 µm Bulk CCD44-82. From the results the following observations can be made. As expected, the PSF improves as the collection phase voltage is increased and the PSF is better for longer wavelengths (red photons) than shorter ones (blue photons). For Standard Silicon CCD44-82 at wavelength > 700nm, the measurement of PSF becomes difficult due to fringing, and the PSF flattens out with wavelength and collection phase voltage. The variation with wavelength and collection phase voltage is in general greater for thinner than for thicker devices; the Bulk CCD varies the least with wavelength and collection phase voltage and between wavelengths of 400nm to 700nm is almost flat.

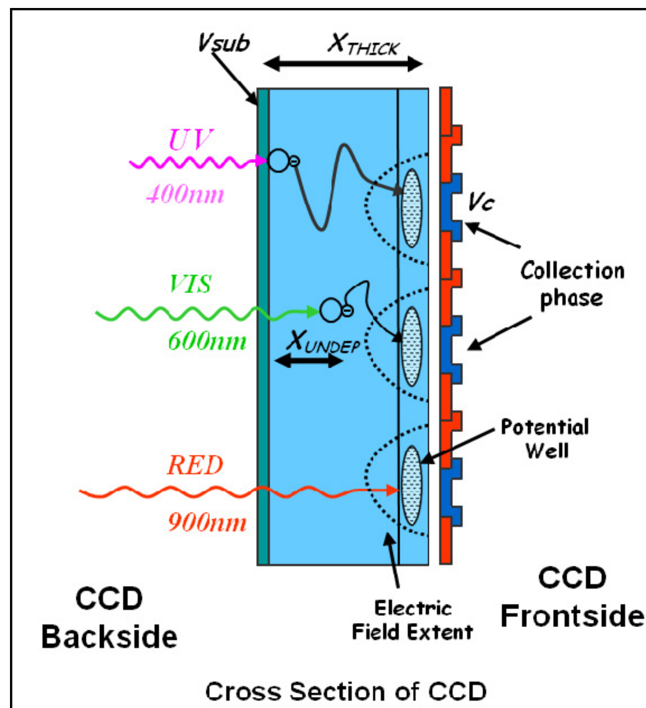


Figure 15: Cross-section of CCD defining terms such as substrate voltage, V_{SUB}, thickness of CCD, X_{THICK}, collection phase voltage, V_C, and undepleted depth, X_{UNDEP}.

2 MIT/LL - MIT Lincoln Laboratory, http://www.ll.mit.edu

3 HiRes – High Resistivity silicon for deep depletion and higher QE in the far red

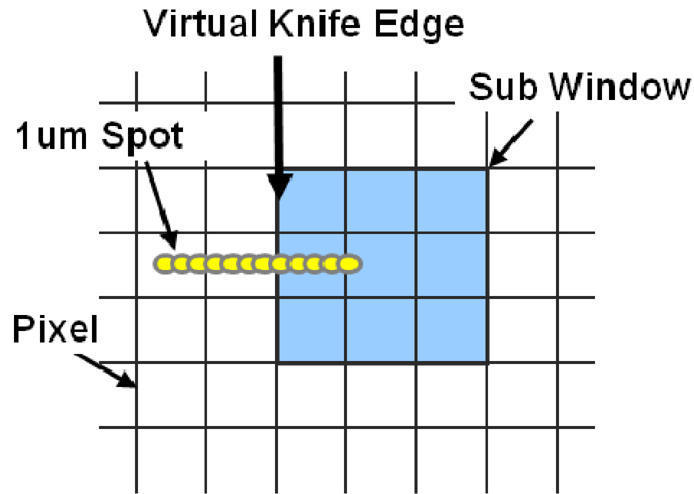


Figure 16: Diagram describing the virtual knife edge technique used at ESO to measure PSF. A 1μm spot is scanned across the CCD into a small sub-window.

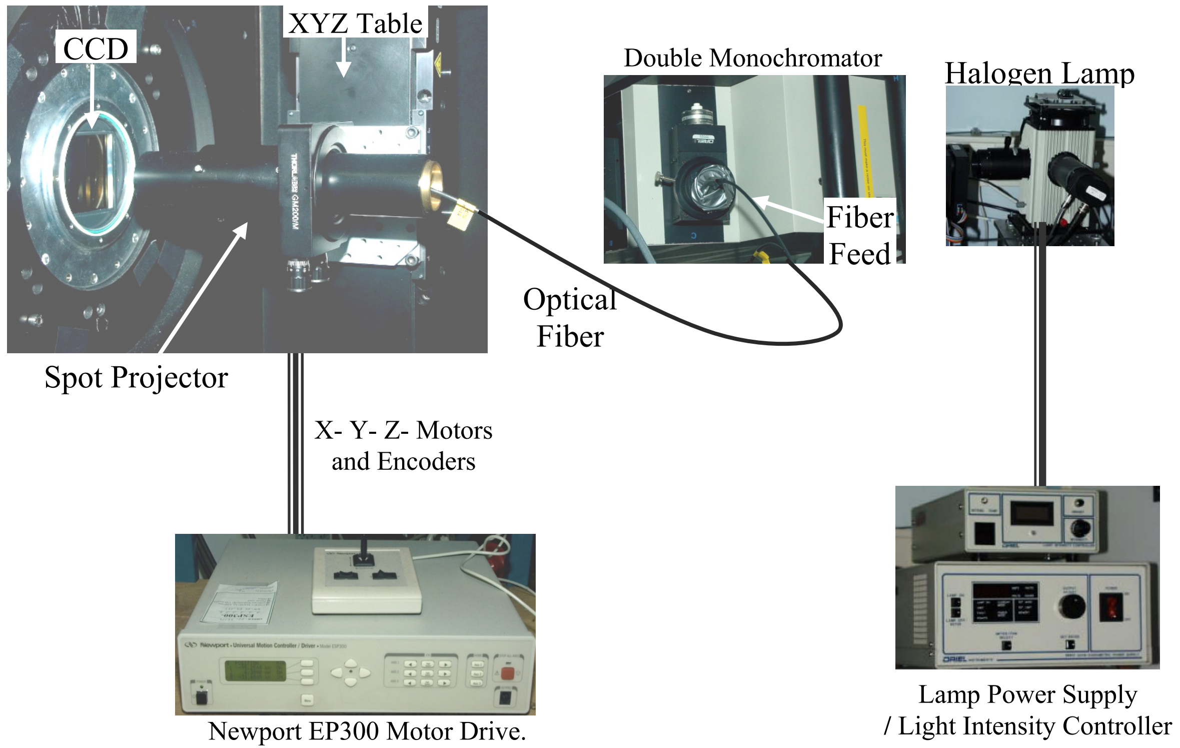


Figure 17: Test Bench setup at ESO for PSF measurements. A spot projector mounted on a XYZ table is scanned across the CCD. A Monochromator feed allows the illumination source to be varied in wavelength (300-1100nm) and bandwidth (2-15nm).

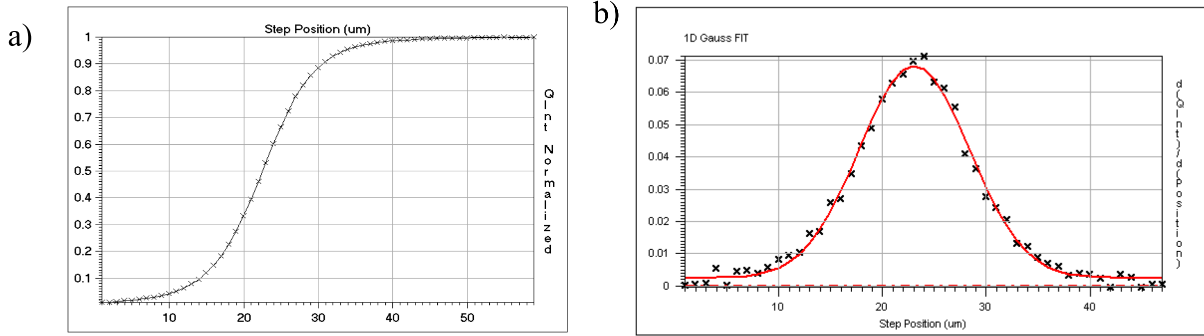
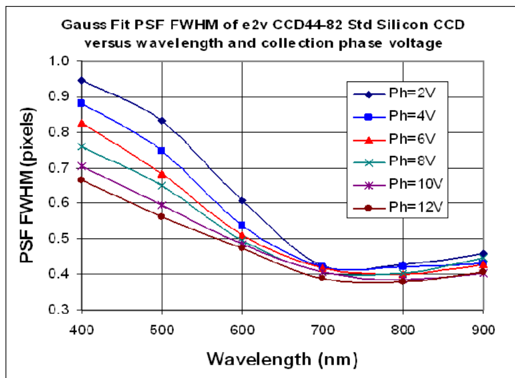
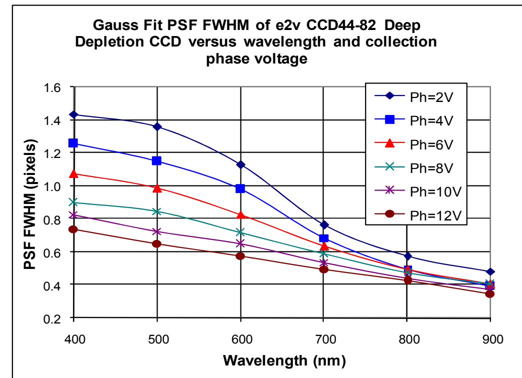


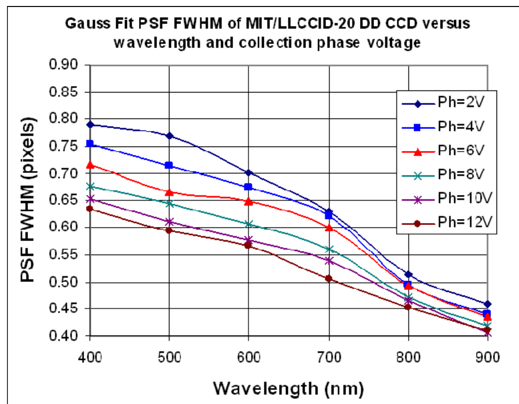
Figure 18: a) Variation of charge (normalized) in sub-region versus scan position. At zero step position, the spot is completely outside the sub-region, while at step position of 60 µm the spot is completed contained inside the sub-region. The charge in the sub-region is normalized to the total charge read out on the detector. b) Derivative of charge in sub-region versus scan position. The smooth (red) curve is a Gaussian fit from which the FWHM of the PSF is calculated.



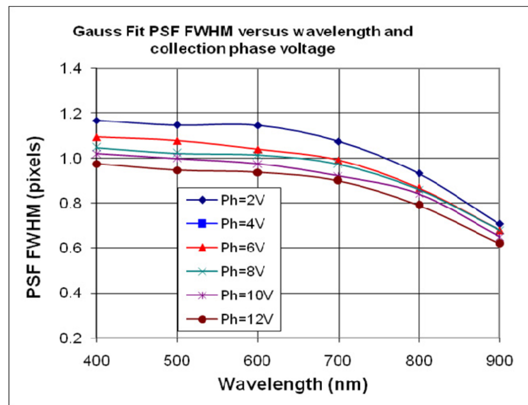
a) e2v 16 µm Standard Silicon CCD44-



b) e2v 40 µm Deep Depletion CCD44-82



c) MIT/LL 40µm HIRES CCID-20



d) e2v 70 µm Bulk Silicon CCD44-82

Figure 19: Plots of PSF versus wavelength for: a) e2v 16 µm Standard Silicon CCD44-82, b) e2v 40 µm Deep Depletion CCD44-82, c) MIT/LL 40 µm HIRES CCID-20, and d) e2v 70 µm Bulk CCD44-82.

4. PHOTON TRANSFER CURVE AND WELL DEPTH

Besides improving the PSF, changing the collection phase voltage also affects the pixel well depth. This section uses the photon transfer curve technique[8] to measure and investigate this variation. The high output amplifier responsitivities of > 6 µV/e- of modern low noise scientific CCDs makes it impossible to exercise the output amplifier to signal levels large enough to measure pixel full well. The CCD44-82, fortunately, has a capability[4] to reduce the output amplifier responsitivity to 1.5 µV/e- by increasing the bias voltage on one, OG2, of the two output gates, and thus allow full well to be measured.

The following read out method was used to measure full well. The CCD was first wiped then a quarter of the CCD exposed to a uniform flat field. At the end of the exposure, the collected charge was toggled between two collection phases while the third one acted as a barrier phase to contain the charge within the image area pixel. The toggled phases were alternatively driven into and out of inversion to promote hole recombination at the surface with any charge that interacts with the Si-SiO2 interface. The integration time was varied from low signal level up until either bloomed or surface full well was reached. The process was repeated for each collection phase voltage (Vc). The photon transfer curve (mean unbiased signal versus variance) was then plotted. Full well was determined by noting where the photon transfer curve significantly deviates from linearity.

Plots of photon transfer curve (Figure 20) and full well (Figure 21) versus collection phase voltage of the e2v CCD44-82 16 µm Standard Silicon CCD show text book behavior. Bloomed full well (BFW) occurs at Vc < 2.5V while at Vc > 2.5V, surface full well (SFW) occurs. At Vc of ~ 2.5V, bloomed full well is equal to surface full well (BFW=SFW) and an optimum well depth of 325ke- is calculated.

The photon transfer curve plots (Figure 22) of the e2v CCD44-82 40 µm Deep Depletion CCD on the other hand are not as well behaved as dips [highlighted in plots b) and c)] appears in the curves of Vc between 2V and 4V. At signal levels > 14kADU, the curves deviate from linearity as expected (due to blooming), however, as the signal levels increase further the variance unexpectedly increases (improves). At a Vc of 6V, there is no "dip" in the variance and the images look good (by visual inspection) up until the point of significantly deviation from linearity. Observing this behavior, the conclusion is that optimum full well occurs at a Vc of 6V at which a well depth of 180ke- (Figure 23) is calculated.

The photon transfer curve plots (Figure 24) of the e2v CCD44-82 70 µm bulk CCD has the same unexpected "dip" behavior as for the Deep Depletion CCD (Figure 22), but more pronounced and starting at a lower Vc of < 0V and continuing till a Vc of 6V (same value as the Deep Depletion CCD). Looking at the images, one observes that the degradation of the variance is due to blooming and the recovery (increase) in the variance is brought about by less blooming. The conclusion is thus the same as for the Deep Depletion CCD, the optimum full well occurs at a Vc of 6V at which a well depth of 220ke- (Figure 25) is calculated.

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[4] CCD44-82 data sheet http://www.e2v.com/assets/media/files/documents/imaging-space-and-scientific-sensors/a1a-100027_7_v1.pdf

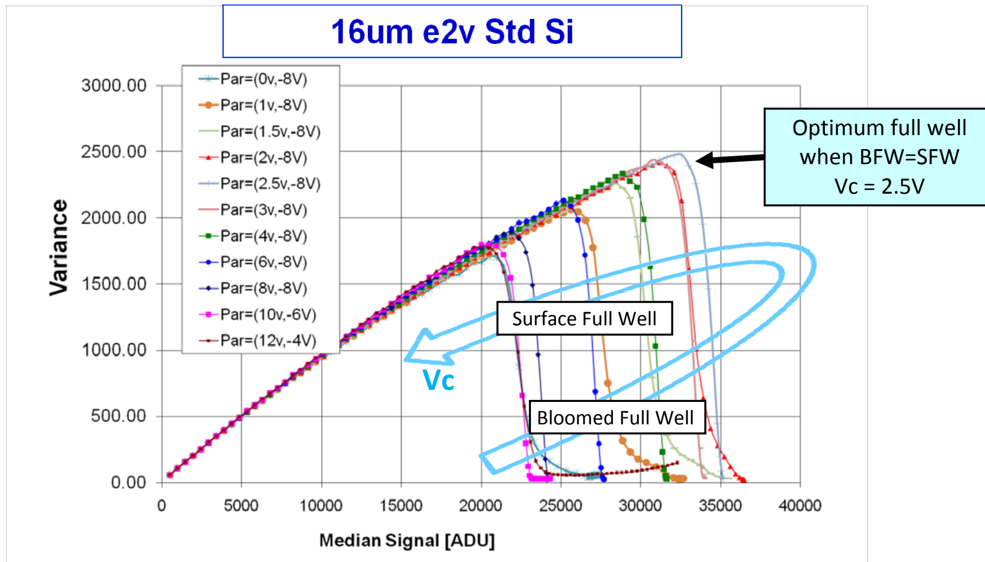

Figure 20: Photon transfer curve plots of e2v CCD44-82 16 µm Standard Silicon CCDs as image area collection (Vc) and barrier phase (Vb) voltages [Par=(Vc,Vb)] are varied. Gain is ~ 11 e-/ADU. The family of curves is well behaved and as described in the text books. Full well can be determined by observing where the curves significantly vary from linearity. At Vc < 2.5V, bloomed full well, (BFW) occurs. At Vc > 2.5V, surface full well (SFW) occurs. At Vc ~ 2.5V, bloomed full well is equal to surface full well (BFW=SFW).

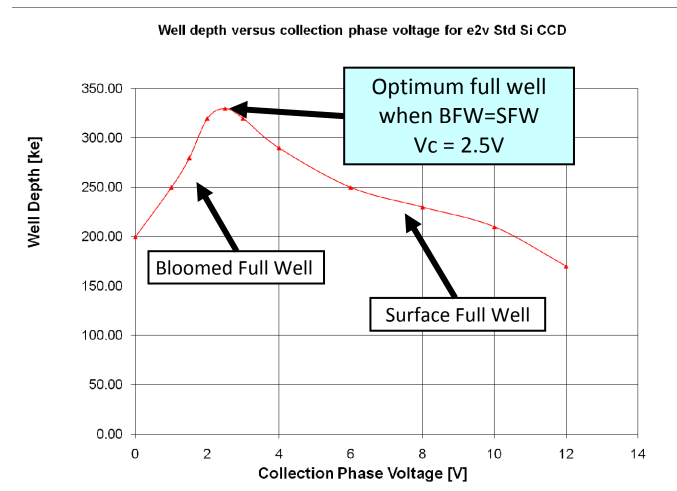

Figure 21: Plot of full well versus collection (Vc) phase voltages of e2v CCD44-82 16 µm Standard Silicon CCDs determined by calculating where the photon transfer curve (Figure 20) significantly deviates from linearity. Optimum full well of 325ke- occurs at a Vc of 2.5V.

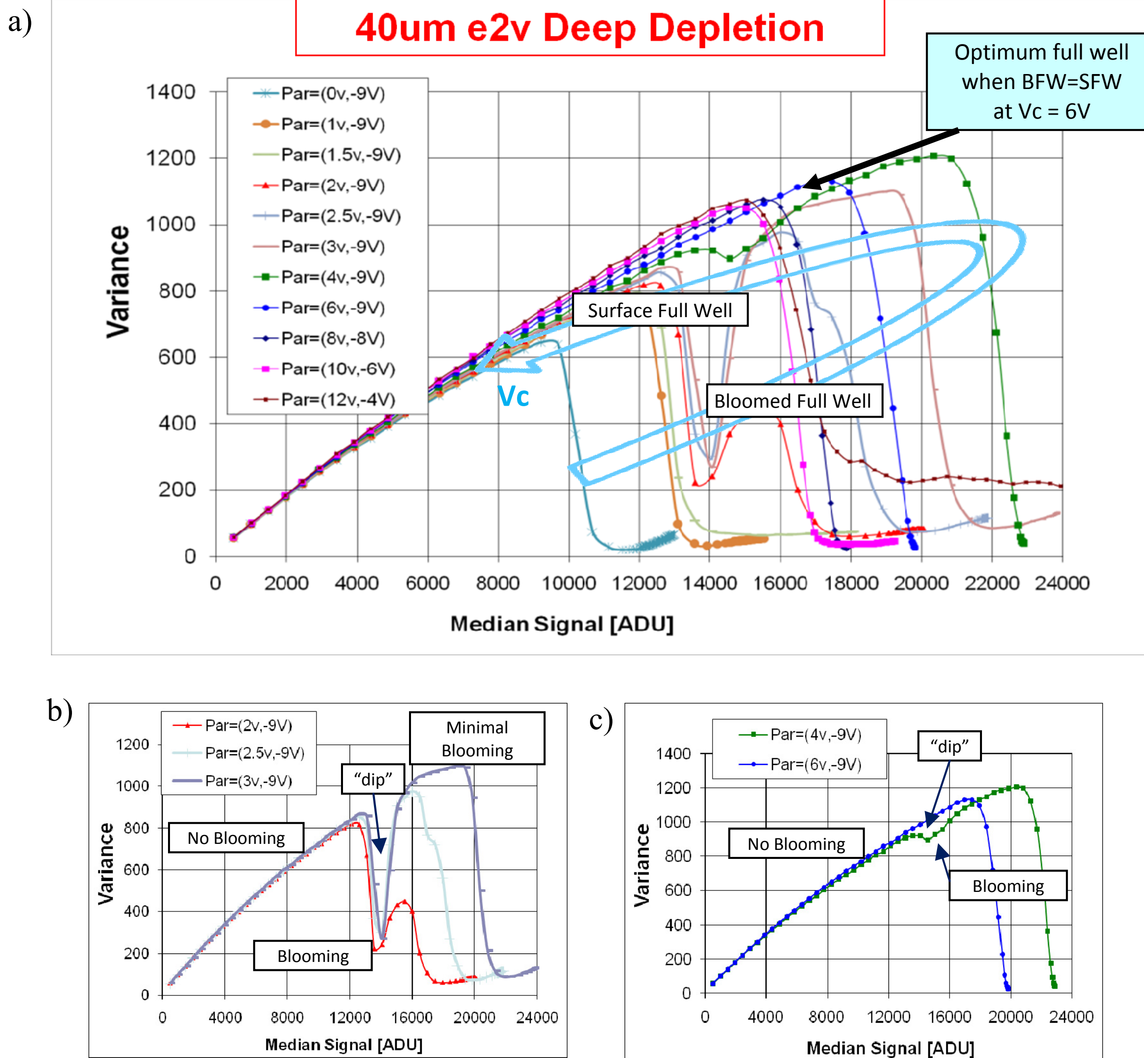

Figure 22: Photon transfer curve plots of e2v CCD44-82 40 µm Deep Depletion CCD as image area collection (Vc) and barrier phase (Vb) voltages [Par=(Vc,Vb)] are varied. Gain is ~ 11 e-/ADU. The family of curves is not as well behaved as that of Figure 20 as a "dip" [highlighted in plots b) and c)] appears in the curves of Vc between 2V and 4V. At signal levels of >14kADU, the curves deviate from linearity as expected (due to blooming), however, as the signal levels increases further the variance unexpectedly increases. At Vc of 6V, there is no "dip" in the variance and the images look good up until significant non-linearity occurs. Observing this behavior, the conclusion is that optimum full well occurs at Vc=6V.

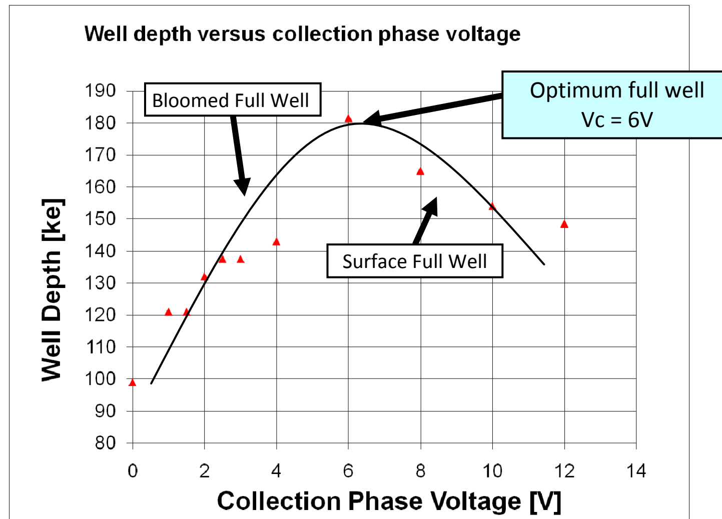

Figure 23: Plot of full well versus collection (Vc) phase voltages of e2v CCD44-82 40 µm Deep Depletion CCD determined by calculating where the photon transfer curve (Figure 22) significantly deviates from linearity. Optimum full well of 180ke- occurs at a Vc of 6V.

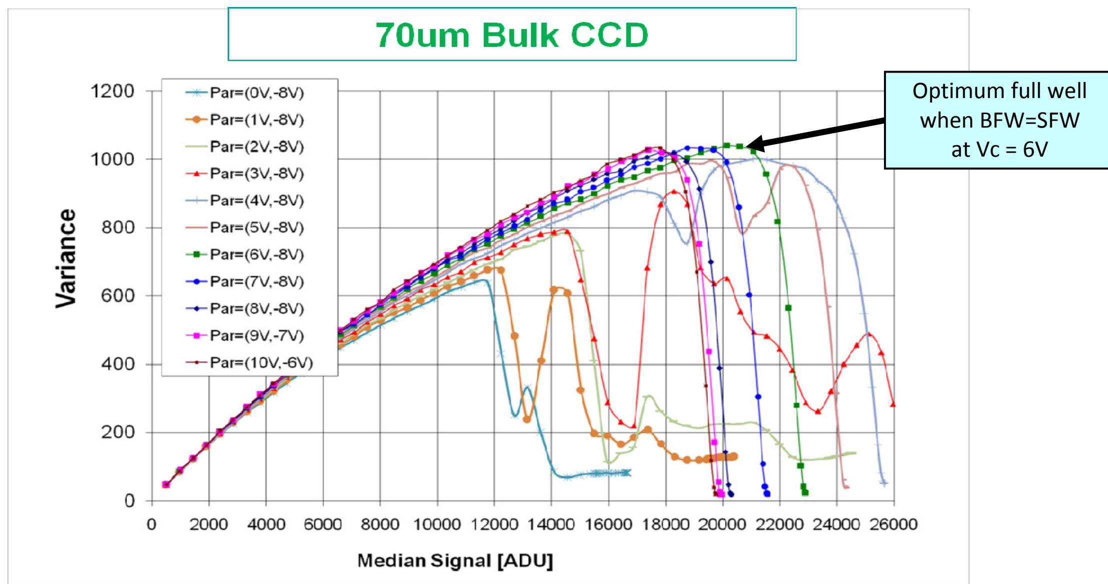

Figure 24: Photon transfer curve plots of the e2v CCD44-82 70 µm bulk CCD as image area collection (Vc) and barrier phase (Vb) voltages [Par=(Vc,Vb)] are varied. Gain is ~ 11 e-/ADU. Note the same unexpected "dip" behavior as for the Deep Depletion CCD (Figure 22), but more pronounced and starting at a lower Vc of < 0V and continuing till a Vc of 6V (same value as the Deep Depletion CCD). Looking at the images, one observes that the degradation of the variance is due to blooming and the recovery in the variance is brought about by less blooming. The conclusion is thus the same as for the Deep Depletion CCD, the optimum full well occurs at Vc=6V.

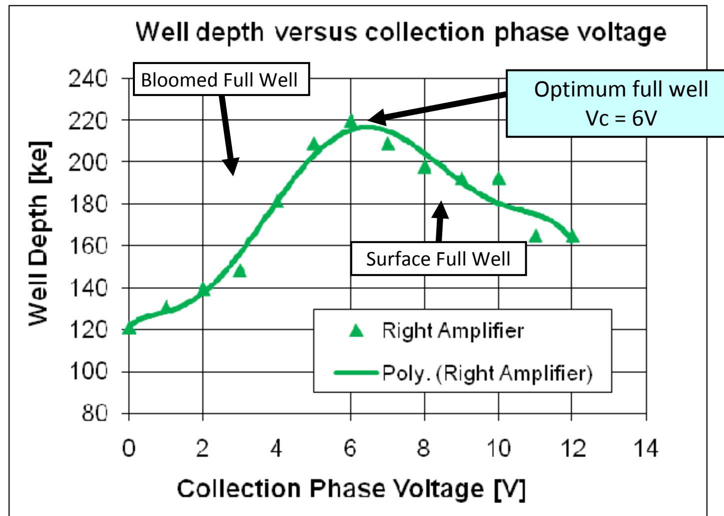

Figure 25: Plot of full well versus collection (Vc) phase voltages of e2v CCD44-82 70 µm bulk CCD determined by calculating where the photon transfer curve (Figure 24) significantly deviates from linearity. Optimum full well of 220ke- occurs at a Vc of 6V.

5. SUMMARY/CONCLUSION

The performance of the Bulk silicon CCD44-82 at -120DegC with respect to noise, gain, linearity, cosmetic, dark current, and CTE is as good as previous e2v CCD44-82 CCDs. The Bulk CCD delivers better QE in the "red" and much less fringing. For performance parameters that depend on knowing the gain accurately, care must be taken when using the photon transfer curve to calculate gain and binning of 4x4 is recommended. Below -120DegC, hot pixels are not a problem. In thicker devices, cosmic rays events affect multiple pixels and their impact needs to be carefully considered.

With a PSF of ~ 1 pixel, the bulk CCD is very suitable for not too demanding optical designs. PSF can be improved by increasing collection phase voltage or running at a lower active substrate voltage. When increasing the collection phase voltage, one has to consider the trade with well depth.

As CCDs are made from higher resistivity silicon, the photon transfer curve becomes more interesting and does not agree fully with the explanation in the text books[8].

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