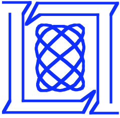

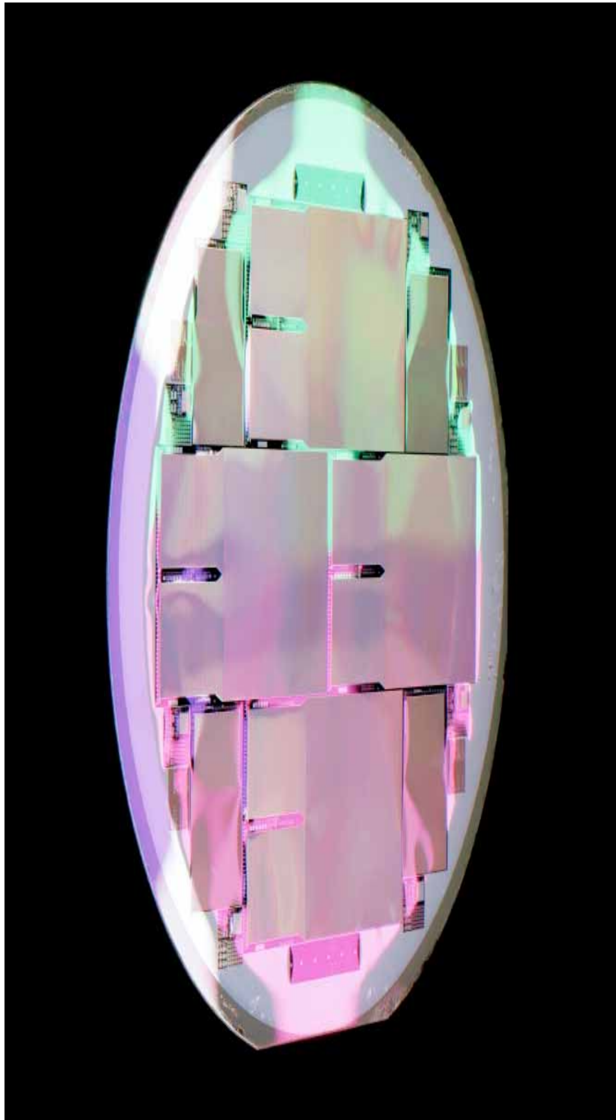

Advanced Imager Technology Development at MIT Lincoln Laboratory

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Barry E. Burke, James Gregory, Robert K. Reich
MIT Lincoln Laboratory

Detectors for Astronomy, ESO Garching
12-16 October 2009

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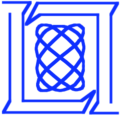
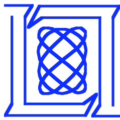


Outline

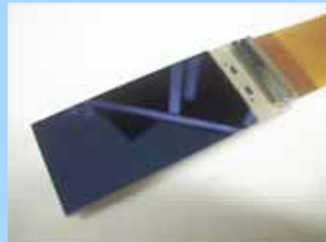
- Overview of MIT-LL X-ray, visible to NIR imaging technology
  - Tiled CCD Imagers for astronomy
  - Devices for adaptive optics
  - Back-illumination processes
- Next-generation technologies
  - Stitched large-format, small-pixel CCDs
  - Four-side abuttable CCD and 3-D CMOS image sensors
- Summary



Imaging Devices at MIT Lincoln Laboratory

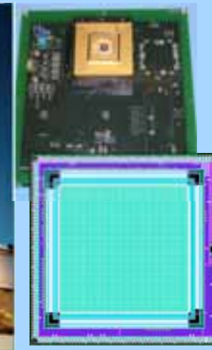
Program Areas

Space- and Ground-based Surveillance and Scientific Imagers



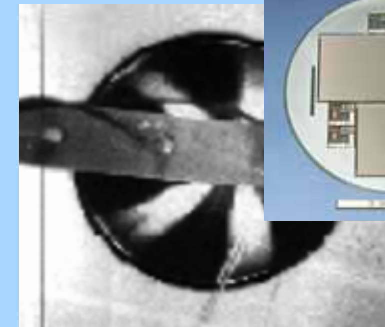
- Curved CCDs
- Orthogonal Transfer Arrays
- Large-format, small-pixel imagers

Silicon Photon Counting Arrays



- High-fill-factor APDs
- CMOS ROIC for photon counting
- Single-electron sensitive readout

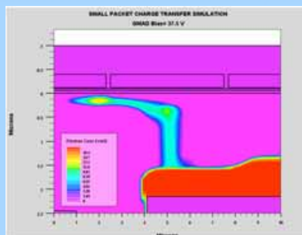
High-Speed Imaging



- High-speed camera electronics
- CMOS x-ray sensor
- Multi-sample CCD

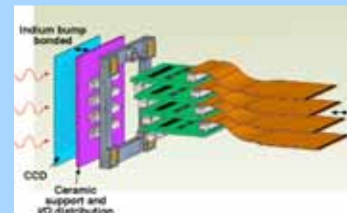
Technology Elements

Detector Design

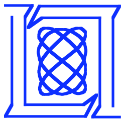


Silicon Detector Process Development

Advanced Packaging

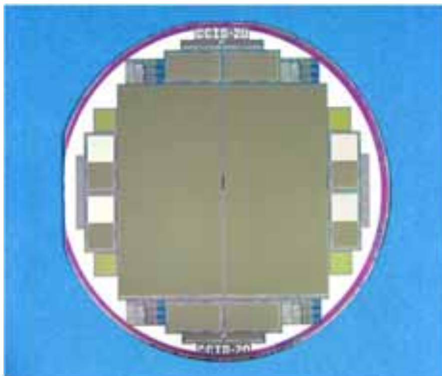


Electronics

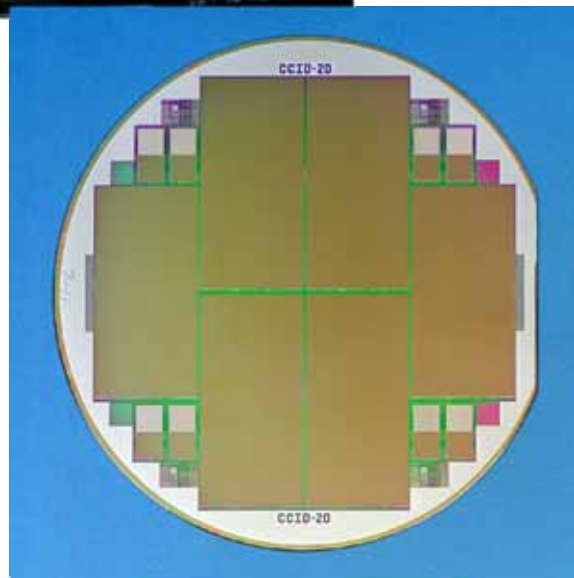


Microelectronics Facility Upgrade to 200-mm Silicon Wafer Size

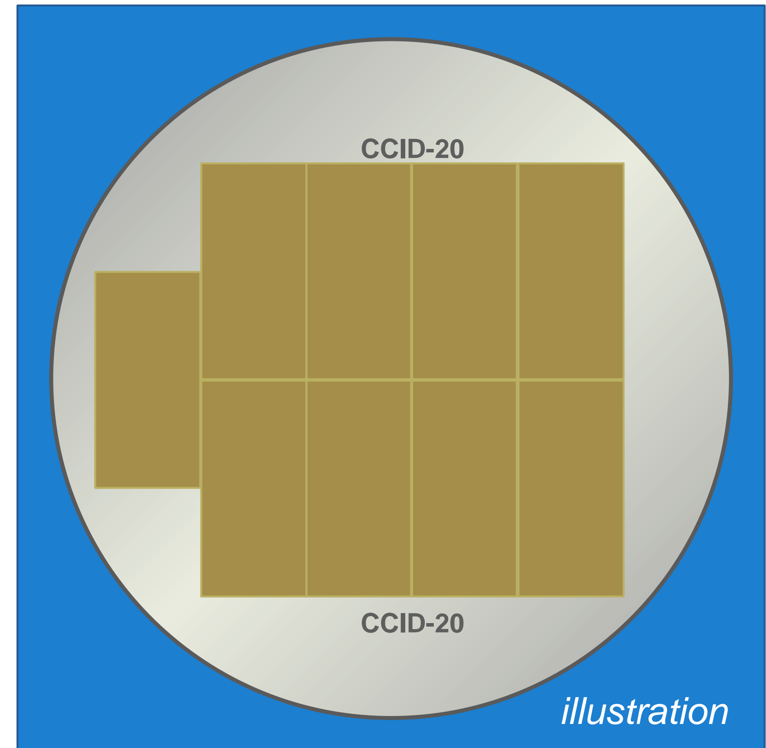
- **Three-year capability upgrade in progress**
  - **First 200-mm device lots beginning Feb. 2011**
- **Nine CCID-20s on a 200-mm wafer**
  - **15-µm pixel, 2K x 4K, 32mm x 63mm**



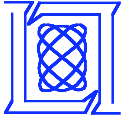
100-mm wafer
Two devices (2K x 4K)



150-mm wafer
Six devices

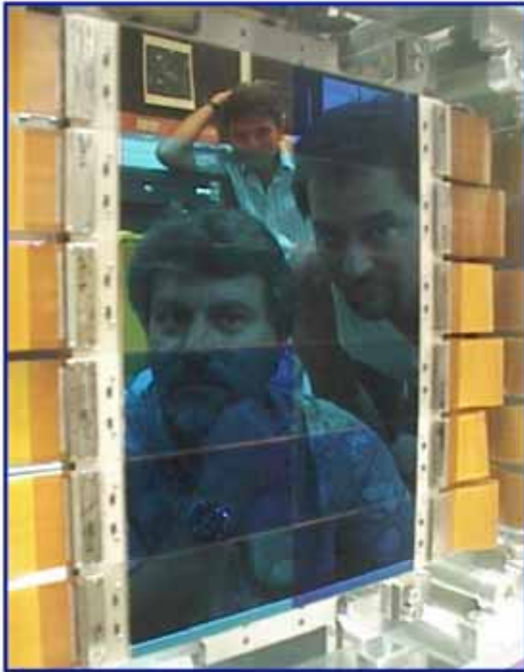


200-mm wafer
Nine devices



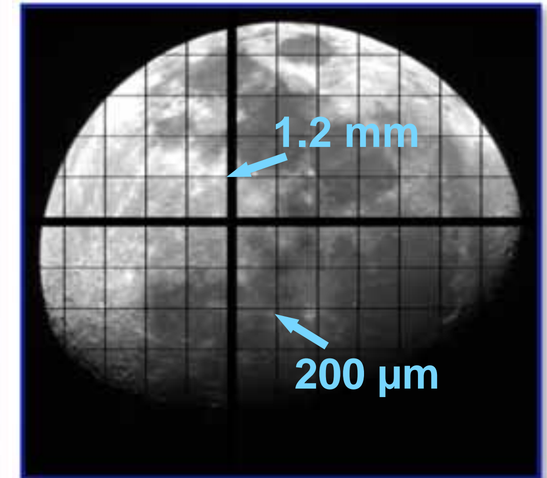
Tiled CCD Imagers for Astronomy

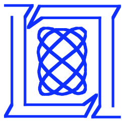
12-CCD UH/CFHT FPA
100Mpix



60 Orthogonal-Transfer CCDs
Pan-STARRs (3° WFOV)
1.36 Gpixels

Image from First Light
(August 2007)





Lincoln Laboratory High-Speed CCDs for Adaptive Optics

1985 | 1990 | 1995 | 2000 | 2005 | 2010

First AO devices

64×64, 4 ports

Electronic shutter

128×128, 16 ports

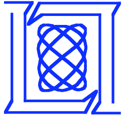
CCD and camera electronics

CCD for curvature wavefront sensing

160×160, 20 ports; pJFET sense amplifier

256×256, 32/64 ports (in design)

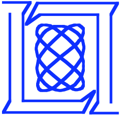
Polar-coordinate imager (in design)



Performance of pJFET-based Output Circuit

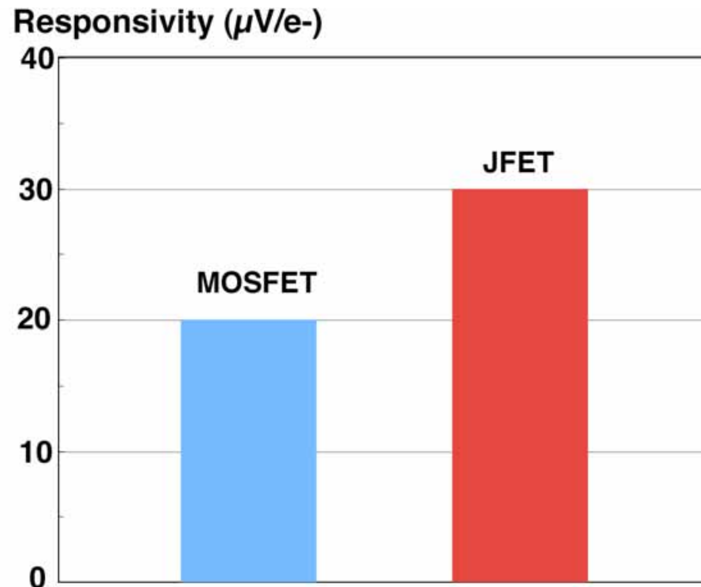
10
Single-stage nMOSFET
Two-stage nMOSFET
pJFET
1
0.1
0.01
0.1
1.0
10
Amplifier read noise (rms electrons)
Output Data Rate (MHz)

Noise: pJFET vs. nMOSFET

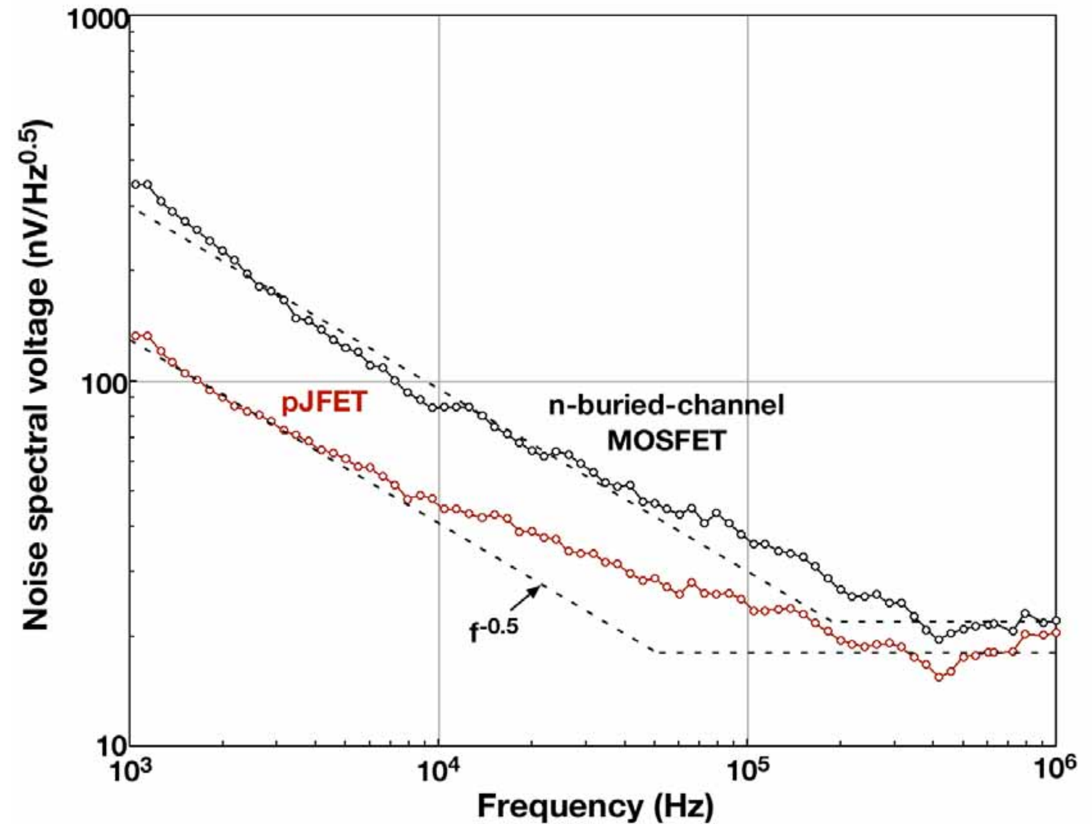


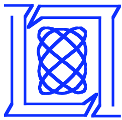
Output Circuit Comparison

Sense-node capacitance is lower (⇒higher responsivity) for JFET than MOSFET

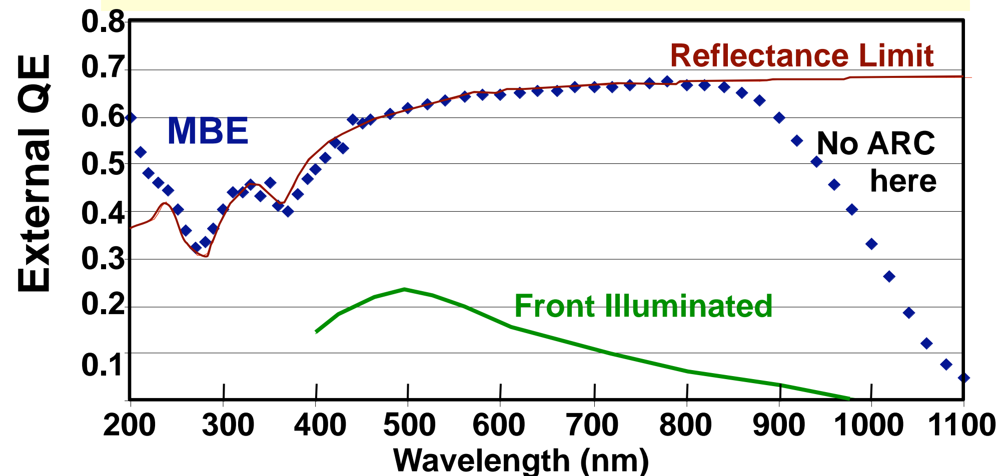


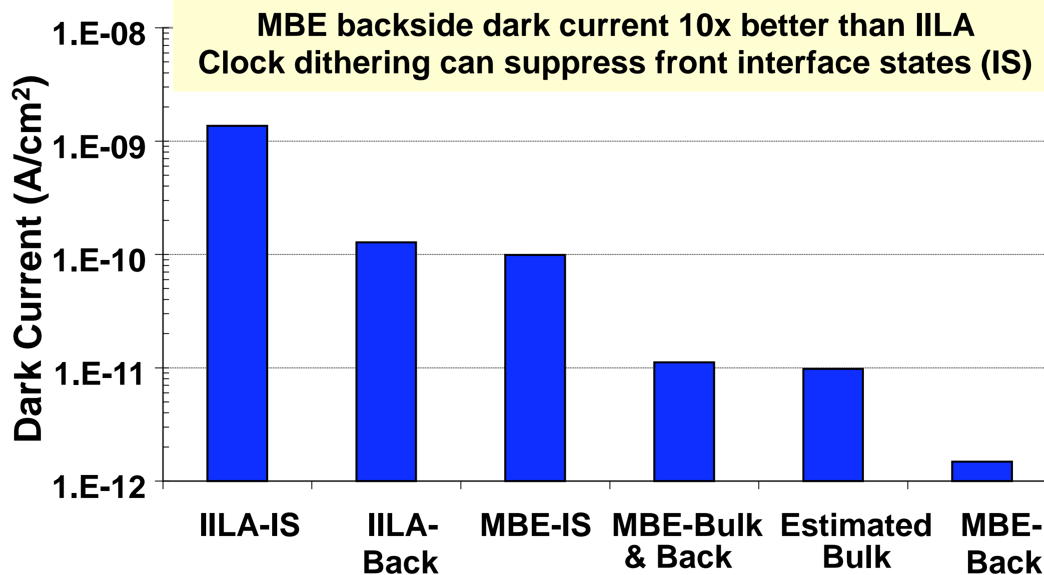
Noise spectral voltage is lower for JFET than MOSFET





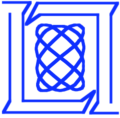
Back Illumination Processes MBE and Laser Anneal (IILA)





Room Temperature (20°C) Result
60-sec Integration Time
Wafer-level Image
of Buckman Tavern

Vignetting from test setup



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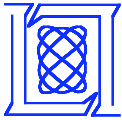
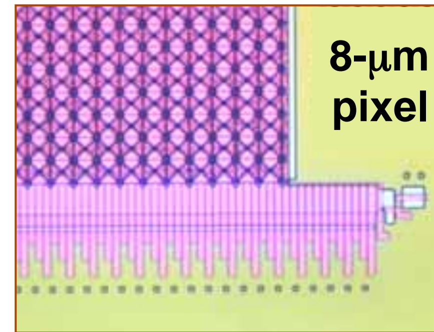
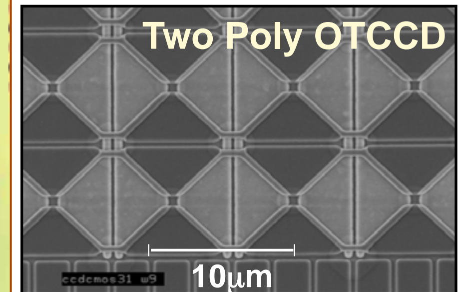
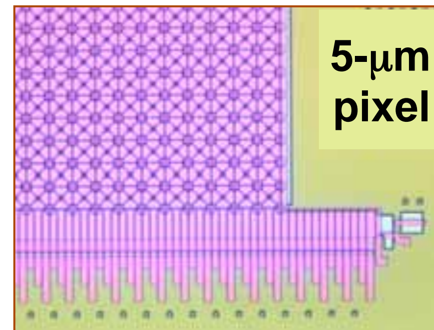


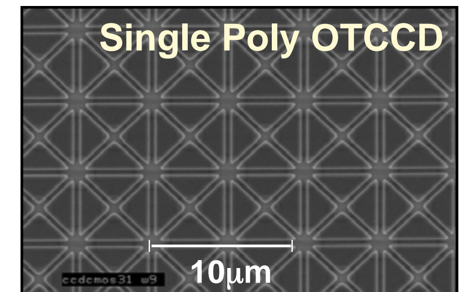
Deeply Scaled CCD Process Technology

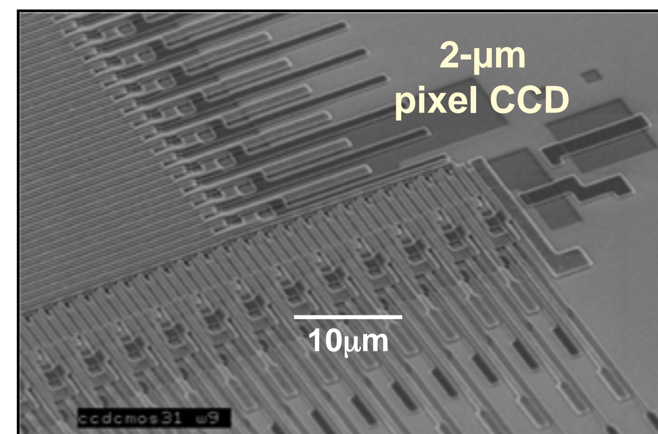
- Small pixels, low-voltage, CMOS-compatible operation
- Demonstrated small-array CCDs
  - Simplified single and two poly fabrication
  - Reduced pixel dimension (8-, 5-, 2-µm)
  - ~150,000 e- well capacity for 8-µm pixel at 3V
- Current efforts: Apply to large area devices
  - Deep ultraviolet photolithography for submicron features (pixel sizes to 2 µm)
  - Stitching for large format imagers

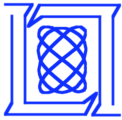












Large-Format, Modular CCD Imagers

- Example: 3K x 3K OTCCD image sensor with 8µm x 8µm pixels
- Pixels with submicron dimensions require high-resolution (248-nm) patterning
  - Lithography field size is smaller than device size
- Design is fractured into functional blocks onto a multi-field reticle and precisely stitched back together on wafer

Design Concept → Layout Fractured Functional Blocks → Multi-field Reticle → Reassembled Design on Wafer

Frame Store (FS)
3072 × 1536,
8.0(H) × 7.5(V)

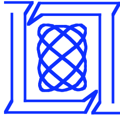
Imaging Array (IA)
3072 × 3072,
8.0 µm × 8.0 µm pixels

50 mm

26 mm

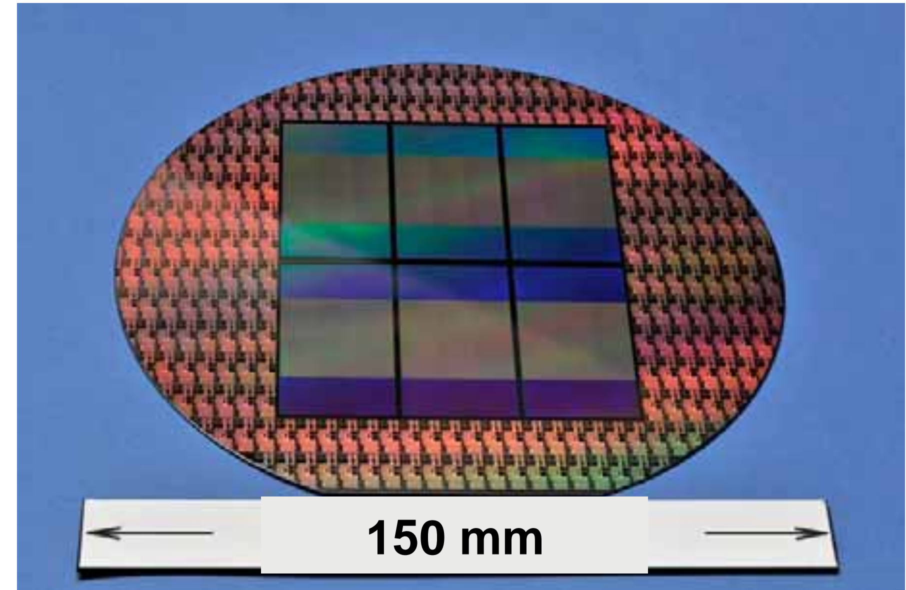
22 mm

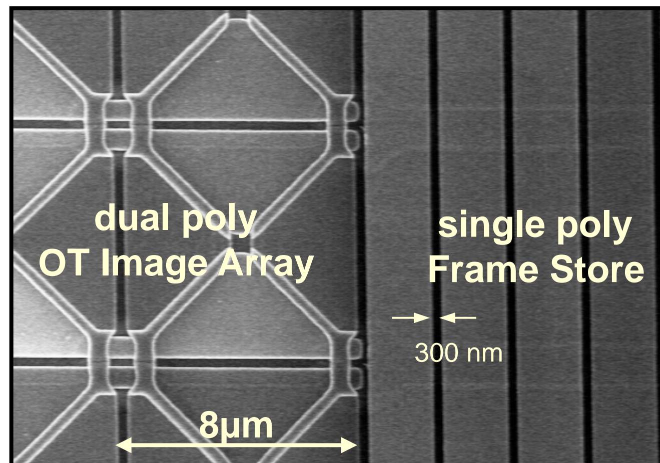
150 mm



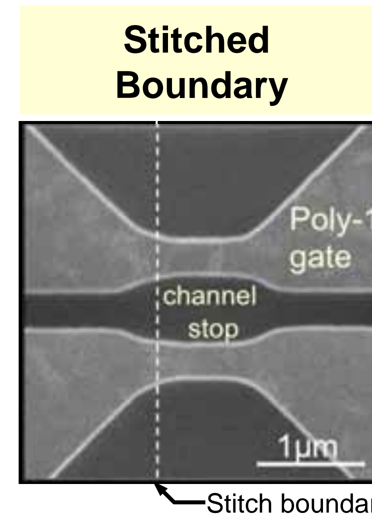
Completed 3K x 3K OTCCD Devices

- Large-area devices (26 mm x 50 mm) fabricated with low-voltage CCD technology
- Stitching methods achieve 35nm (3σ) precision with 8-μm pixel active devices
- Device test results expected in Dec. 2009
- Process technology will be migrated to 200-mm substrates

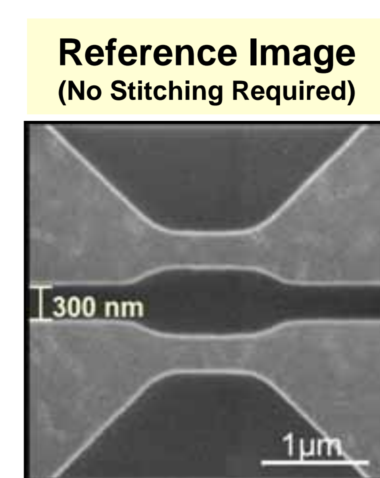


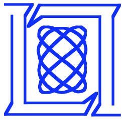


Stitched Boundary



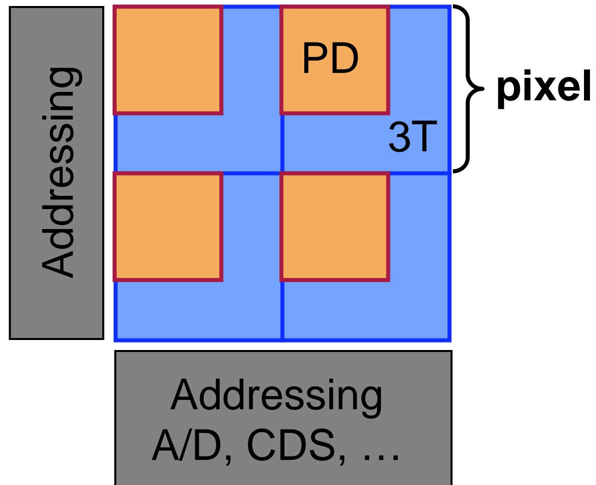
Reference Image
(No Stitching Required)



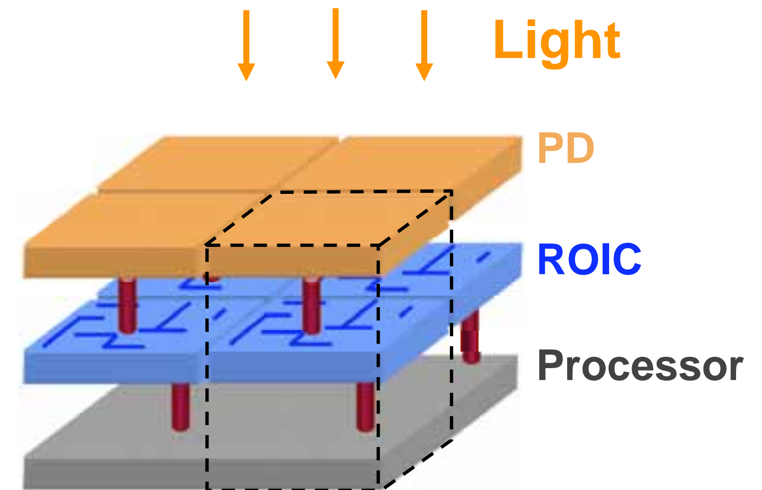


Four-Side Abuttable 3-D CMOS Image Sensor Development

Conventional Monolithic CMOS Image Sensor

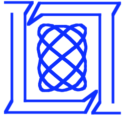


3-D Pixel



- Pixel electronics and detectors share area
- Fill factor loss
- Co-optimized fabrication
- Control and support electronics placed outside of imaging area

- 100% fill factor detector
- Fabrication optimized by layer function
- Local image processing
  - Power and noise management
- Scalable to large-area focal planes



Oxide-Bonded 3D-I Technology

- Smaller pixels than bump bonding
- 100% Fill Factor for Back Illumination

Tier-2 Readout

Tier-1 Detector 50µm thick

Center of Pixel Array

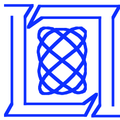
SOI Transistor

3-D Via

Oxide Bond

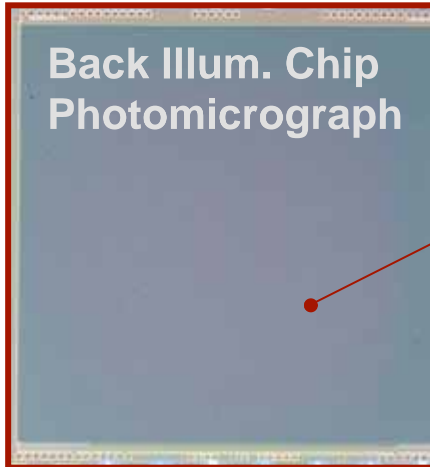
Single 8-µm pixel

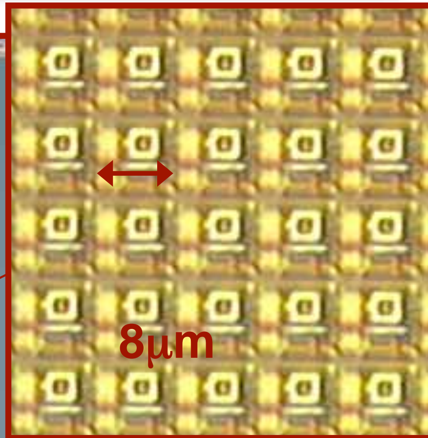
10µm

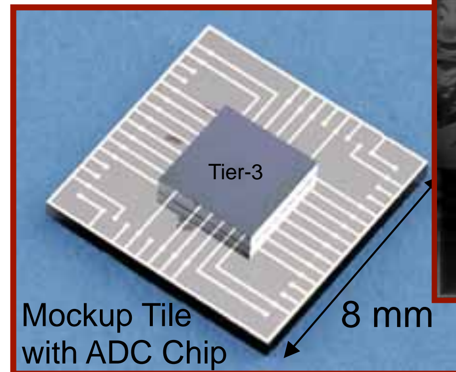


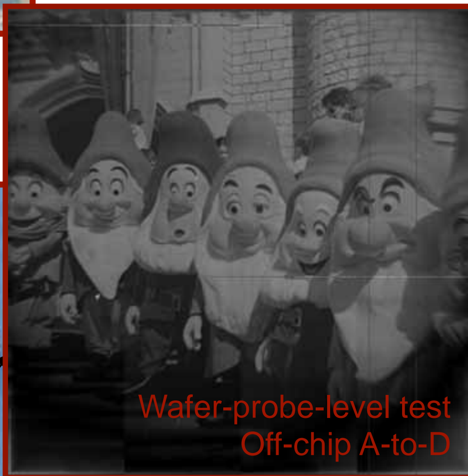
Example 3D Imager Demonstrations (1)

Two-Tier, CMOS Image Sensor
1024x1024 Array, 8-µm pixel



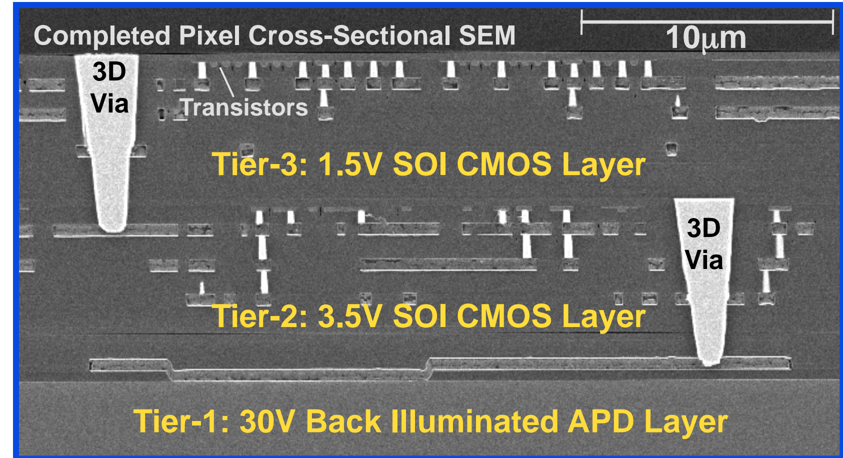


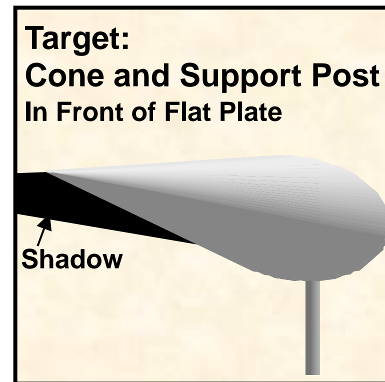


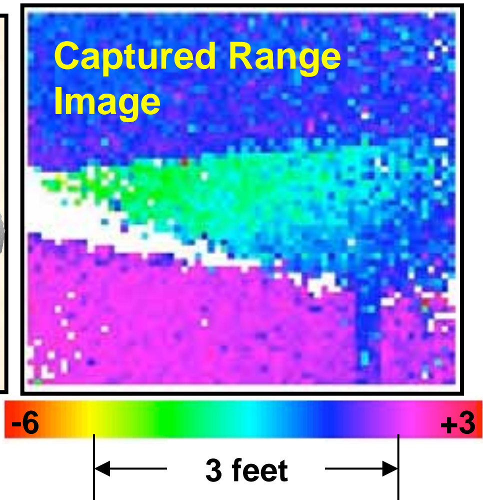


IEEE ISSCC 2005

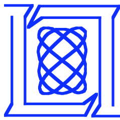
Three-Tier, GmAPD Laser Radar
64x64 Array, 50-µm pixel





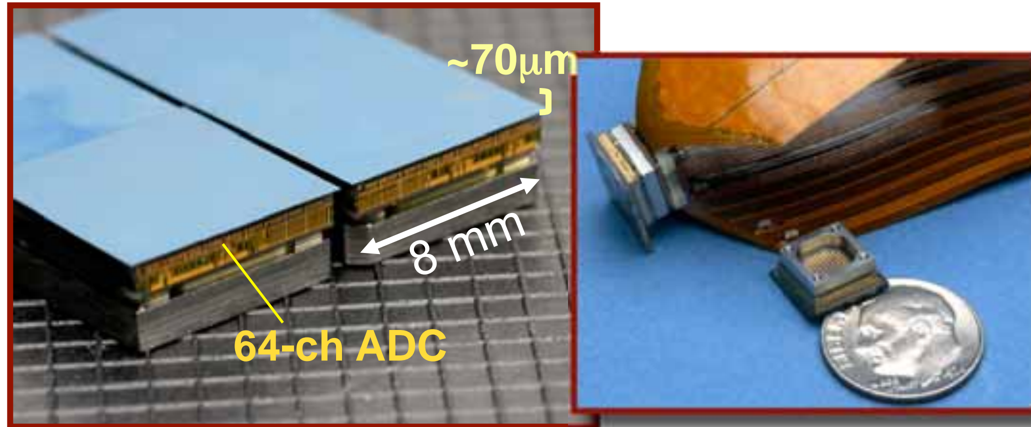


IEEE ISSCC 2006

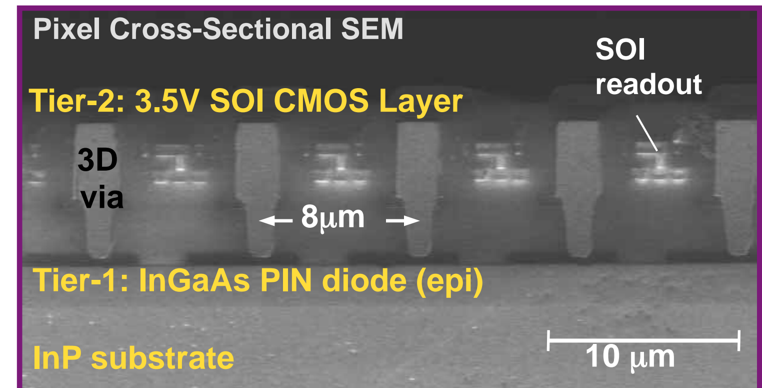


Example 3D Imager Demonstrations (2)

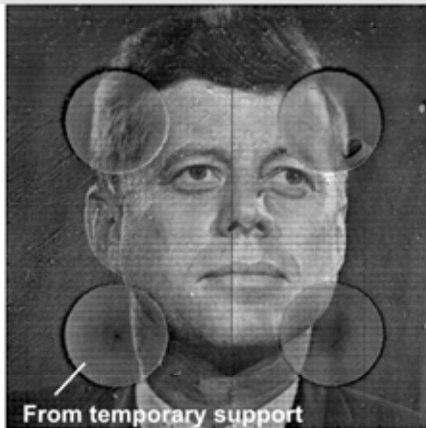
Seven-Tier, Four-side Abuttable CMOS APS
1024x1024 Array, 8-μm pixel



Two-Tier, InGaAs Detector
8-μm pixel

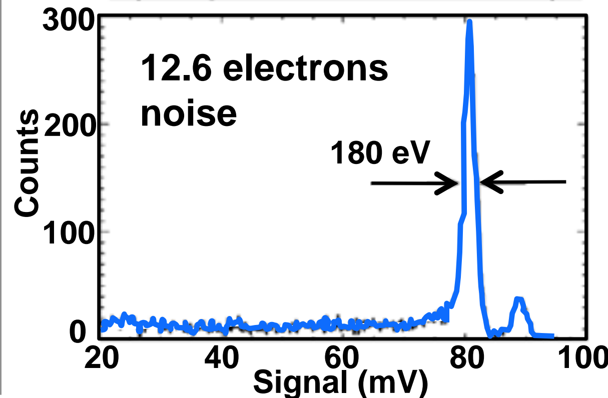


Captured Image at 10fps



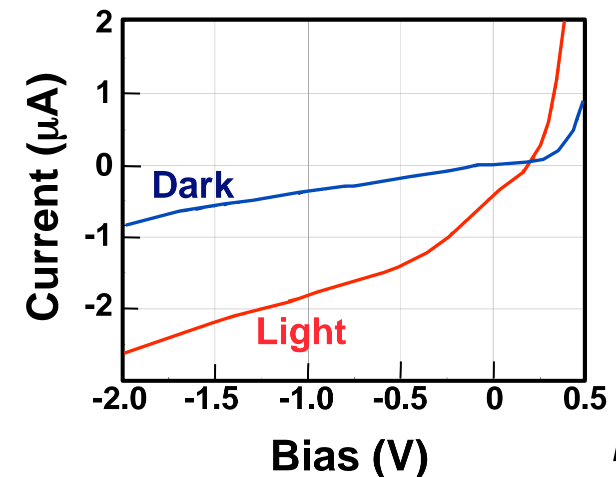
IEEE ISSCC 2009

Fe^{55} X-ray histogram
(companion two tier sensor)

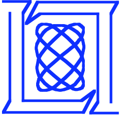


IEEE Trans. Elec. Dev.2009

Photo-response in PIN diode current

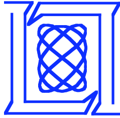


IEEE 3DIC 2009



Summary

- Lincoln Laboratory develops tiled CCD imagers with novel architectures for astronomy
  - First gigapixel focal plane successfully deployed
- New device and process improvements continue to increase responsivity and reduce dark current
- Next-generation imagers in development
  - Small pixel, large format, four-side abuttable devices
  - CCD and CMOS-based detectors
  - Back-illuminated, 100% fill factor, 3-D integrated image sensors
  - Advanced package development for higher data rate, tiled image sensors



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Dan O'Mara
Tony Soares

Microelectronics Lab
Doug Young
Andy Loomis
Chenson Chen
Jeff Knecht
Donna Yost
Kevin Newcomb
Keith Warner
Dave Astolfi
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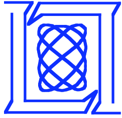
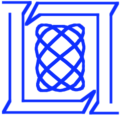


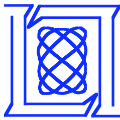
Backup



Tile Block Diagram

- Vertically stacked
- Pixel readout on Tier-2
- Timing control in Stack
- 64-ch 12-b pipelined ADC
- Digital output

Light
Tier-1
Pixel Array 1024 x 1024
Tier-2
Pixel Readout
64
Row decode/drive
Column decoder/amp
32
32
Imager Timing Control
5-Layer Silicon Stack incl. 2 CMOS chips
ADC Timing
32-ch ADC
ADC Timing
32-ch ADC
12
12
Sequencer
Ref
I2C and Clocks
Analog Power
LVDS out



Finished Tile Stack Appearance

Back Illuminated
3-D CMOS Imager
1024 x 1024 pixels
8.3 x 8.3 μm^2 pixel
64 analog outputs

5 layer stack
64 A/D converters
Timing & Control

1024x1024 pixels
>1 Million vias
144 gold stud bumps
2 x 96 side bus lines
88 POGO pins

Programmable Digital Imaging Tile