detectors for astronomy 2009

LCOGT detector electronics

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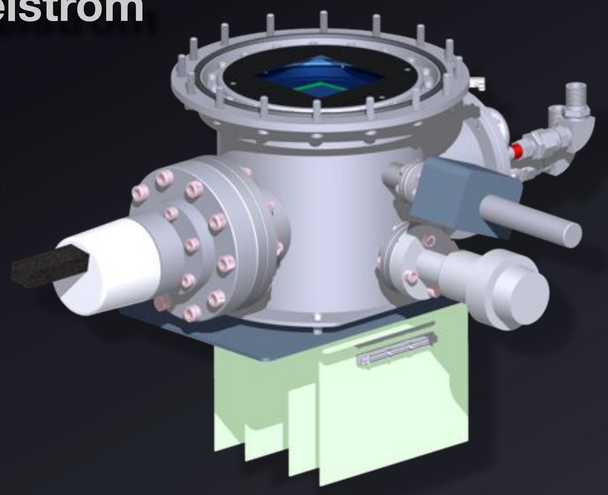
Abstract

LCOGT aims to build a worldwide network of 2, 1, and 0.4 m telescopes. Each will be equipped with high performance CCD cameras optimized for precision photometry. The baseline detector is a cryogenically cooled Fairchild CCD486. The sheer number of instruments involved in the project and their global deployment drives us to develop our own controller and interface software. The system is designed to handle up to 16 channels (for a future 4 CCD mosaic) at 2 Mpix/s with 16 bit resolution.

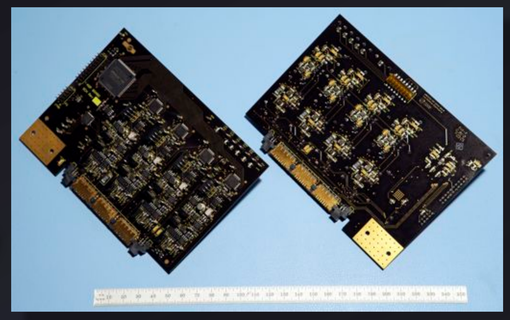
The key feature of our controller is the DC coupled analog signal processor. CCD output signals of interest are a set of small time-variant (AC) voltage steps (on the order of uV) embedded in a waveform with a large time-invariant (DC) value (on the order of 20V). Typically the large DC component is removed by AC coupling of the signal and subsequently amplifying and measuring the resultant waveform.

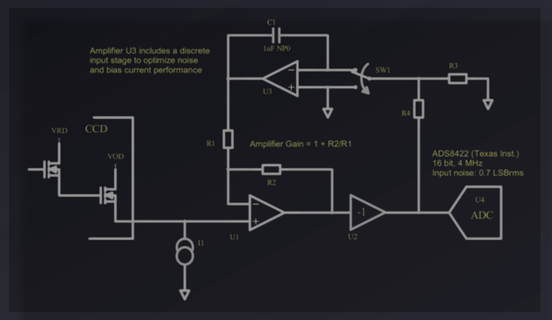
Our system optimizes detector readout rate, eliminates all sources of error due to non-ideal properties of capacitors, eliminates charge injection and reduces temperature induced gain non-linearity. In addition, the information in the DC level is preserved and available for measurement.



Prototype camera with attached controller

Analog Signal Processor





Analog output waveforms

Green is the raw DC coupled CCD output relative to ground. Yellow and cyan are the differential inputs to the ADC. Each A/D conversion is indicated by the rising edge of the square waveform.

During Exposure:

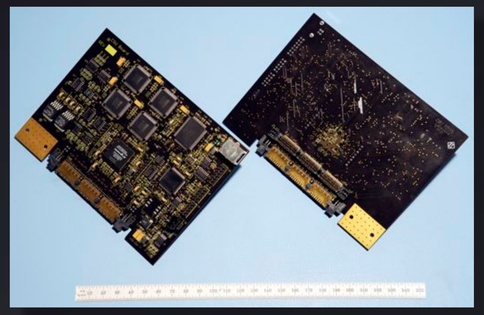
1. SW1 is in upper position which closes global feedback loop.
2. Resistors R3 and R4 maintain input to ADC at zero volts.
3. Output of U1 is forced to zero volts.
4. Output of U3 negates the DC level of the CCD

During Readout:

5. Immediately prior to frame readout, SW1 is switched to lower position and opens global feedback loop
6. C1 becomes a S/H element and holds the DC voltage that negates the DC level of the CCD
7. Amplifier gain is set by R1 and R2 and is: (1 + R2/R1)
8. ADC is used to accomplish Digital CDS
9. I1 is configured as a low-noise Widlar current source to provide an active load to the CCD output maximizing gain.

Clock Sequencer Unit

The CSU is designed to handle 16 channels of 4 MHz 16-bit data. It also sequences up to four clock drivers, performs digital filtering and multiplexes data over a single output bus. The prototype is USB based for simplicity and is bus limited. We plan a gigabit ethernet output, and if speed requires it, a dedicated point-to-point fiber link. Each controller uses one CSU, and one temperature and telemetry module.

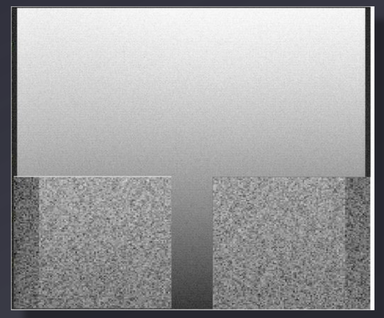


Controller First Light

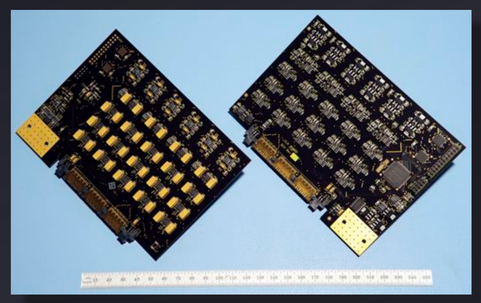
Image of a plastic water bottle using a simple pinhole as a lens. Engineering grade SITe 1024 device. Thermoelectrically cooled to -24 °C.

Dark Current Flat Field

Bias level (0 s) exposure, showing the accumulation of dark charge during a readout. The insets show pre/over scan with increasing contrast .

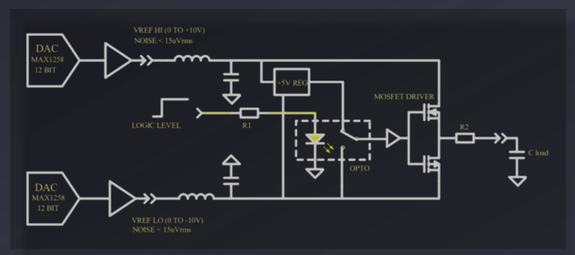


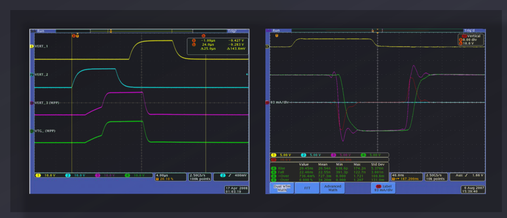
Clock Driver



The front and back of a single clock driver module. The controller is capable of sequencing four such modules.

The clock driver is inherently stable and uses no op-amps in the output stages. It has a very low quiescent power draw as it does not use large bias voltages and currents. It is capable of sourcing 4 A transients into a large capacitive load.

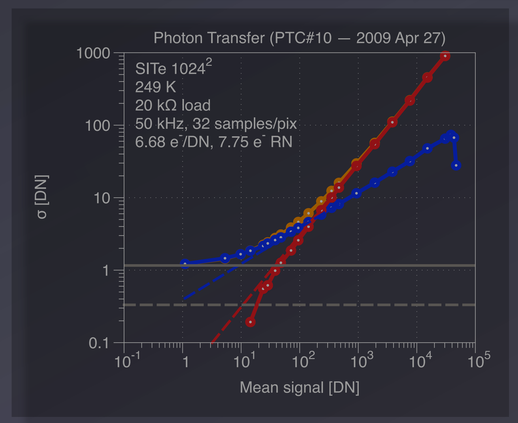




We made an effort to minimize parts count for increased reliability and board yield. A single set of DACs provide reference levels for similar clock phases. The serial phases (right figure) are capable of 20 Vpp at 60 MHz. Shown is the output into a 180 pF, 54 ohm load simulating the serial register of a CCD486. The parallel MPP phases use two slopes to gently bring the phase through inversion decreasing CTI while maintaing a high parallel shift rate (0.1 uF load).

Photon Transfer Curve

Orange indicates raw pixel-to-pixel noise. Red shows the pure fixed pattern noise component (flat field non-uniformity) against theory. Blue indicates system noise asymptoting to system read noise at low signal and shot noise at high signal. The dashed grey line represents controller noise with grounded inputs.



References

1) Janesick, J. R. Scientific Charge-coupled Devices. SPIE, 2000.

2) Janesick, J. R. Photon Transfer. SPIE, 2007.

Acknowledgements

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