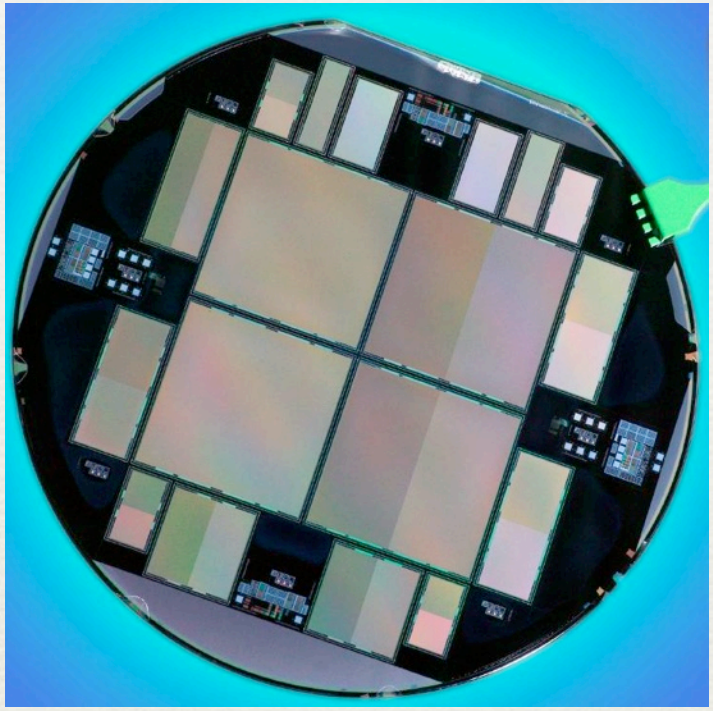
A radiation tolerant, low-power cryogenic capable CCD readout system:

Enabling focal-plane mounted CCD read-out for ground or space applications with a pair of ASICs.

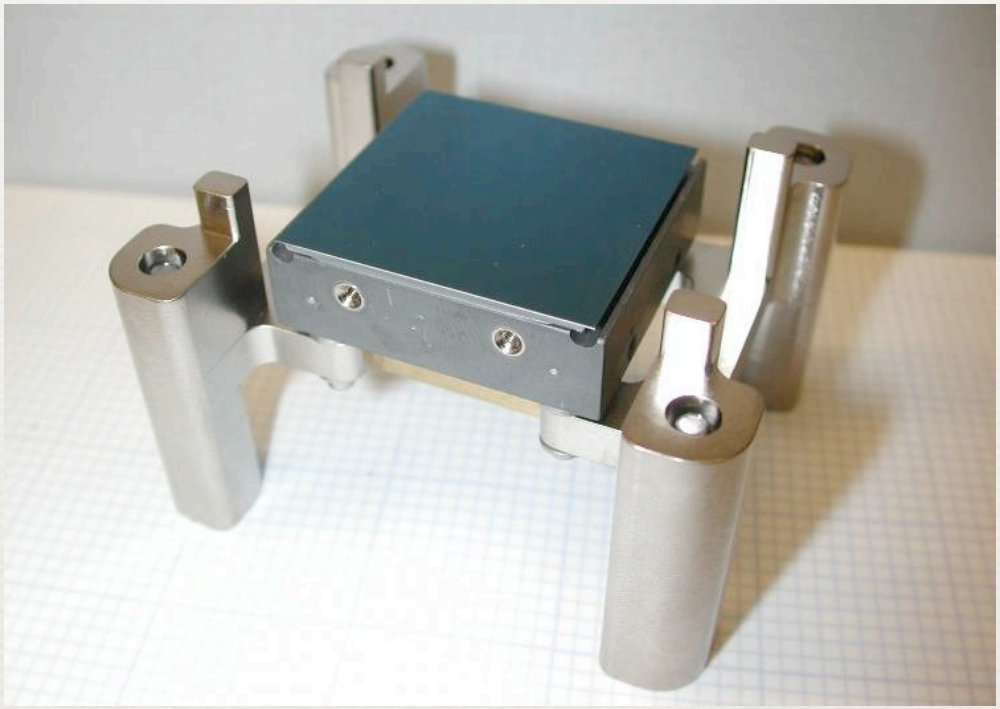
Overview

- What do we want to read out
- The CCD readout system
- The signal processing ASIC
  - Principles of operation
  - Performance
- The clock driver and bias generator ASIC
  - Principles of operation
  - Performance
- Conclusion
- Outlook

CCDs for JDEM



3.5k x3.5k 10.5μm pixel,
4 corner readout devices

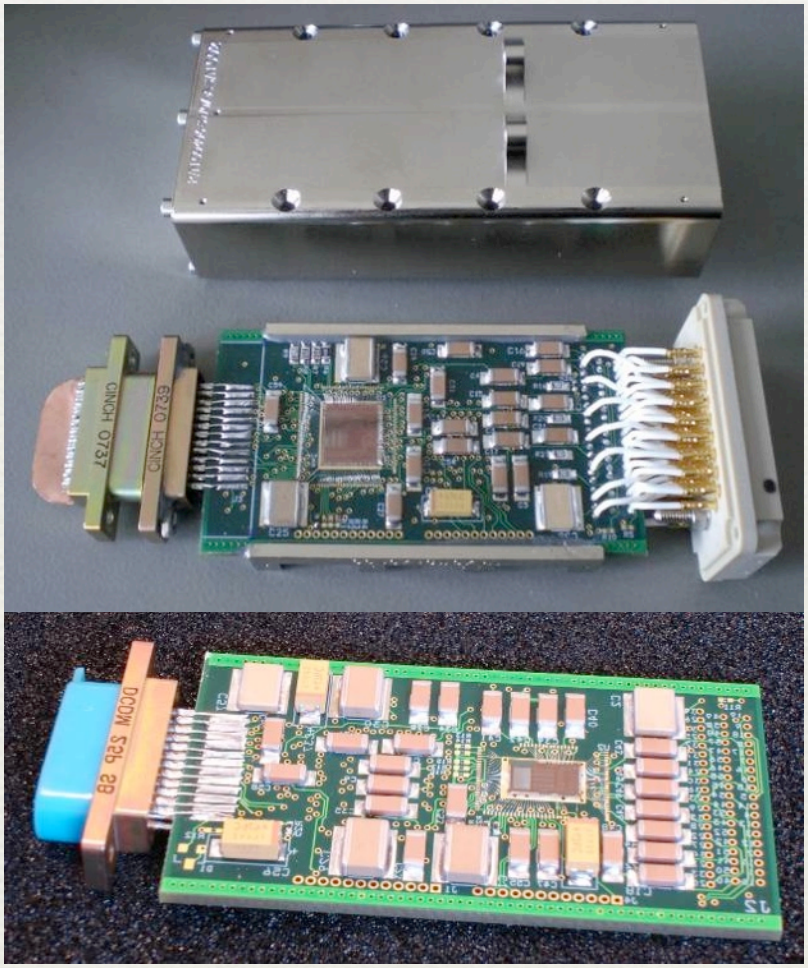


CCD on a 4-side abuttable
SiC mount

Other formats up to 4k x4k 15μm pixel are
manufactured for ground based astronomy

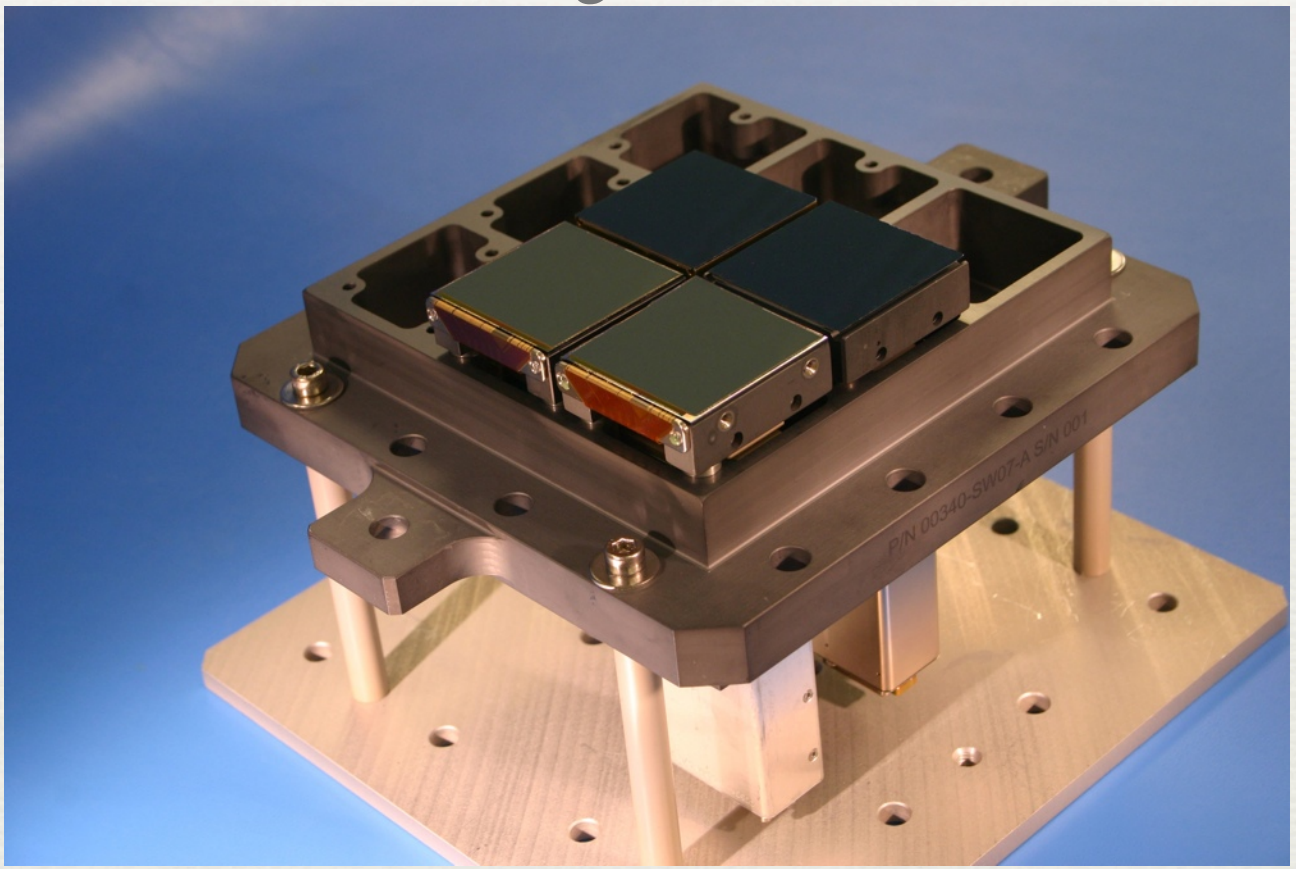
CCD readout module

- Form-factor to fit behind the CCD
- One chip set: Signal processing and clocks/bias voltages
- Attaches directly to the CCD: minimizes noise pick-up, stray capacitance
- Runs in the cold: Need only run power and LVDS wires, no analog video



Readout System

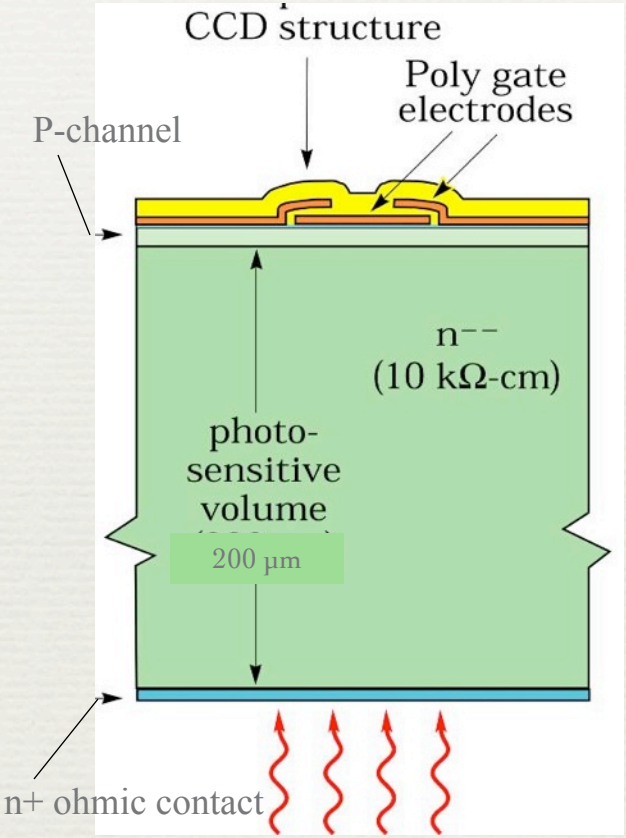
- Compact
- Modular
- Low power
- Scalable



Fill any focal plane and collect the bytes

LBNL CCDs

- P-channel CCDs require opposite polarity bias voltages
  - + Higher radiation tolerance
- Fully depleted CCDs require a depletion voltage
  - + Less than 5μm rms point spread function
- Thick CCDs (~200μm) need to be over-depleted to achieve low charge diffusion

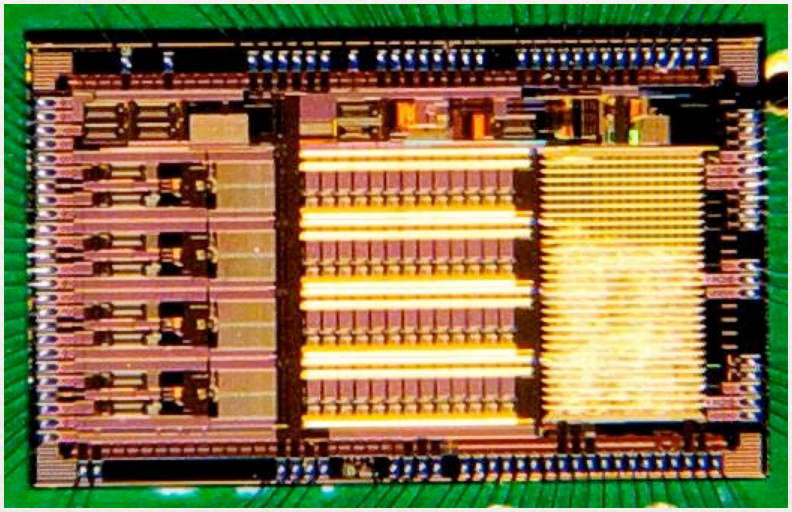


C.J. Bebek et al "Development of Fully Depleted, Back-Illuminated Charge Coupled Devices," SPIE **5499**, 10 (2004)

Analog signal processing design goals

- Low average power (~ 10 mW/channel)
  - Will be higher during read-out
- Ultra low noise (< 10 μV @ 100 kHz, equiv. 2 e^-)
- Large dynamic range (~96 dB)
- On-chip A/D converter
- Good flexibility through programmable timing
- Radiation tolerance
- Operation cryogenically and at room temperature
- 10 mK temperature measurement resolution

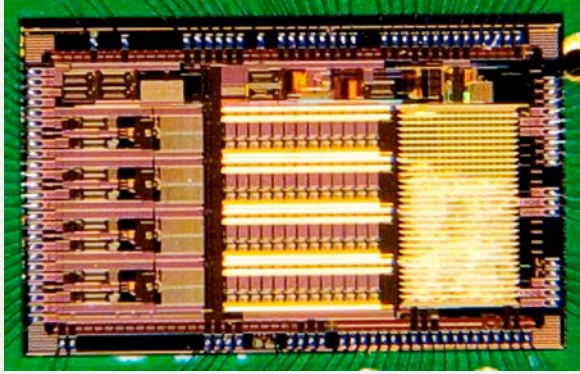
Signal processing: the CRIC (CCD readout IC)

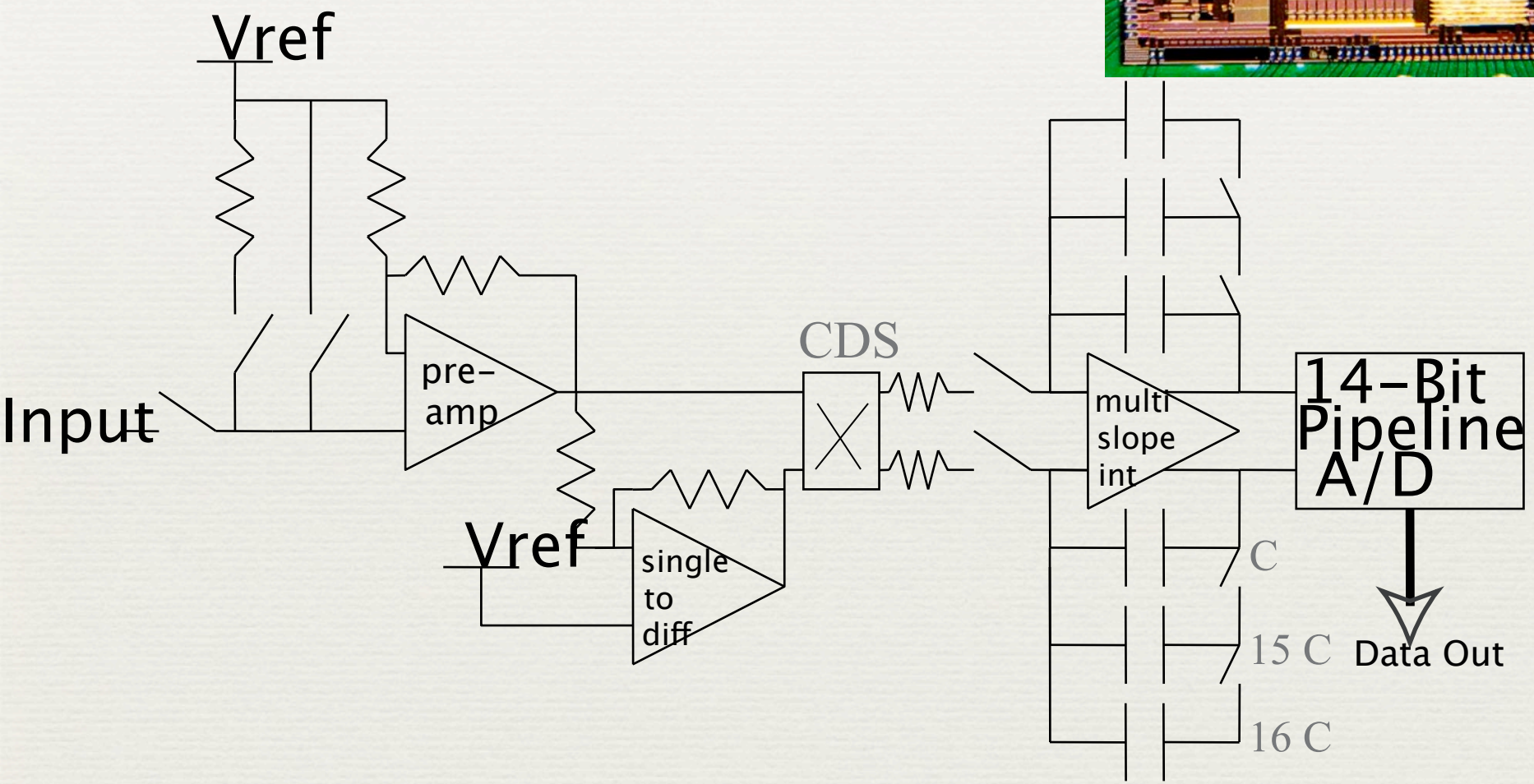


25 μm CMOS implementation of CRIC

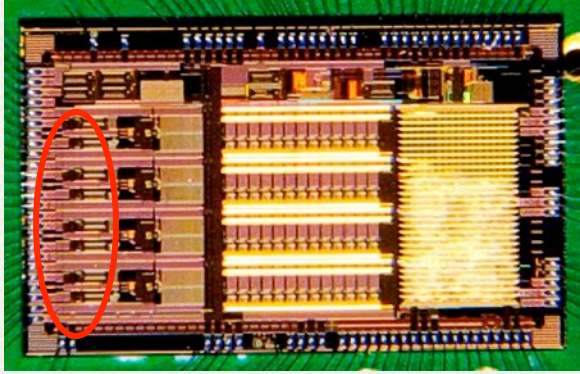
- 4 channels
- Pre-amplifier
- Single-ended to differential conversion
- Dual-slope integrator with three stage auto gain selection
- 14-bit pipeline ADC
- Single 'Convert' signal, all timing generated internally
- Test pulse injection for end-to end data flow test
- Voltage reference with warm and cryogenic mode

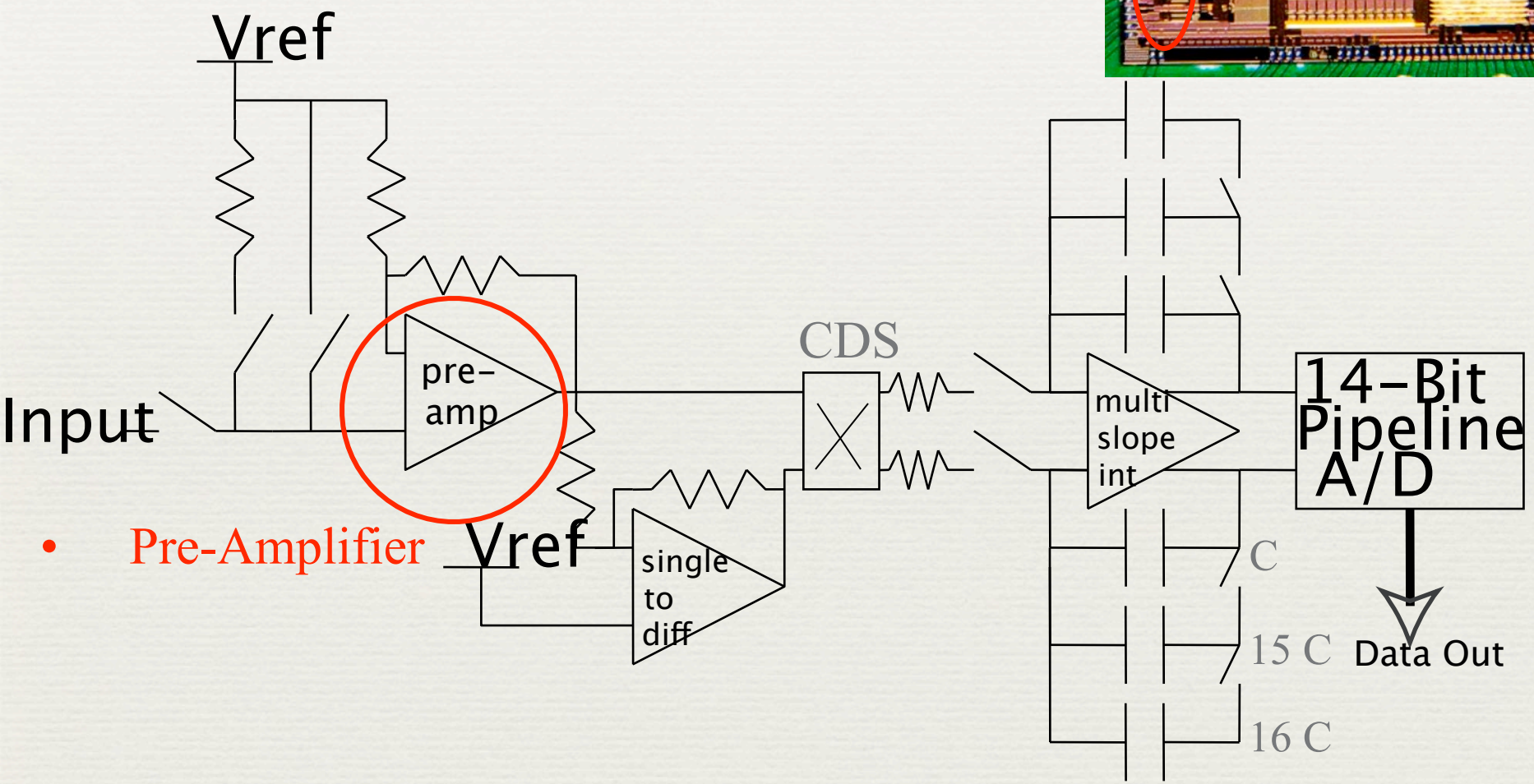
Signal Path




Vref
Input
pre-
amp
CDS
multi
slope
int
14-Bit
Pipeline
A/D
Vref
single
to
diff
C
15 C
16 C
Data Out

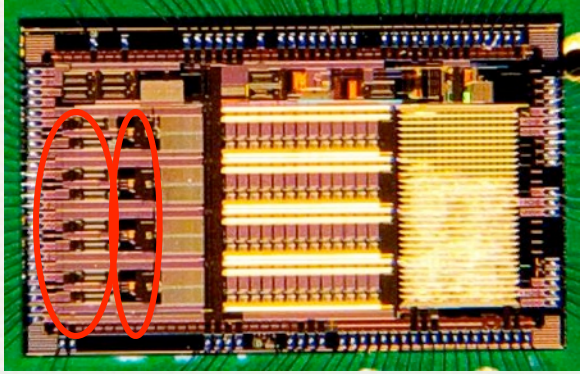
Signal Path

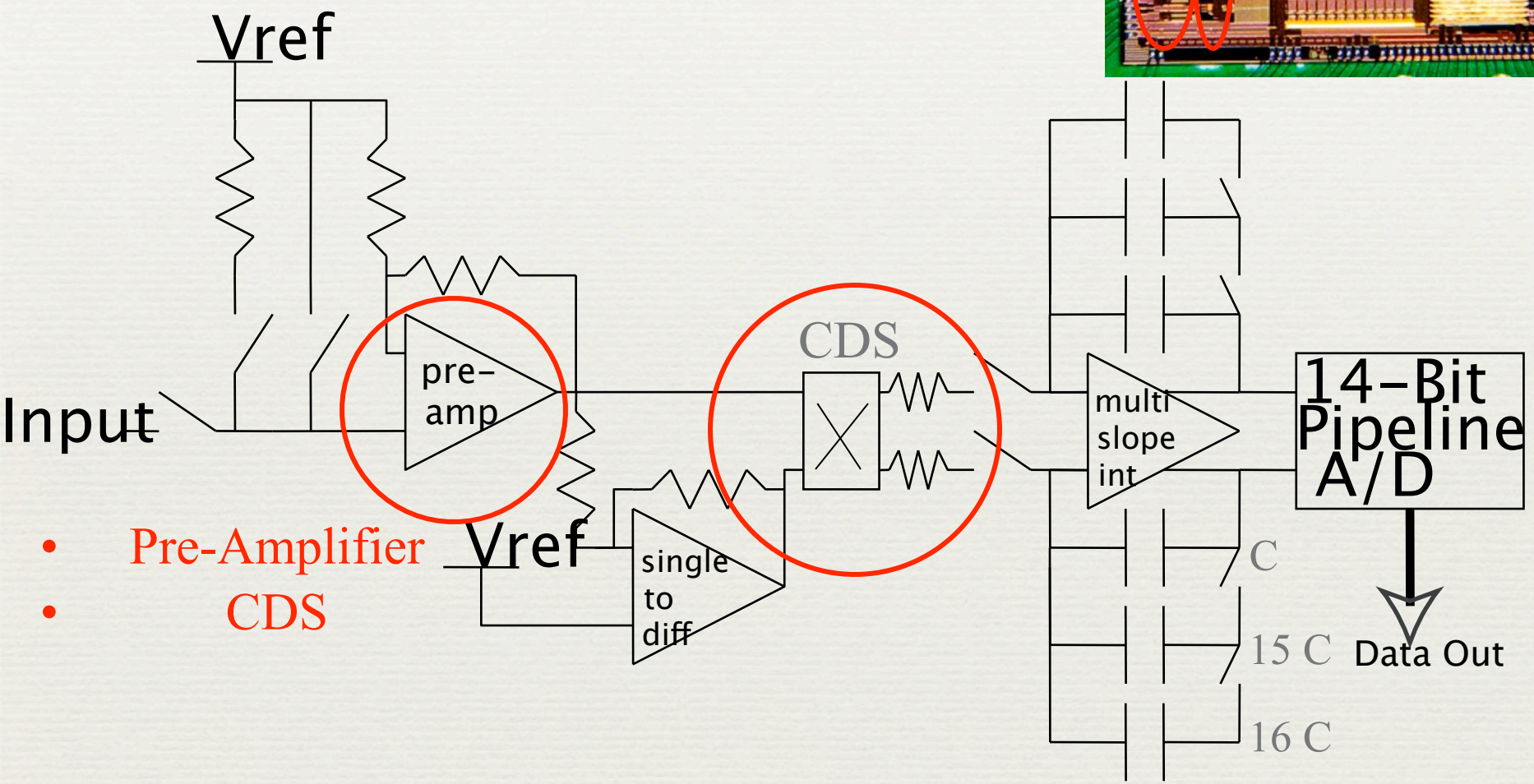




- Pre-Amplifier

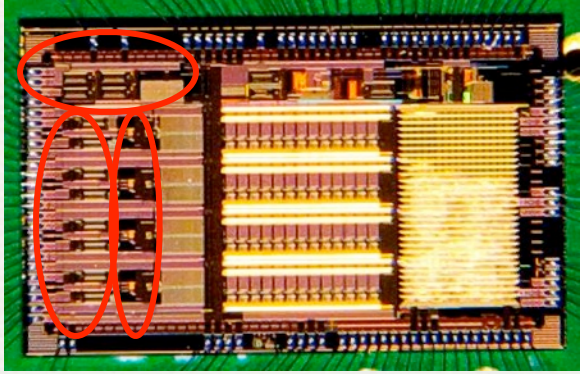
Signal Path

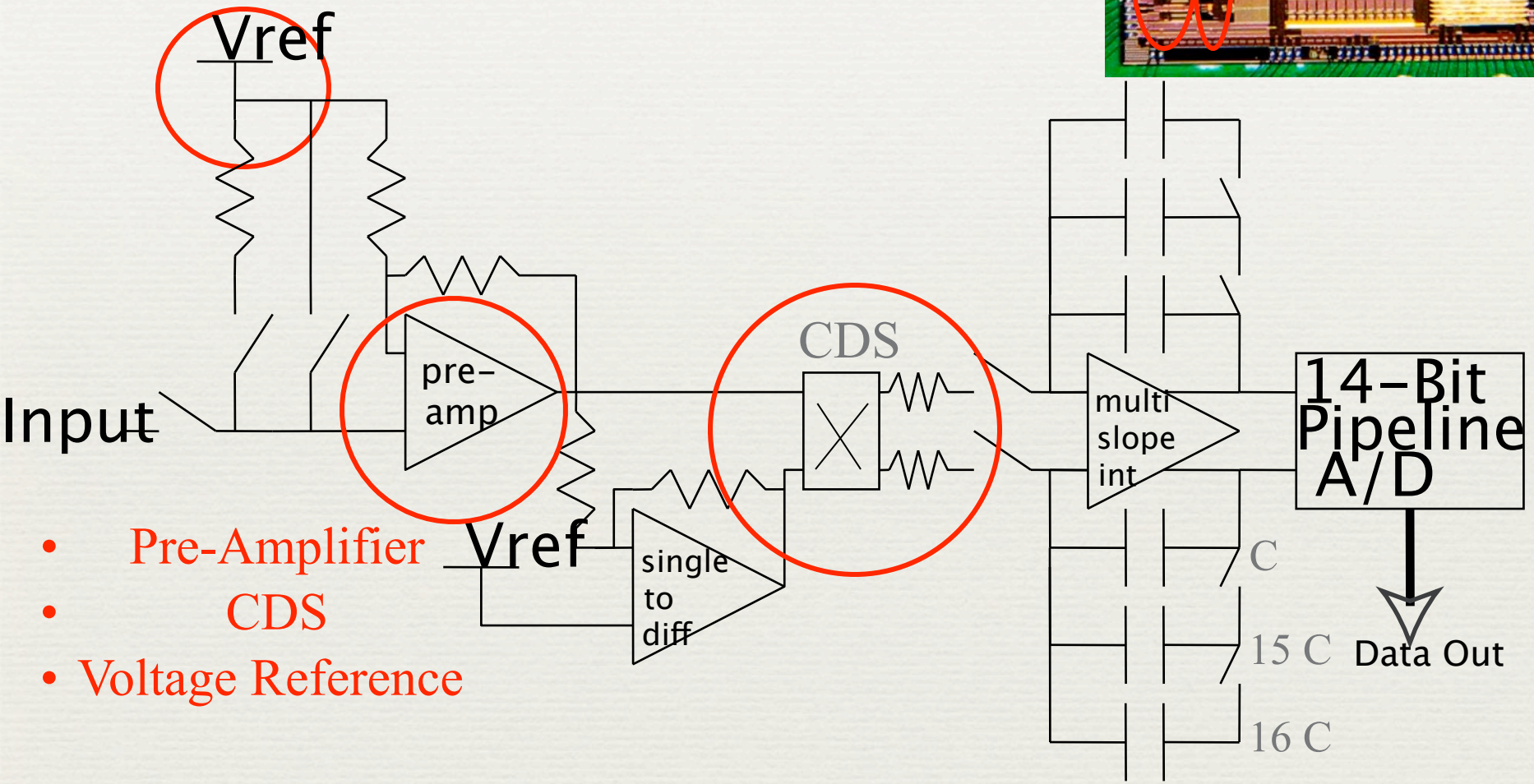




- Pre-Amplifier
- CDS

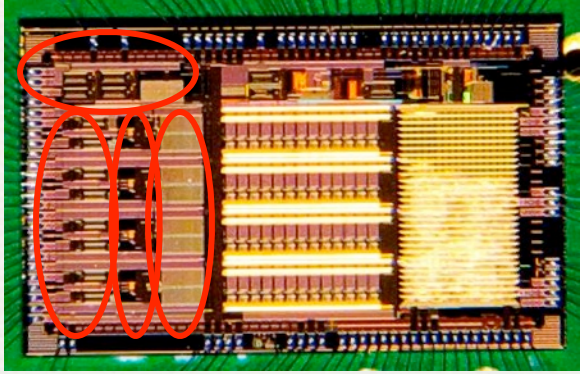
Signal Path

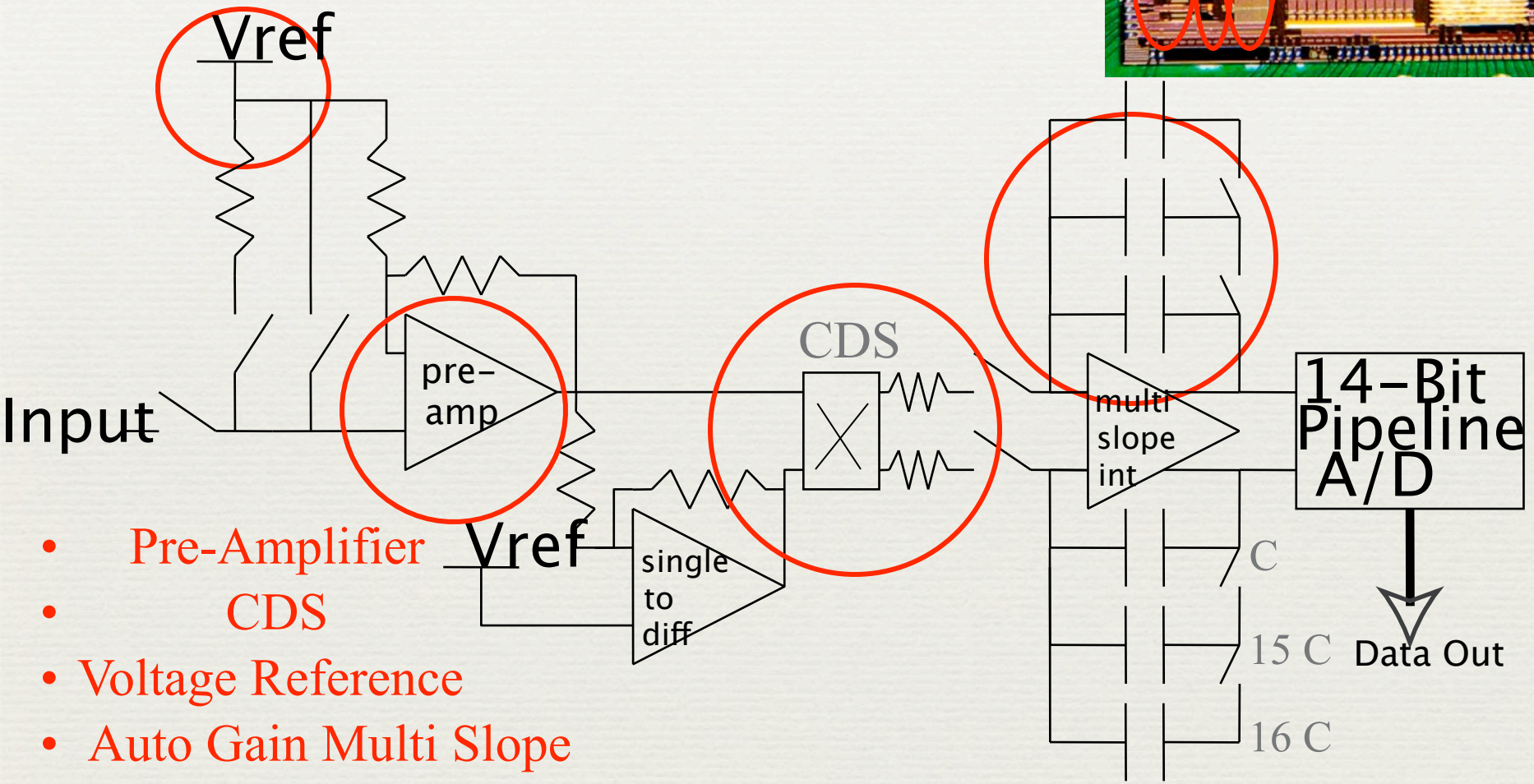




- Pre-Amplifier
- CDS
- Voltage Reference

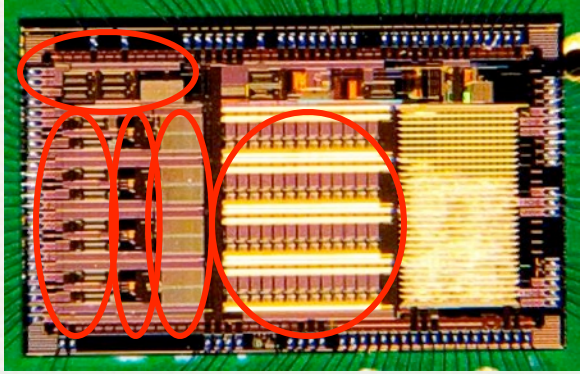
Signal Path

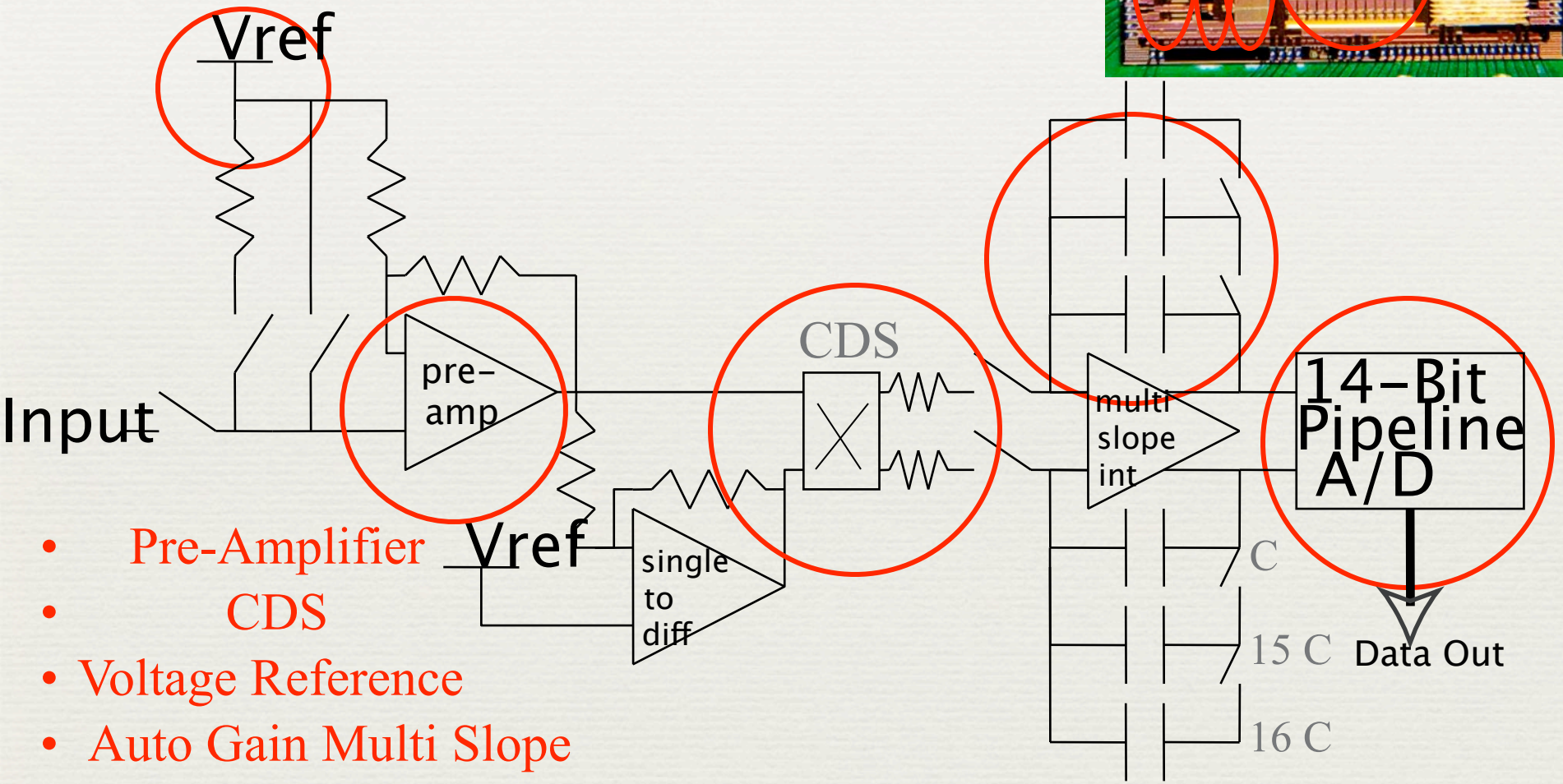




- Pre-Amplifier
- CDS
- Voltage Reference
- Auto Gain Multi Slope

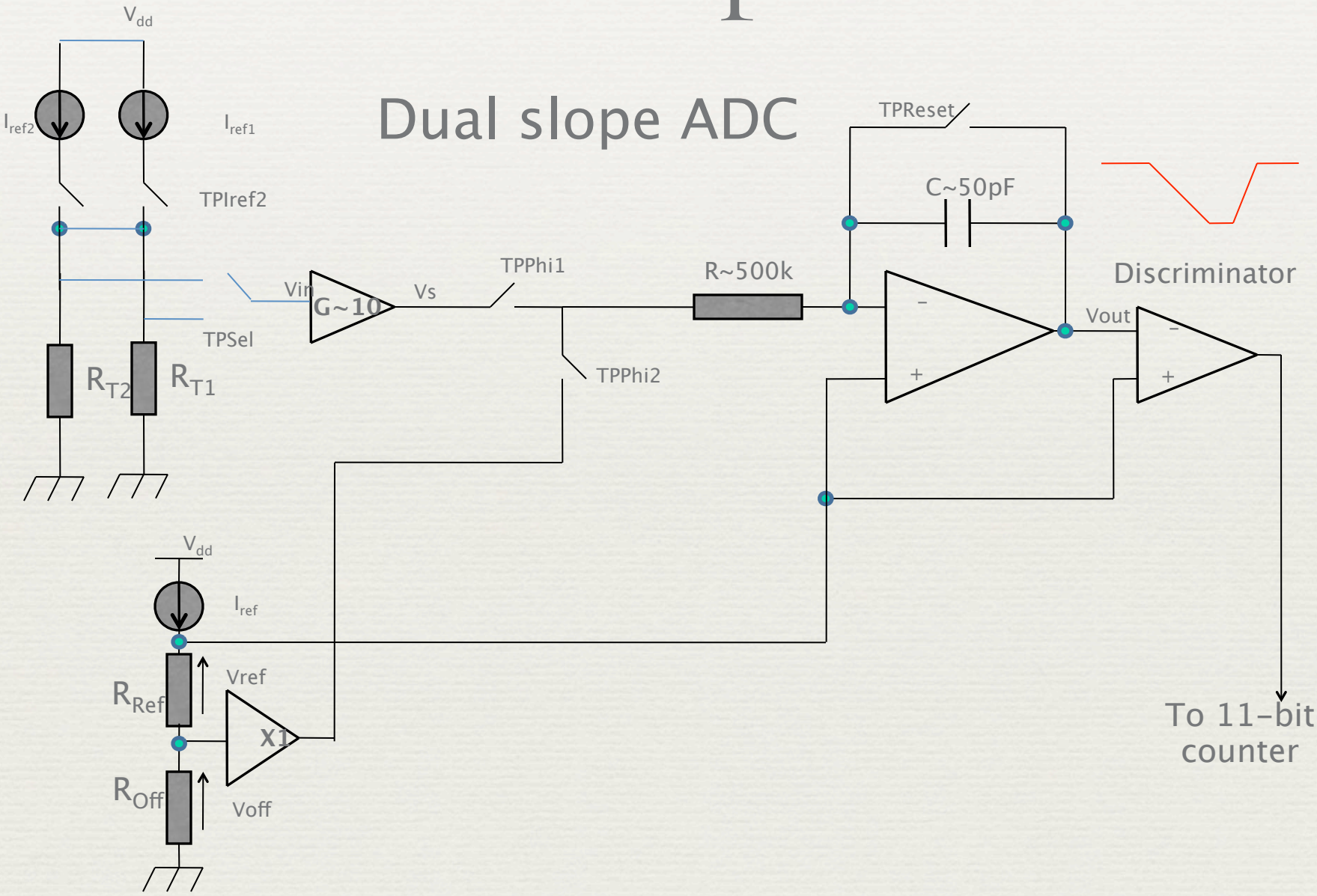
Signal Path



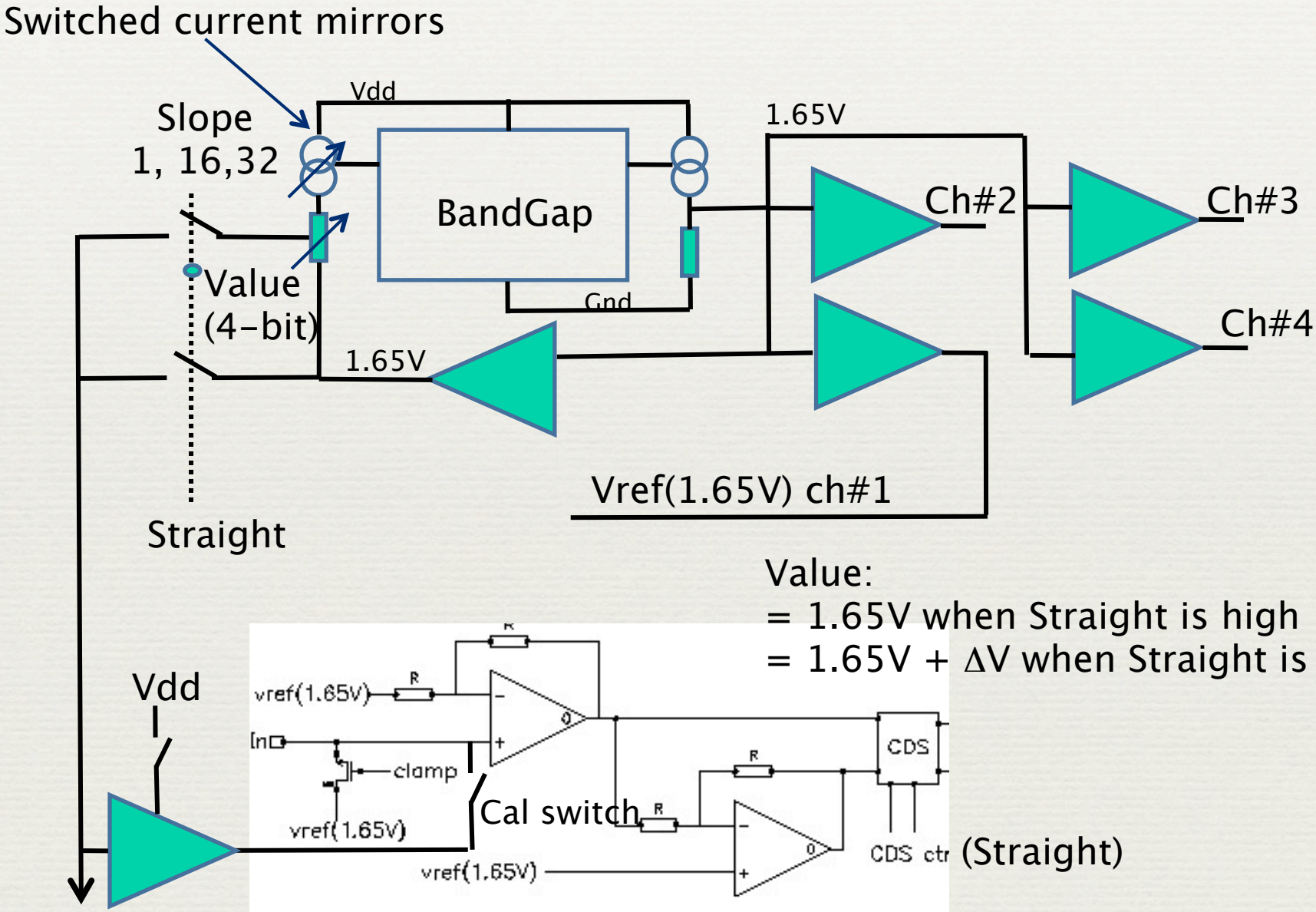


- Pre-Amplifier
- CDS
- Voltage Reference
- Auto Gain Multi Slope
- Pipeline ADC

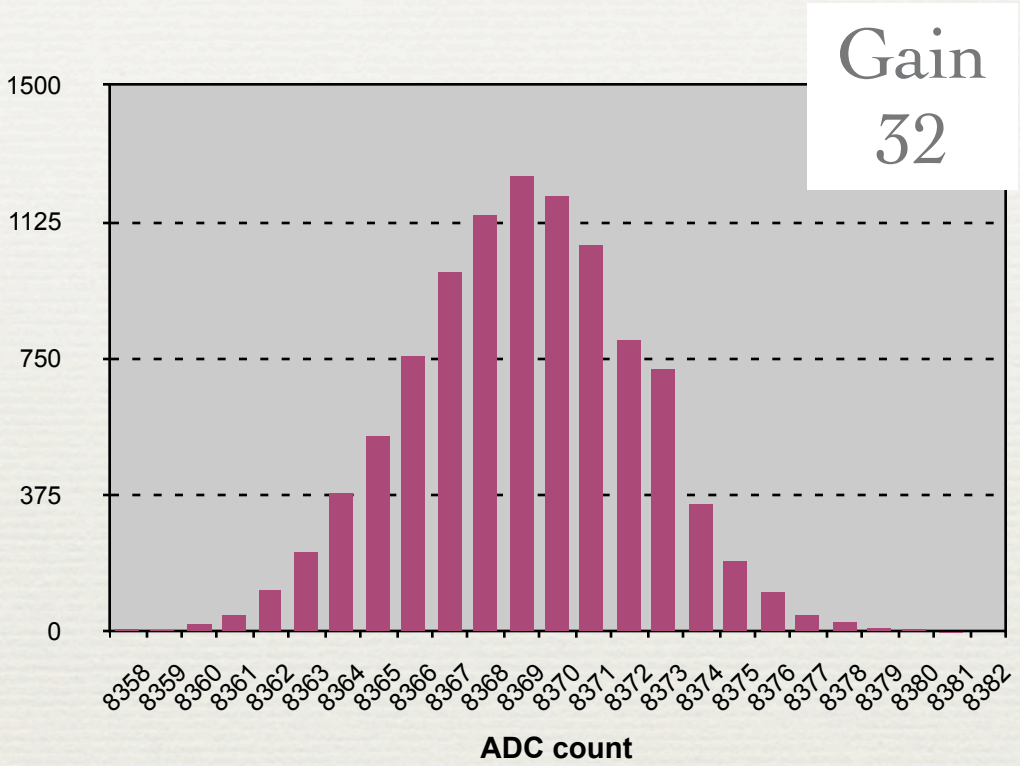
CRIC temperature

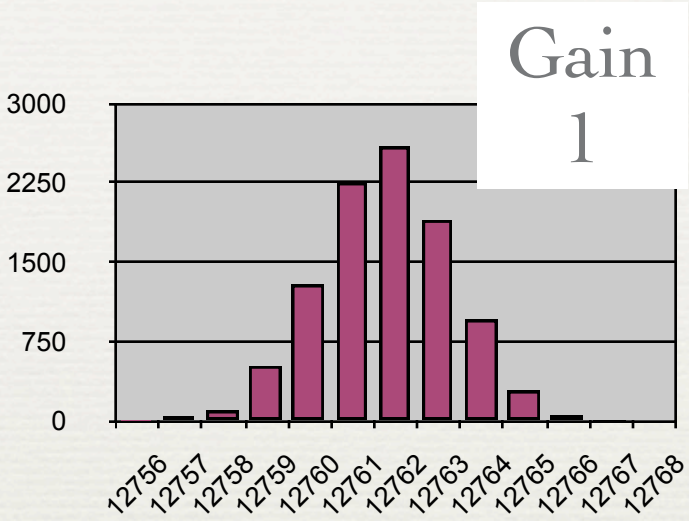


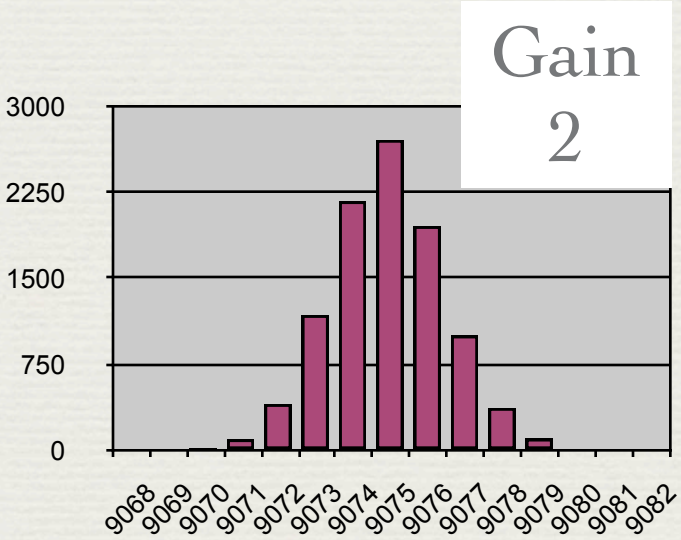
Test pulse injection



Noise





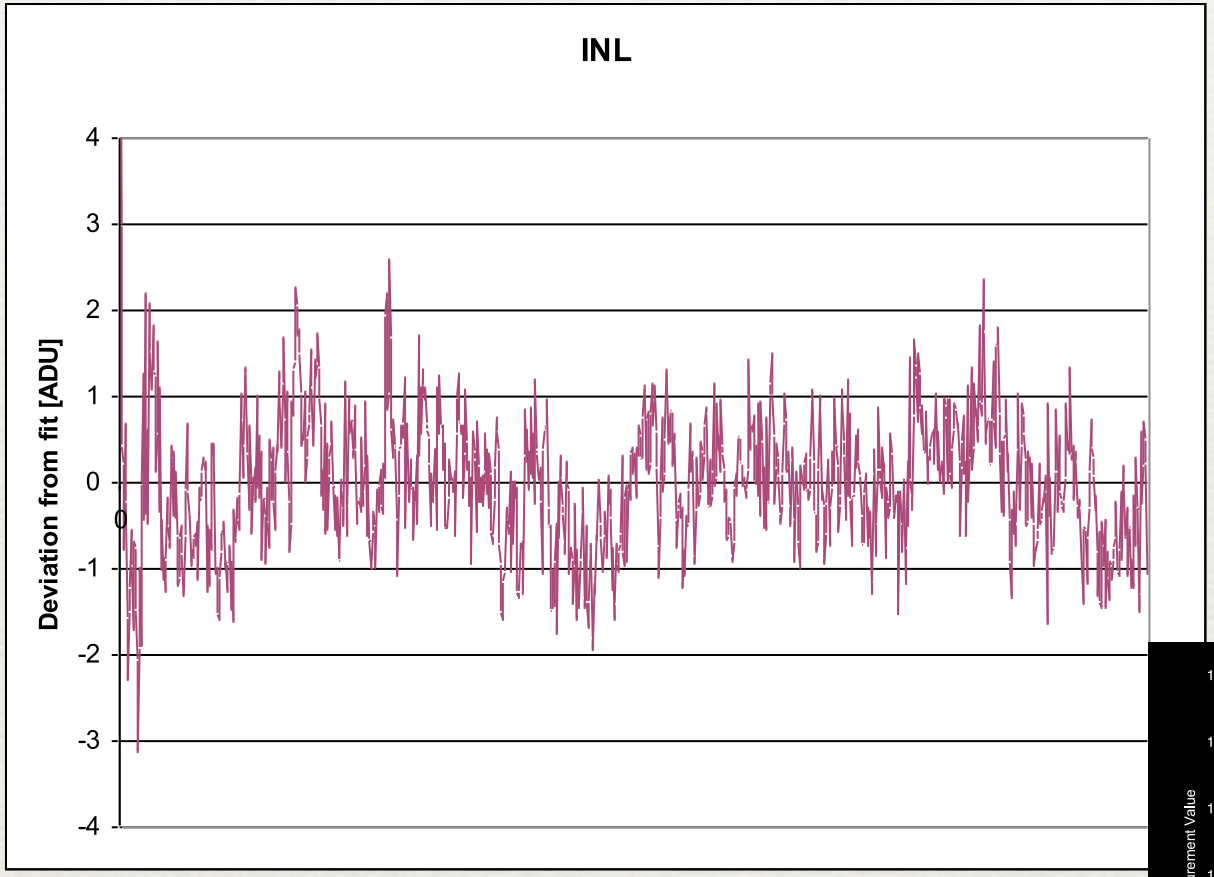


Noise measured at the operating temperature of 140K:

For small signals (high gain) noise is pre-amp dominated at 3.2 counts RMS, equivalent to 6.2 μV

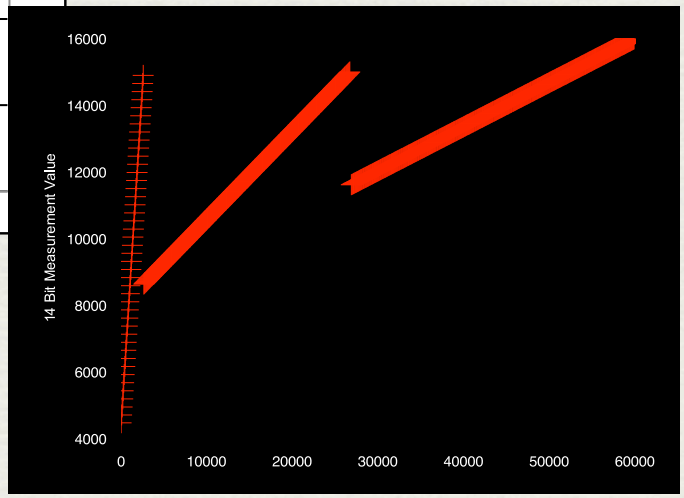
For larger signals (low gain) noise is ADC dominated at 1.5 counts RMS

Integral Nonlinearity



- 0.8 Counts RMS INL
- 6.1 Counts pk-pk

1 Count = 1.93 µV



Power consumption

Digital power

- 5.0 mW/channel in standby
- 5.8 mW/channel sampling at 100 kHz

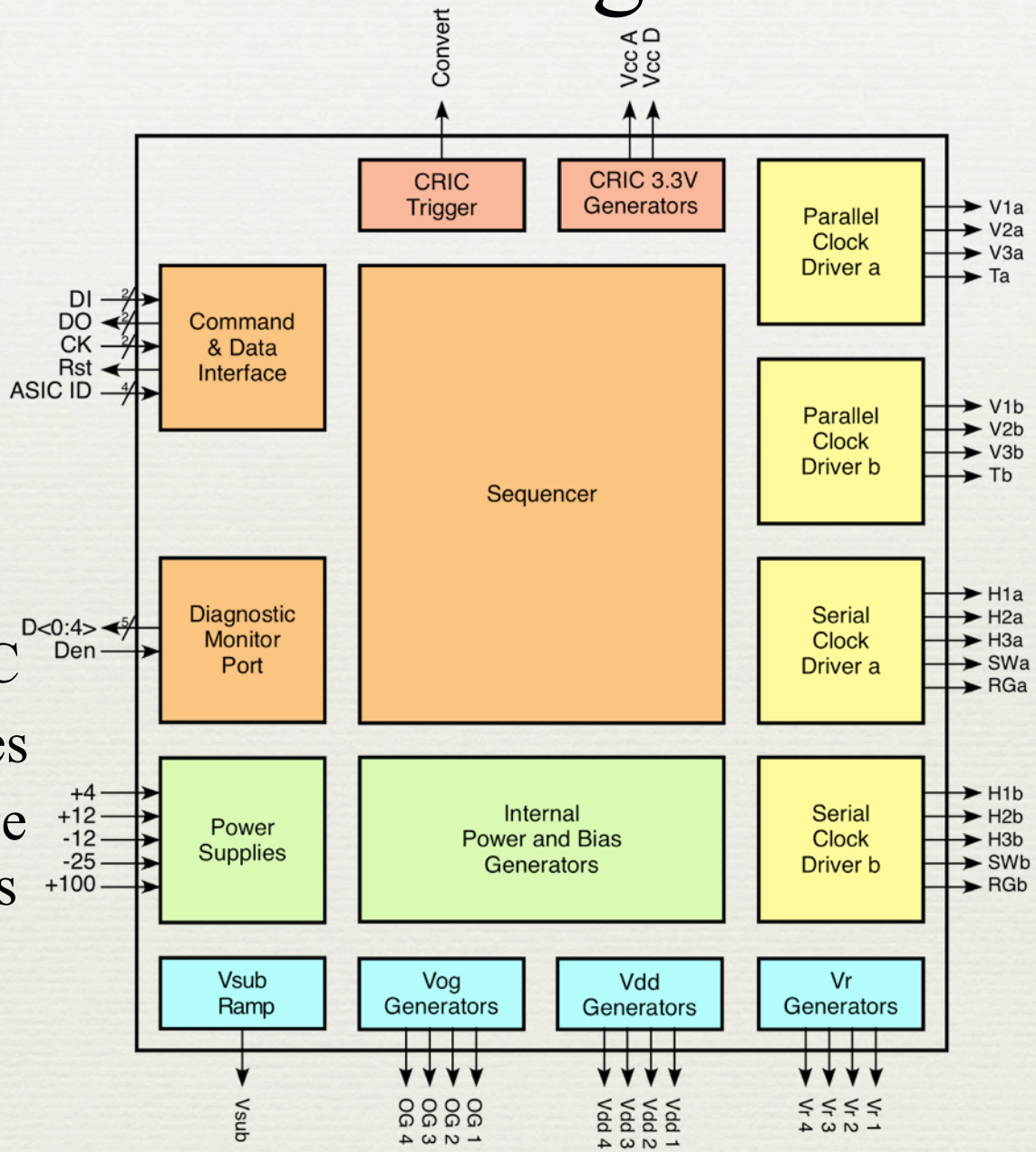
Analog Power

- 0.25 mW/channel in standby
- 13.1 mW/channel sampling at 100 kHz

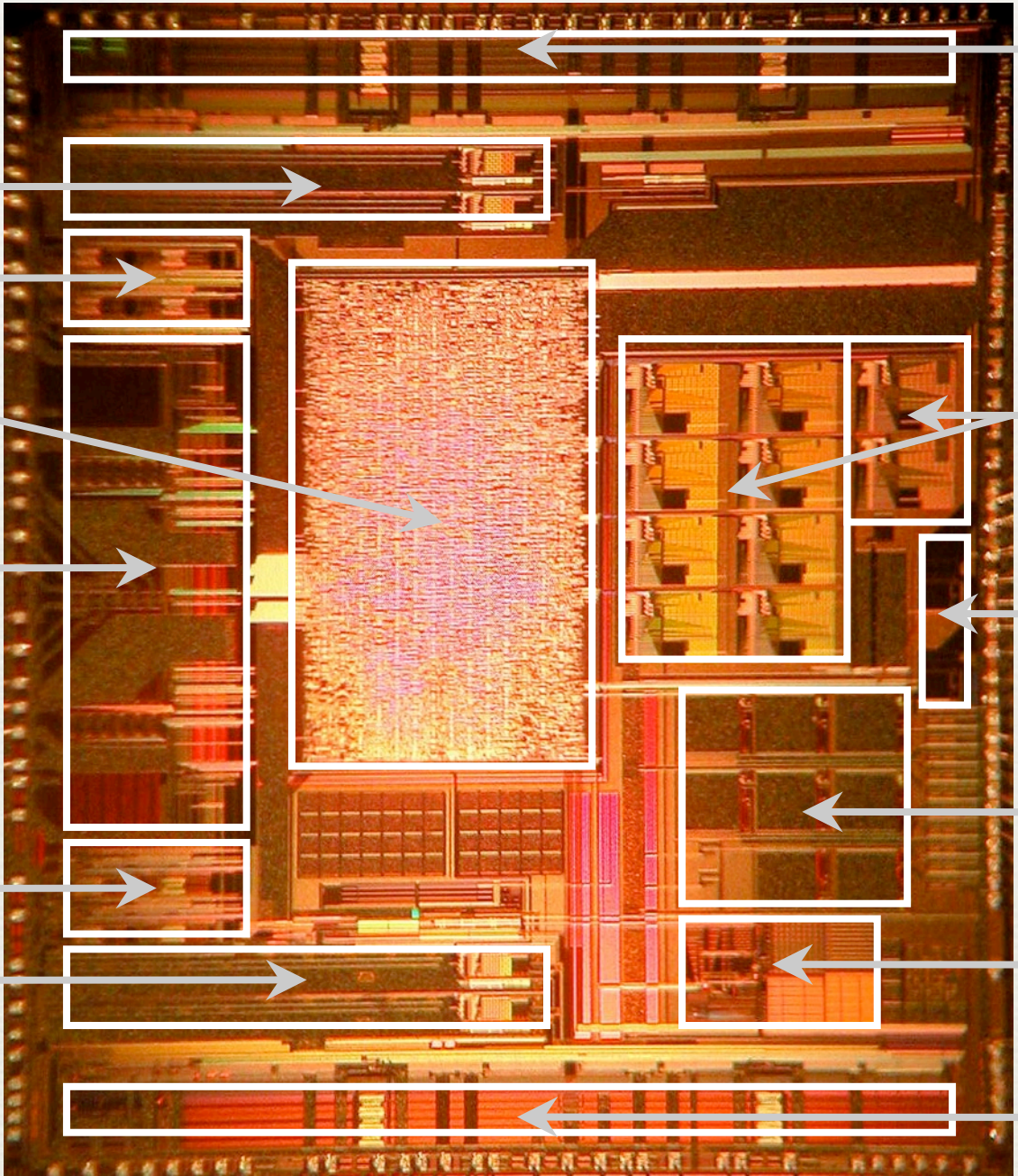
Standby is a low power mode where the bias currents to all amplifiers are disabled, but temperature monitoring and command interface remain active.

CLIC – bias and clock generator

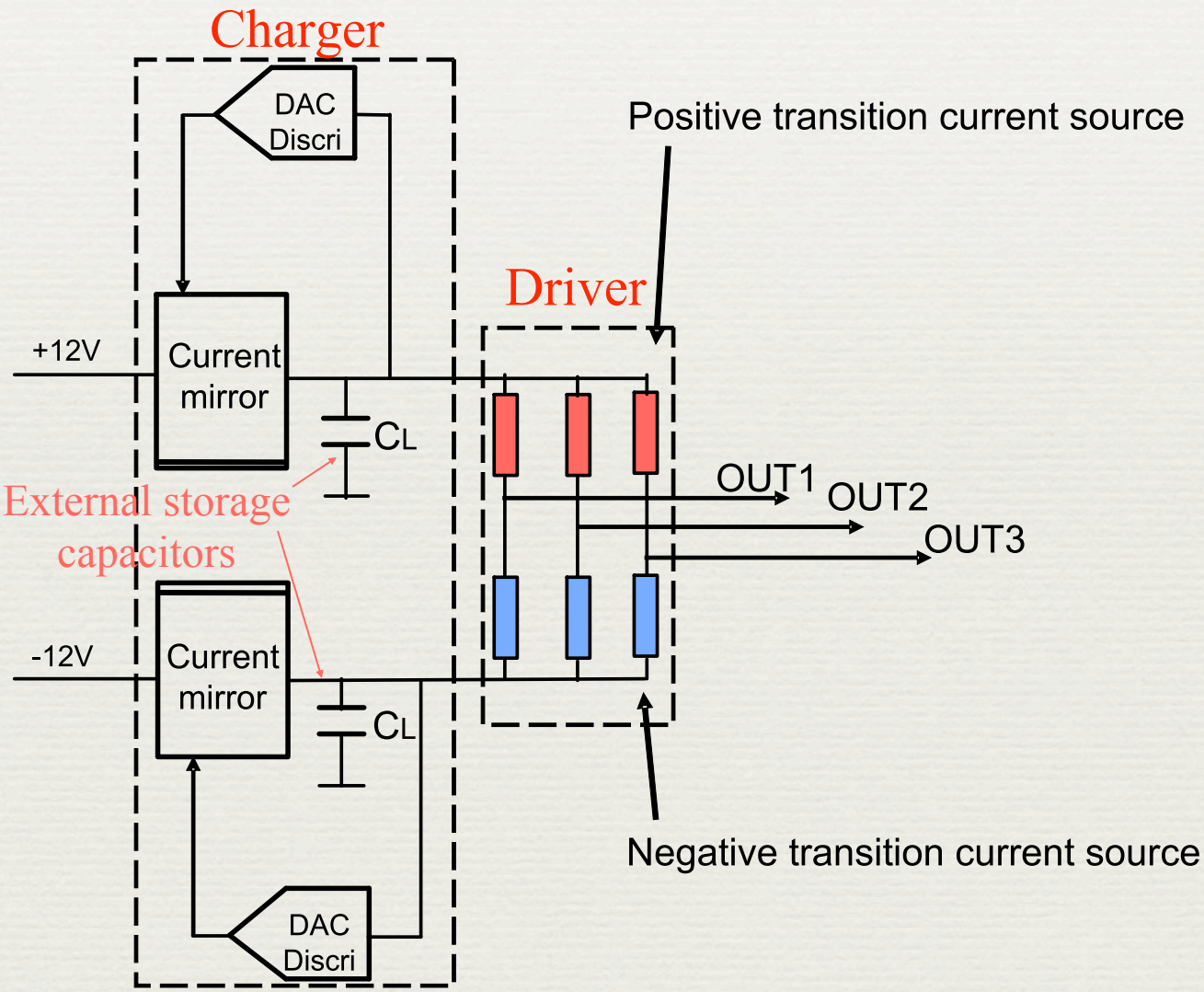
- Flexible clock pattern generator
- Clock level adjustments
- Programmable clock rise time
- Adjustable CCD bias voltage with controlled ramp rate
- 3.3 V generators for CRIC
- 12 adjustable bias voltages
- Supports radiation damage monitoring readout modes of CCD – pocket pump, EPER, FPER.



CLIC – bias and clock generator

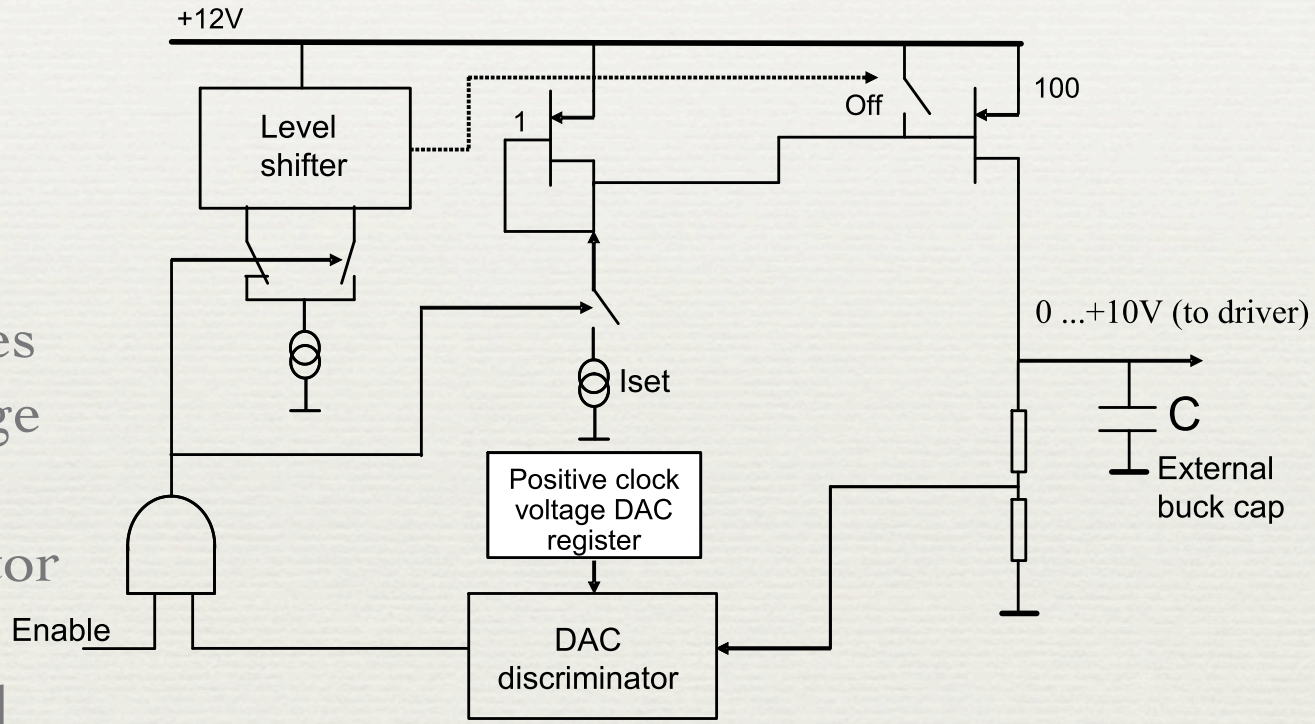


Clock driver: principles of operation



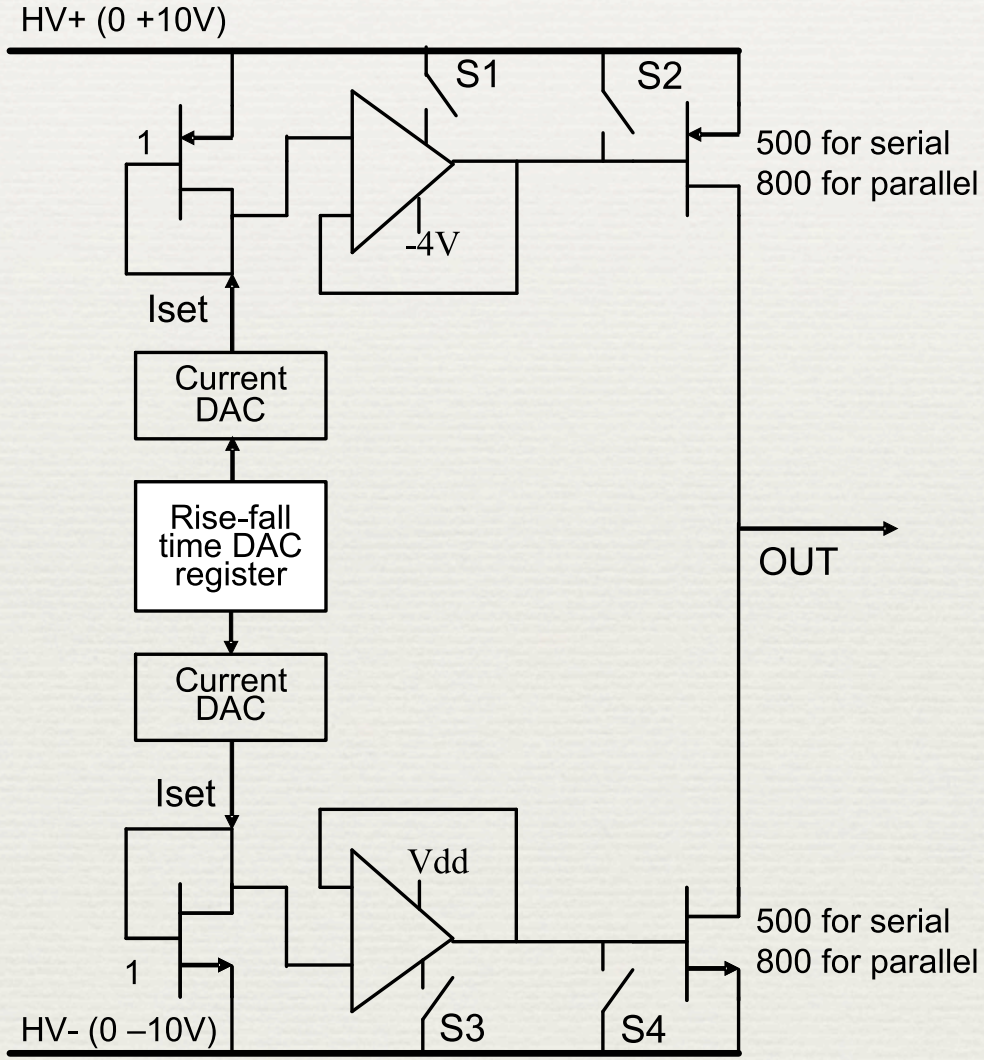
Clock driver details

When the programmable discriminator senses a low output voltage the current source and output transistor are enabled to re-charge the external capacitor which provides the rail for the clock drivers

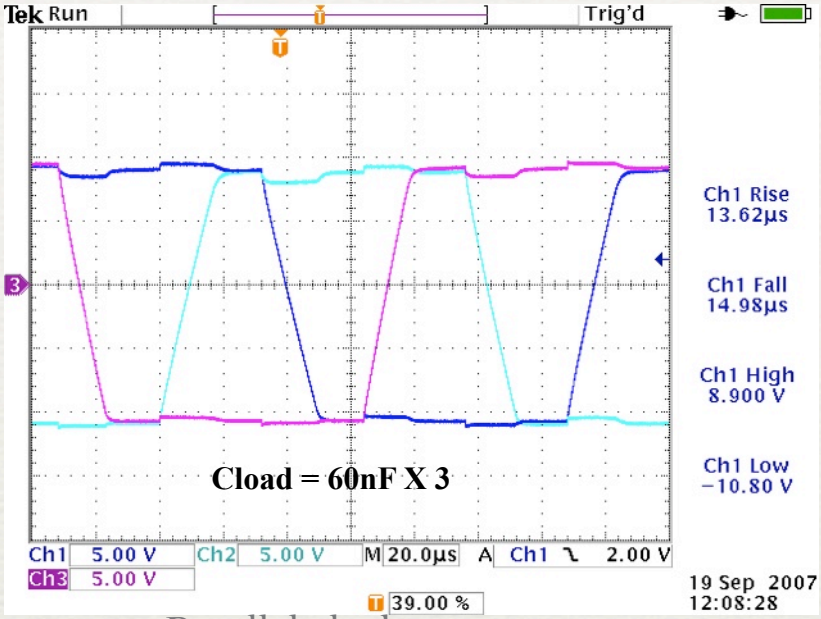


Details continued

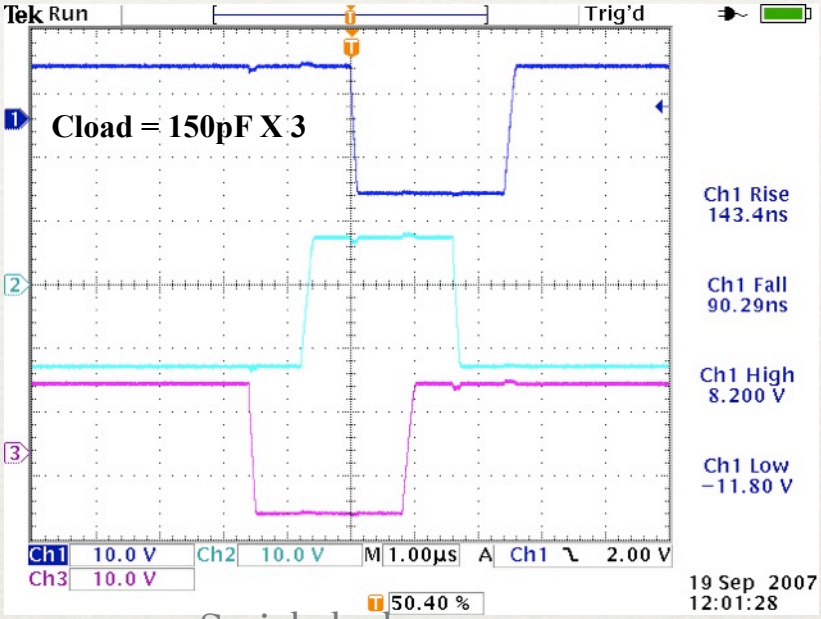
- The clock driver is powered during transitions only. (S1, S3)
- The programmable current mirror provides a linear voltage ramp.
- During the high phase the low-side drive transistor is turned off, and vice versa. (S2, S4)
- The gate capacitance of the output transistor maintains the ‘On’ state after the transition



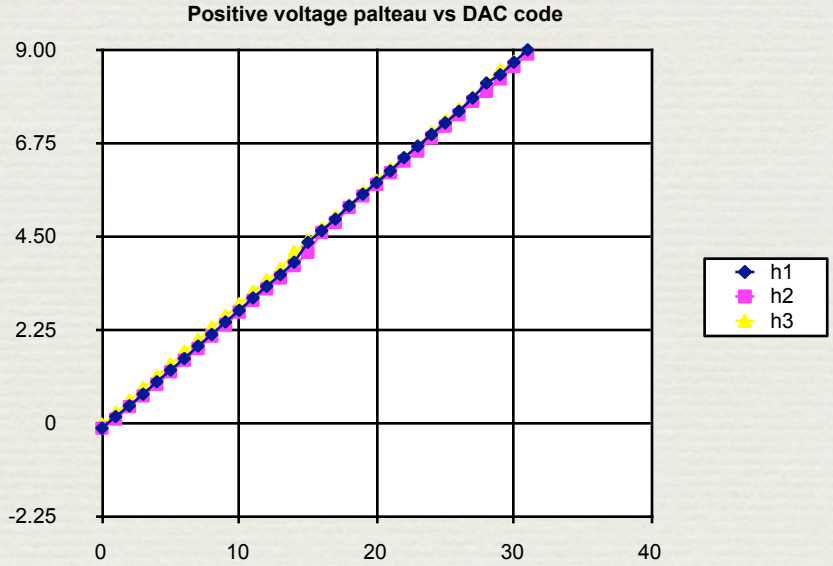
CLIC clocks (300 K)

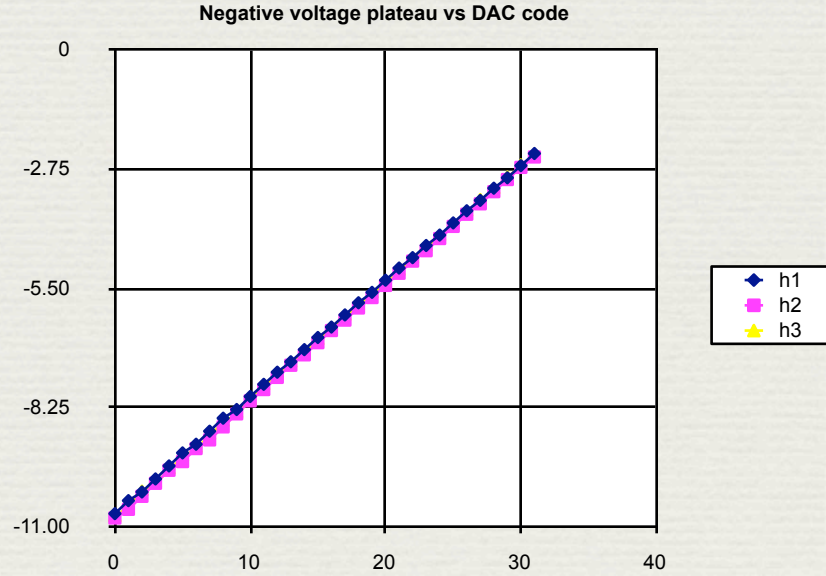


Parallel clock sequence

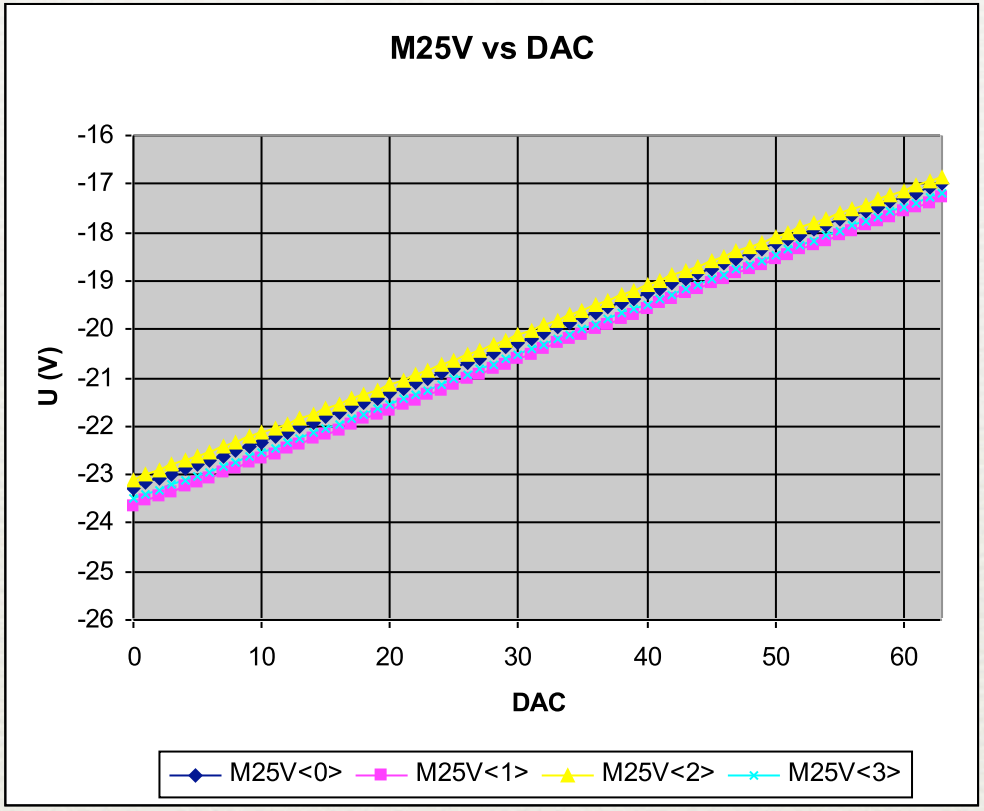


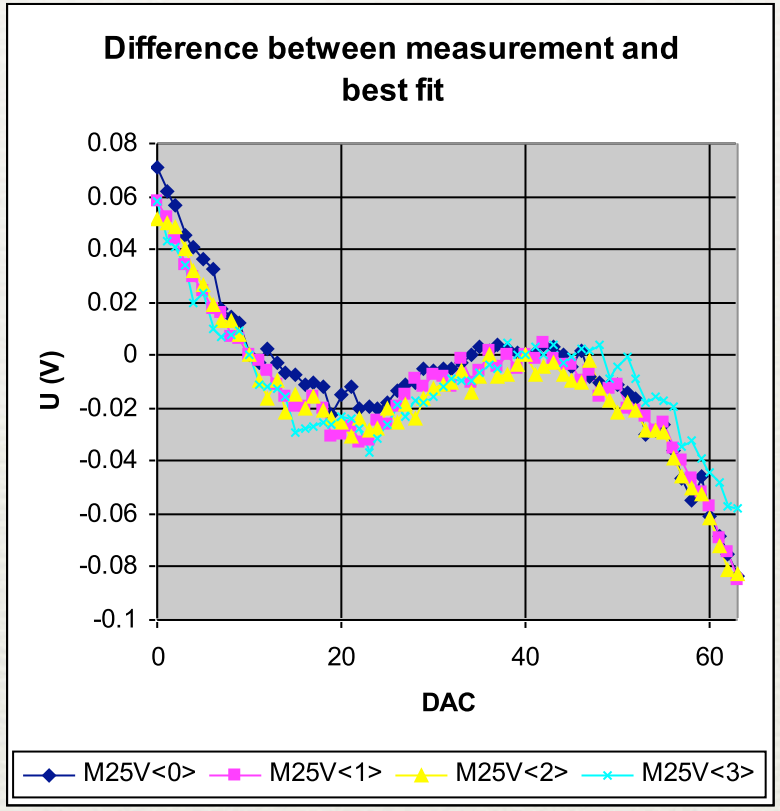
Serial clock sequence





Bias DAC linearity





- Offset dispersion is understood and will be corrected
- Linearity is acceptable (~0.5 LSB INL)

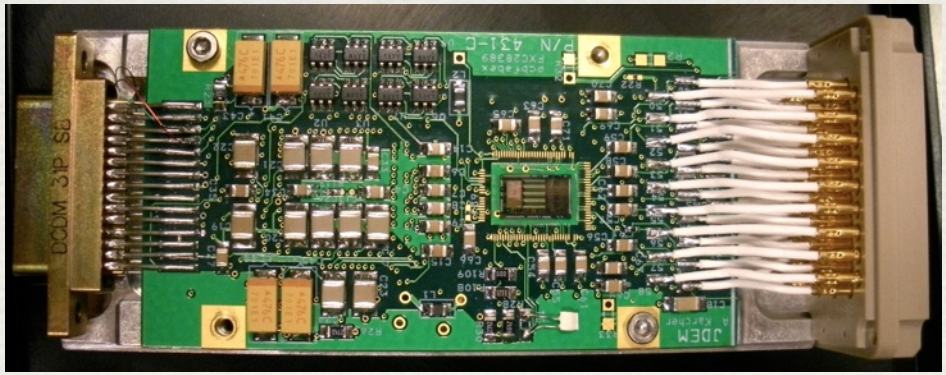
Power consumption

- One of the main goals of the CLIC development is to minimize power consumption.
- The previous, fully tested version is the proof of principle incorporating all necessary functionality.
  - 450 mW during normal CCD read-out.
  - Many voltages can be disabled during exposure, greatly reducing average power.
- Optimization of the digital clock tree will dramatically reduce digital power. (~ ¼)
- Implementation of a band-gap reference instead of zener diodes for all voltage DACs is one of several measures taken to further reduce power in the next version.

Noise issues

The main draw back of the previous version of the CLIC chip is a high noise level on the DC bias lines. This is due to a large excess noise component on the poly-2 resistors used for many feedback elements.

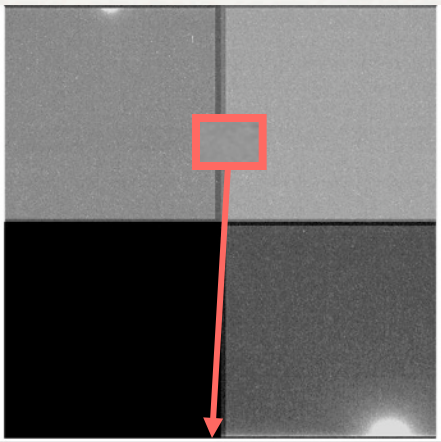
The noise was not properly modeled in the design kit available at the time of chip submission, but has since been rectified. The choice of an implant resistor for the feed back will dramatically reduce noise.

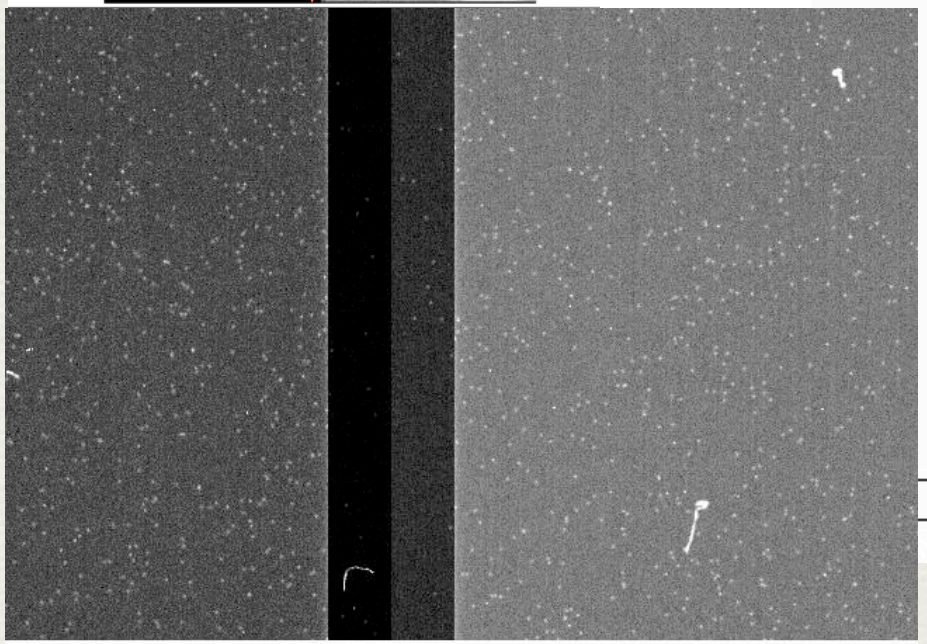


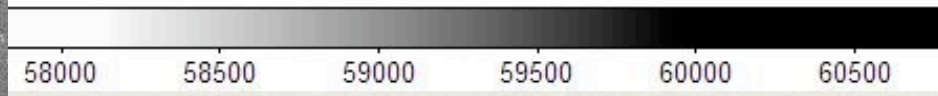
Radiation tolerance

- All flip-flops in CRIC and CLIC have been designed as 'DICE' SEU resistant storage elements.
- No latch-up has been observed in heavy ion testing to LET of 100 MeV/g cm^2.
- Observed SEU rates of 10^{-6} upsets/(particle/cm^2) are most likely due to radiation induced glitches on the asynchronous reset lines (hardened in next version). The current SEU rate translates to less than one upset per chip in ten years in L2 orbit without shielding.

System proof of principle







Conclusion

- We have designed a CCD readout system comprised of two ASICS.
- Preliminary testing of the new version of the clock driver is currently underway. Results are inconclusive, due to fabrication issues at the foundry potentially impacting yield.
- This version of the Clock driver and bias generator is expected to enable a very compact, low noise ($2e^-$) low power (~40 mW/channel average) readout system.

Outlook

- Higher speed
- More channels
- 16 Channel 1MHz readout IC (FCRIC)
  - Proof-of principle exists