JDEM Readout System Development At SLAC for Cold SIDECAR and more

Philip Hart
SLAC
15 Oct 2009

Gunther Haller, James McDonald, Sergio Maldonado, *Aaron Roodman, Leonid Sapozhnikov, Andrew Wagner, et al.

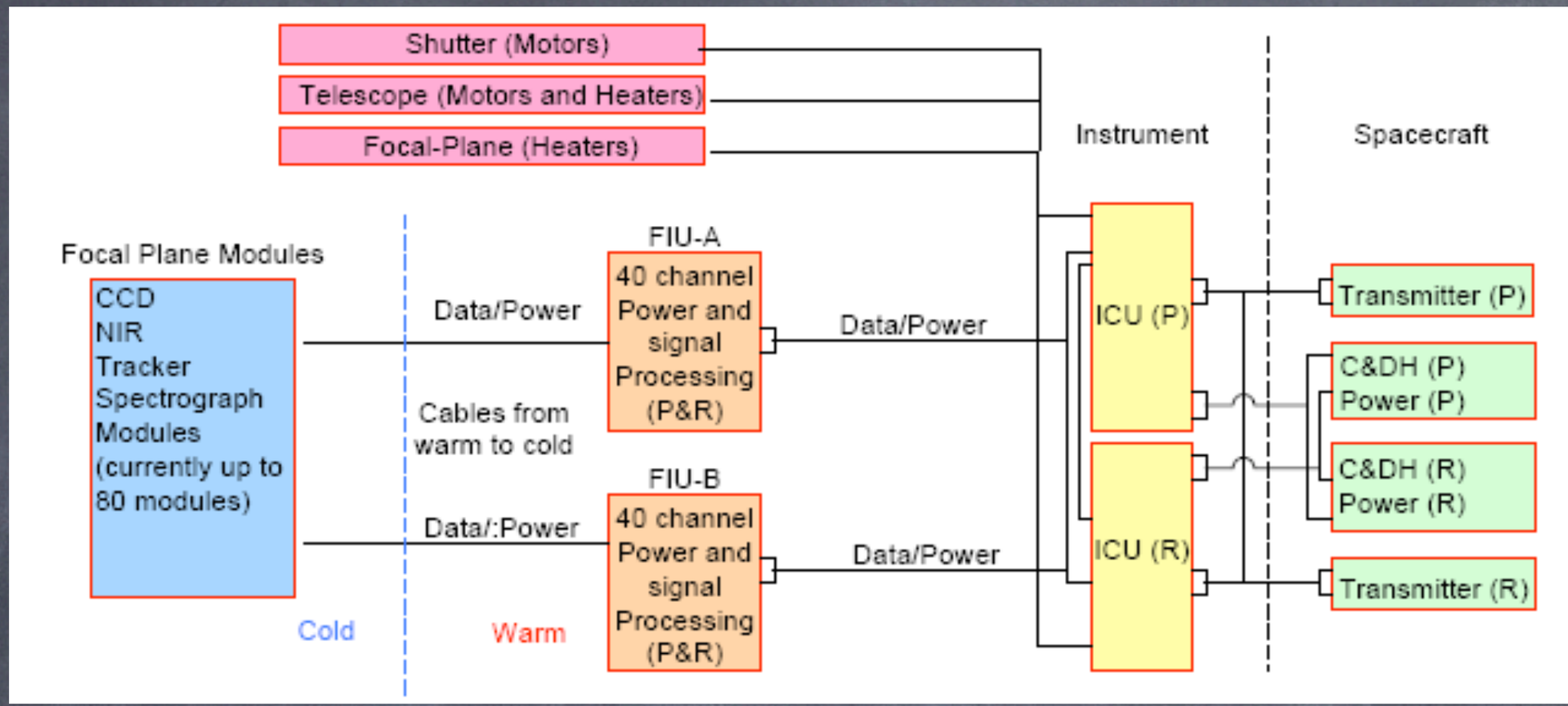
with assistance/consultation from Teledyne; also Markury Sci., Lance Simms, SNAP NIR group

Topics

- SLAC EGSE and experimental setup
  - design <- FERMI (GLAST) heritage
  - hardware
  - interfaces
  - SIDECAR configuration
- First cold SIDECAR data using the EGSE
  - Linearity, PTCs, curiosities/problems
  - Noise studies
    - 32-channel vs 1, noise(gain)

SLAC EGSE

- Complete out-of-the-box SIDECAR etc controller and readout system
  - linux box, cPCI crate w/processor and comm. board, cables
- Throughput ~detector limited for one SIDECAR, ~2.4 MB/s for FSIM
- Extensive GUI interface for easy development
- Python scripting for acquisition/analysis
- Serial device control
  - power supply array, motion stage (guider studies), ...
- In use at Berkeley, Lyon, Michigan
  - active development based on experience

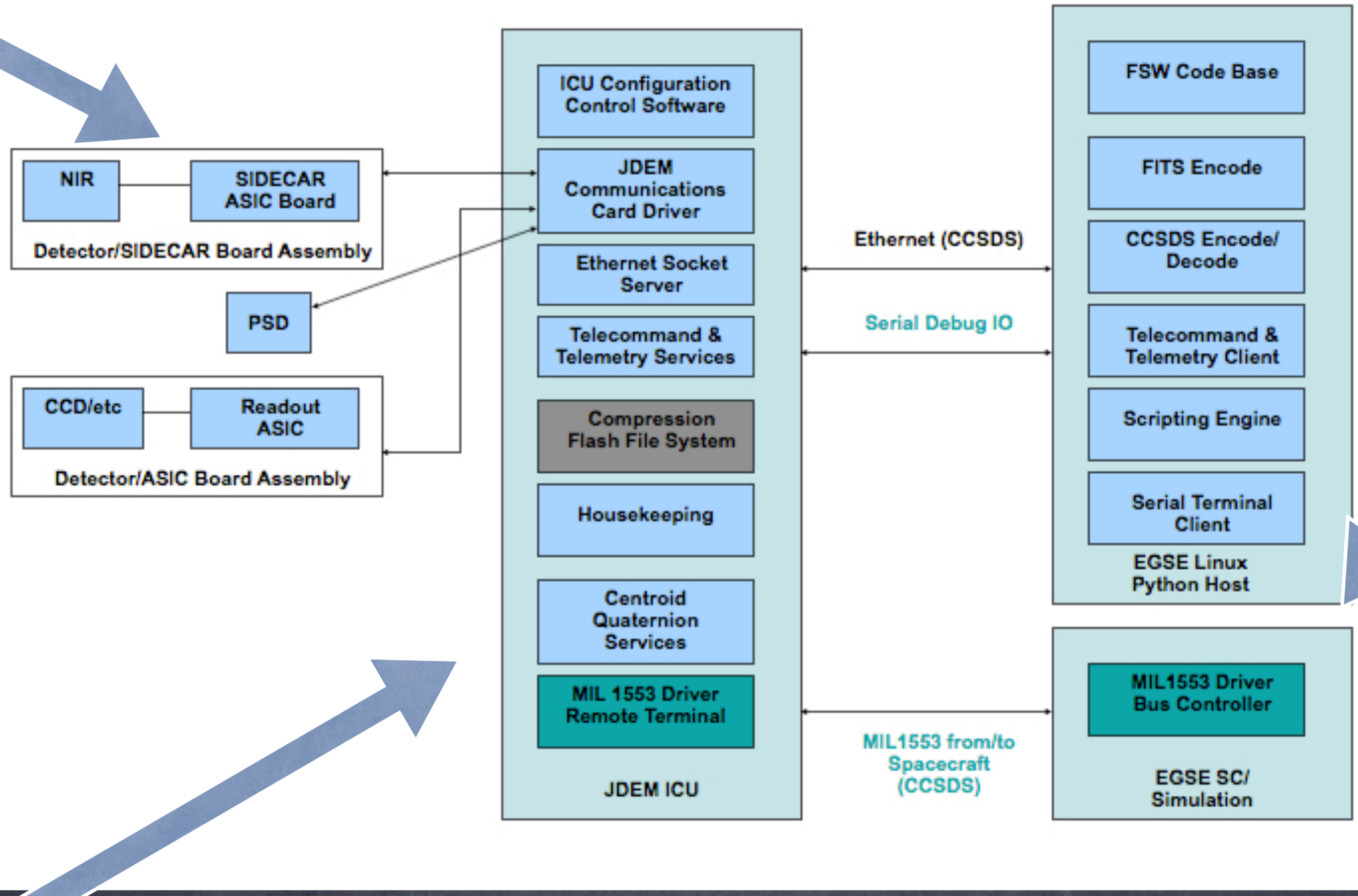


Focal plane Interface Unit
- Signal fan-out and data fan-in
- CCD single-image readout (30sec) & buffering
- NIR fowler/up-the-ramp processing
- Power distribution

Instrument Communication Unit
- Receive data stream from FIUs during 300 sec
- Compress data (in CPU)
- Store in Flash Memory modules
- Transmit to ground during ground contact

SNAP design

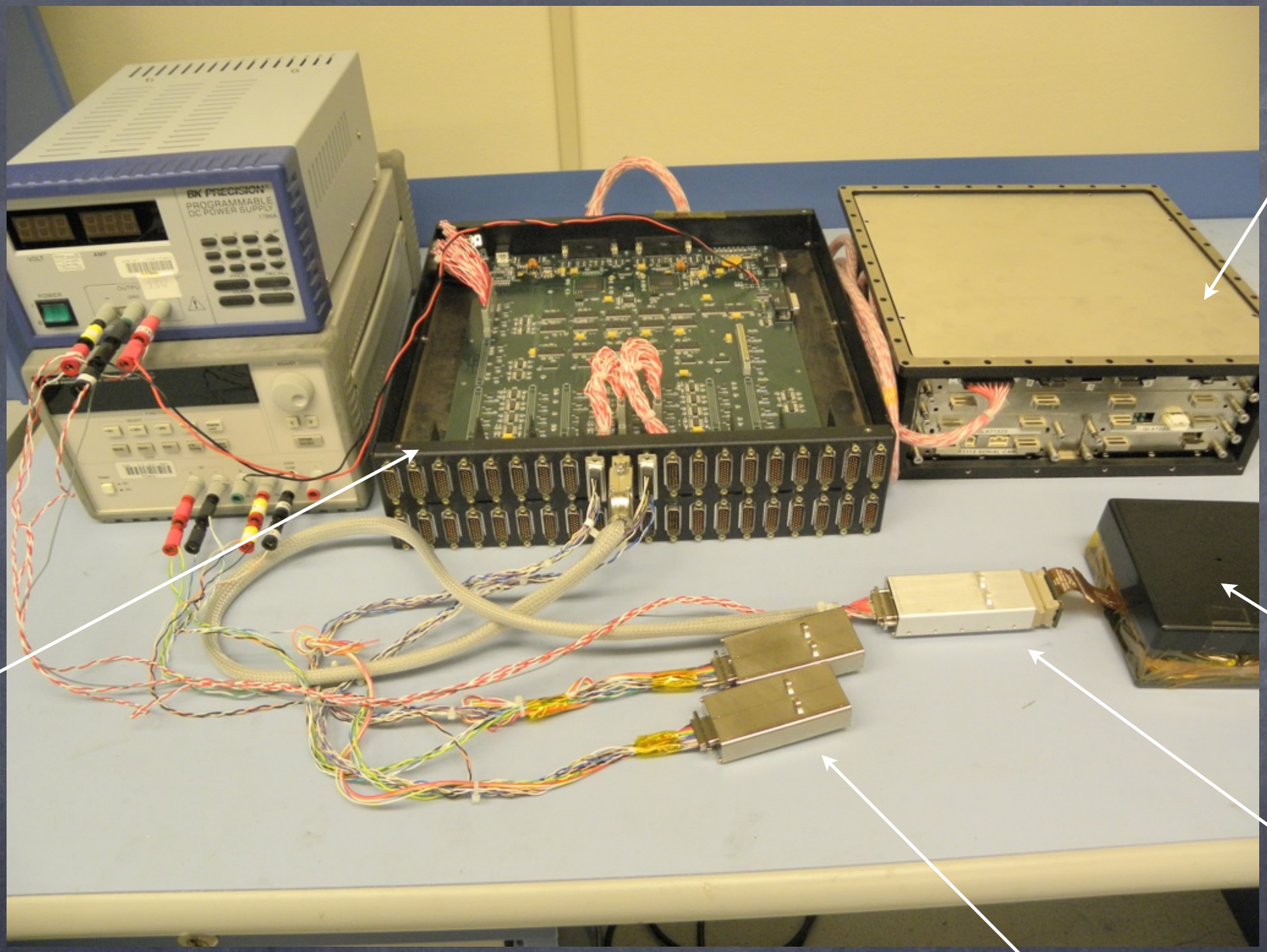
optional FSIM



SLAC EGSE diagram

MCP/RAD750 + custom hardware, VxWorks, custom modules w/FERMI heritage

linux, C/python, custom modules w/ FERMI heritage



ICU - RAD750, communi-cation board

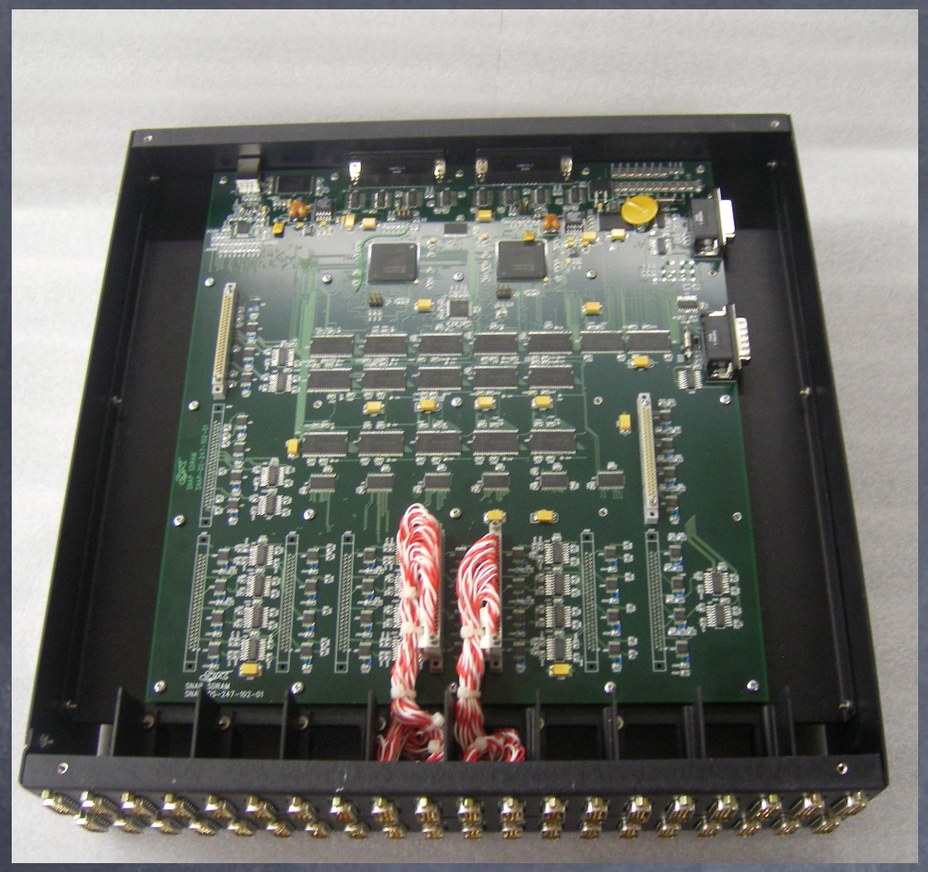
Bare H2RG

FSIM - routing, fanout, buffering, preprocessing

SLAC package w/ SIDECAR

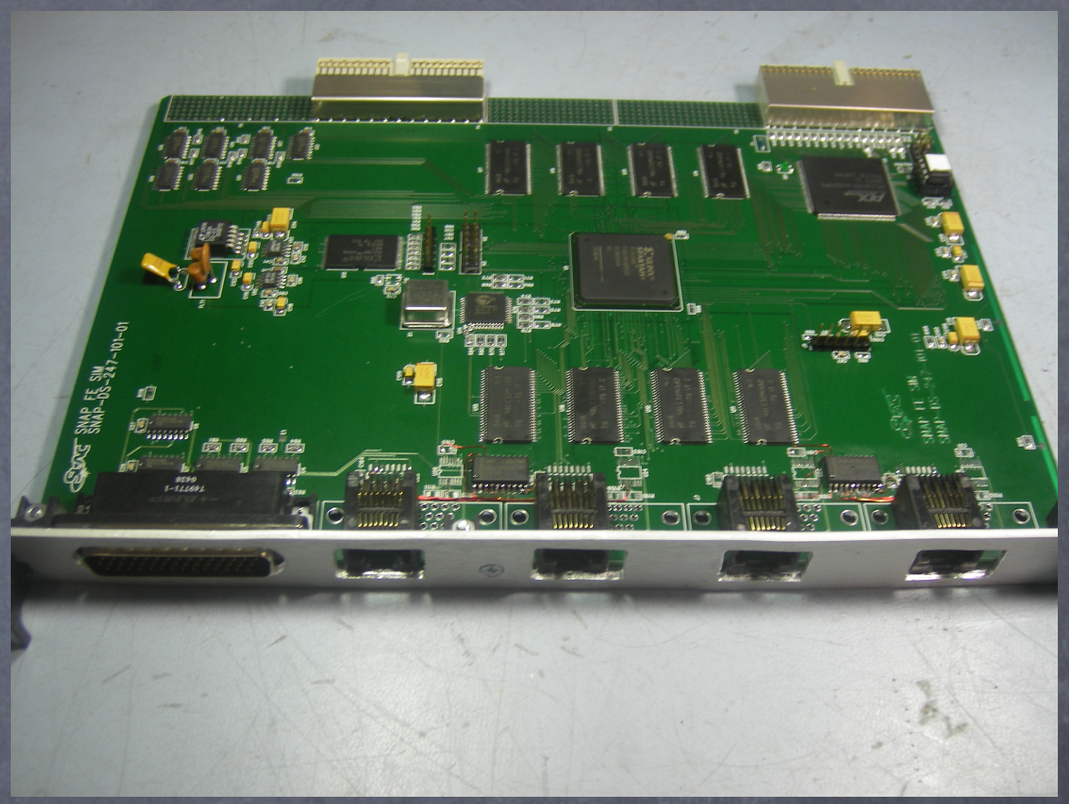
LBNL CRIC/CLICs

Flight-like-like test setup



connectors for 8 of 40 front-end modules

Instrument communication module

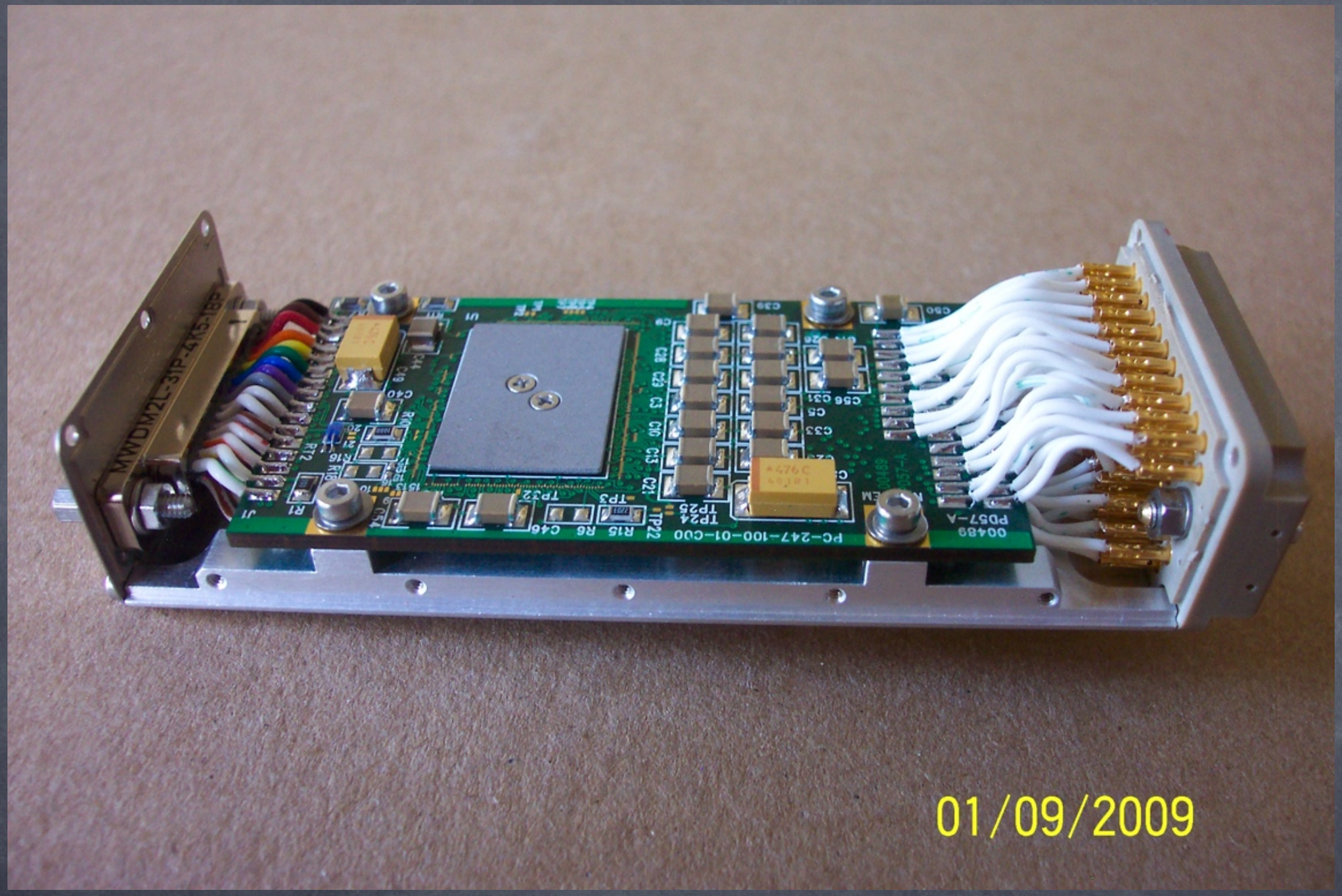


Talks to focal-plane module over serial LVDS,
access to front ends via cPCI, memory, ...

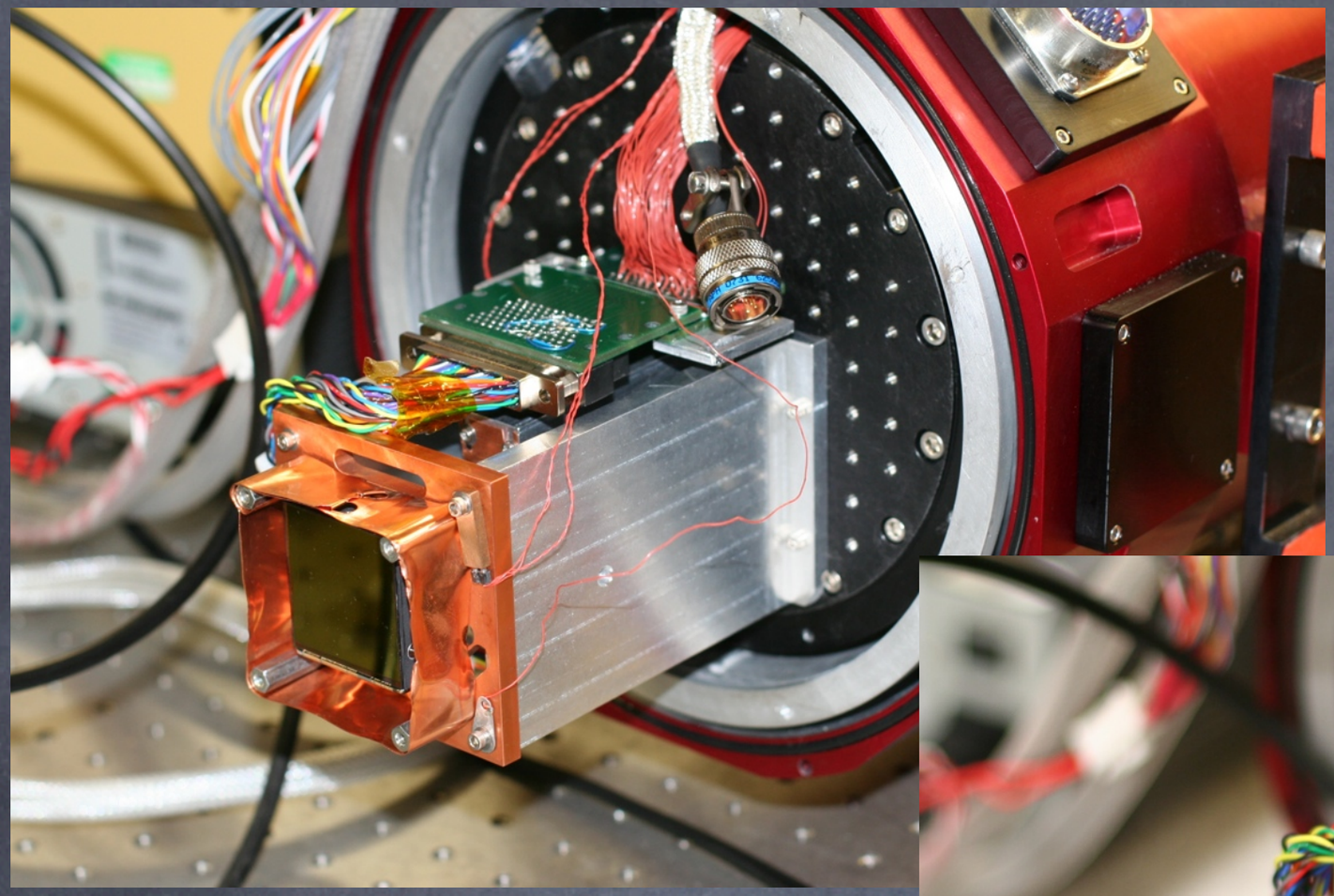
SLAC JDEM prototype boards

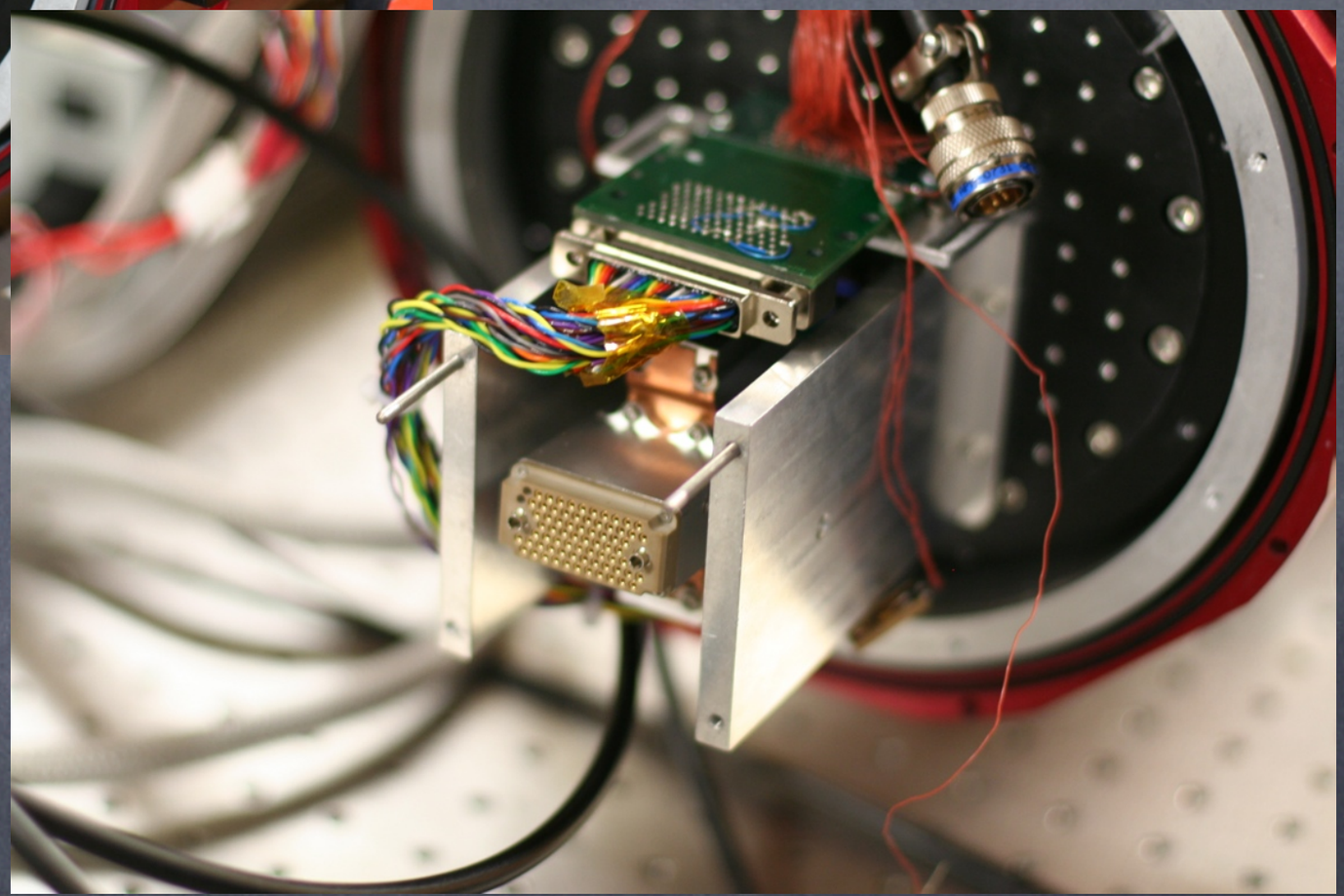
FERMI Heritage

- all core components of the EGSE have GLAST heritage
  - embedded hardware/software plus host side tools
- hardware:
  - communications board <- GLAST comm. board (plus driver model)
  - RAD750 experience
- embedded software
  - for 750, board support package, OS, messaging, 1553 connectivity reused
  - proxy package <- socket code
- Host tools:
  - code management, standards, architecture reused
  - command/telemetry packet creation/management reused
  - GUI/python scripting <- GLAST test executive toolset

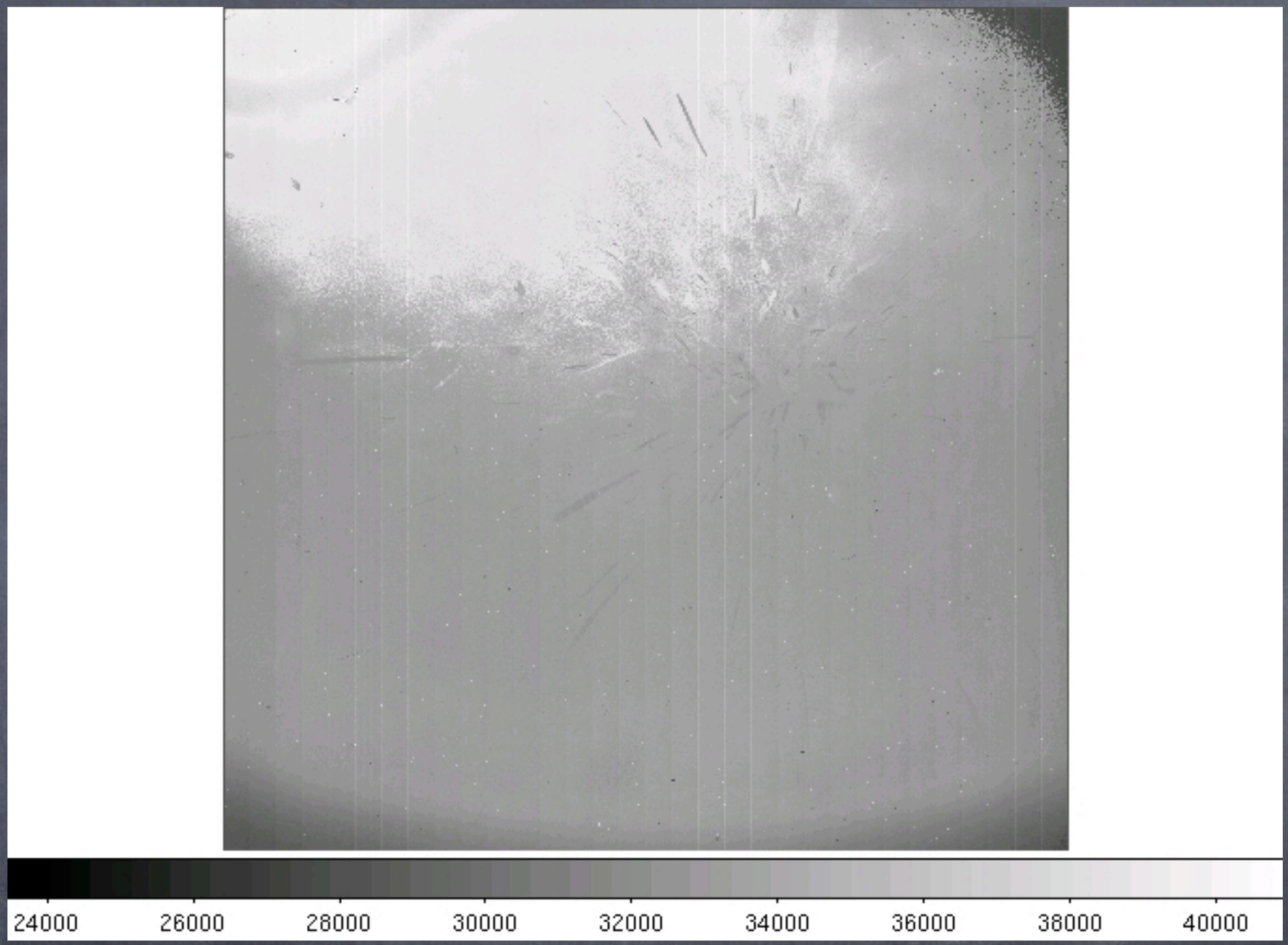


SLAC cryo package for SIDECAR (JDEM prototype)



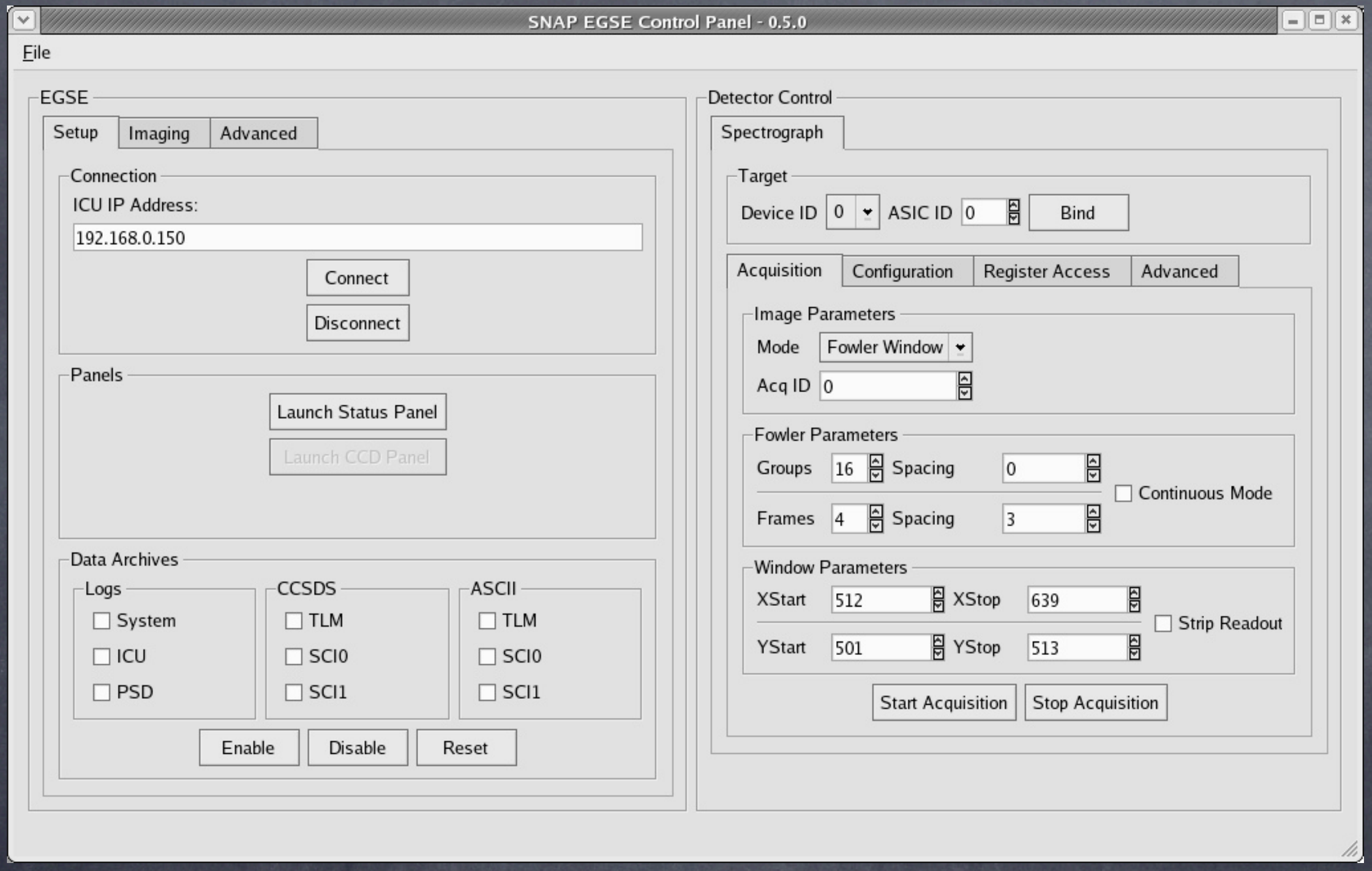


NIR/H2RG, SIDECAR



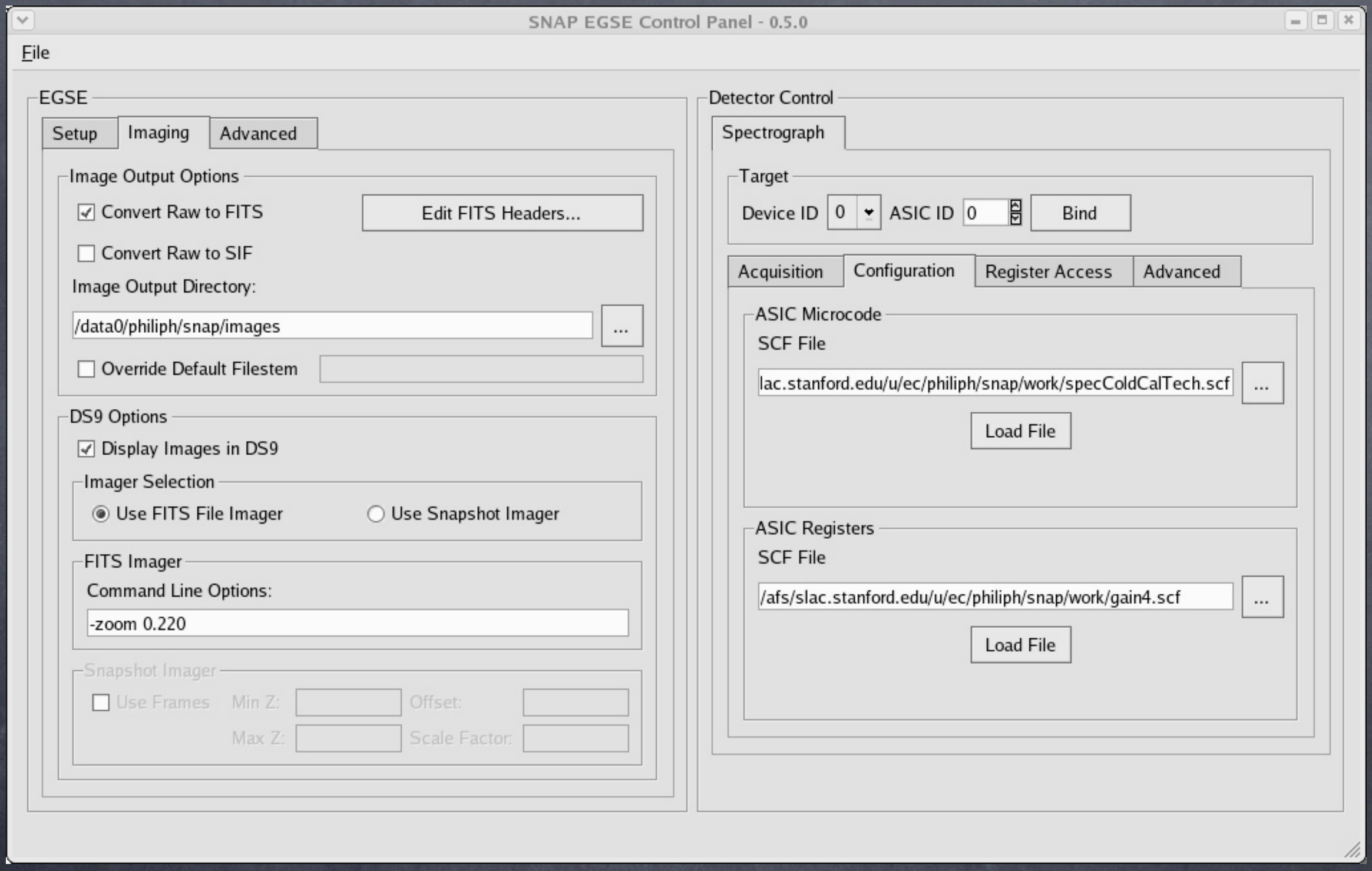
Upper half of detector has high dark current; using center of lower half for studies

H2RG-SNAP141-IR17-LBNL
(not a representative detector - used to test our readout system, not v.v.)

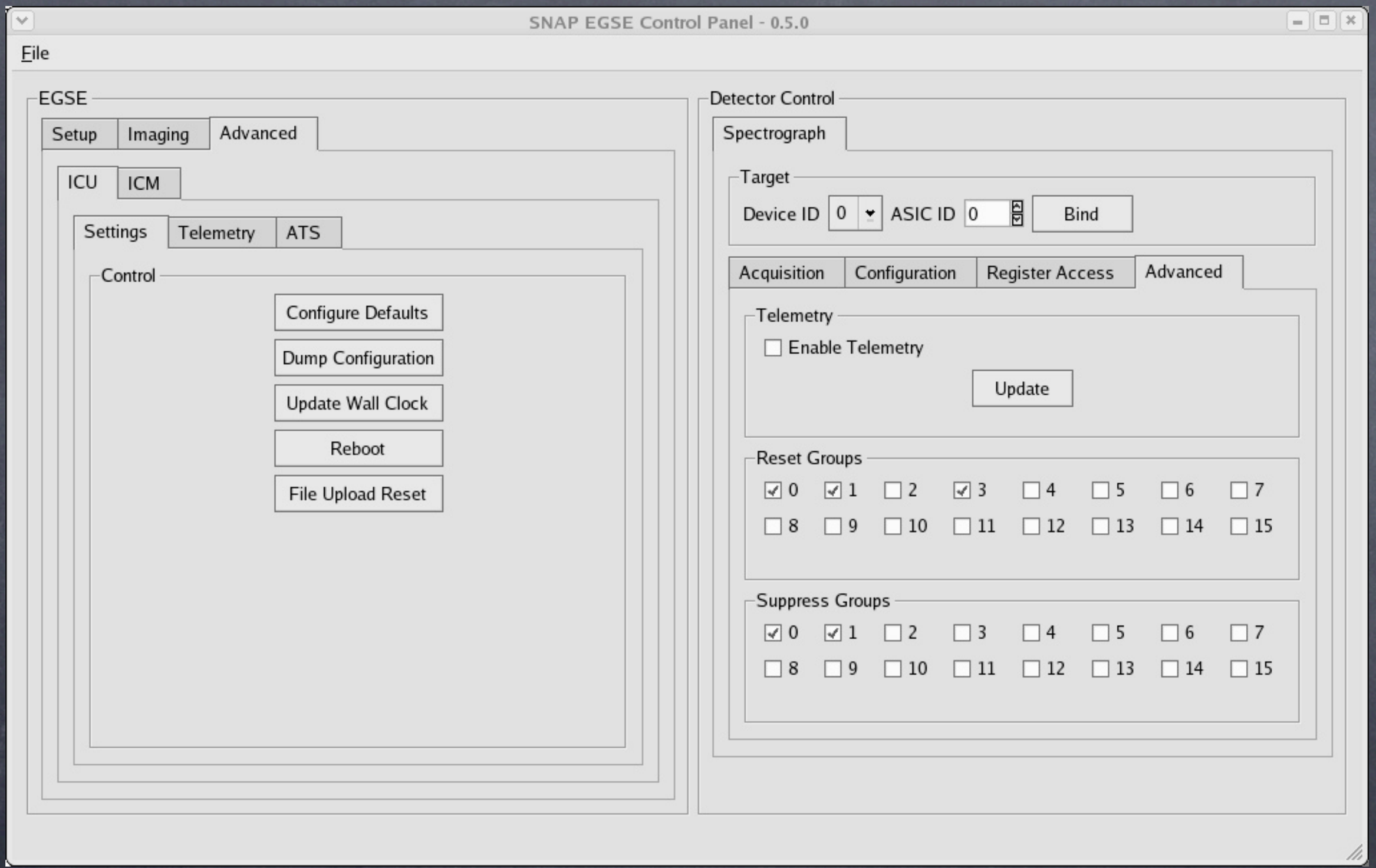


GUI:
Telemetry, (SIDECAR) acquisition

py/qt



Imaging, config controls



Expert, group/frame control

Python scripting

- import Proxy; proxy = Proxy(SNAP_ICU_IP,raw=0,txt=0); proxy.tlm.enable_archive(0,1); proxy.connect(); proxy.cfg_nir('myConfigFile')
- for i in range(20): for j in range(400):files[i, j] = proxy.acquire_nir(grps=2, supr=0, frmt=j, rst=0, wait=1, winmode=2, ystart=501, ystop=512, tranid=0)
- import numpy; for i...; for j ...: fowlerA = utilities.diffArray(files...); fowlerB = ...
  - signal.append((fowlerA+fowlerB)/2).mean()); rms.append(fowlerA+fowlerB).std())
- import Graph; g = Graph(signal, rms*rms, "PTC"); g.makeGraph()

SIDECAR configuration

- SIDECAR science data clocked at 25 MHz
  - processor, ADC at 1 MHz
- Continuously read out H2RG at 100 KHz
- Acquires, ships data according to programmed pattern
  - continuous or in groups with H2RG reset and dropped frames for up-the-ramp, Fowler, ...
- Use global H2RG reset, line-by-line preamp reset with KTC noise reduction
- 32 (full or y-strip), window modes
- tuned warm (shouldn't matter)

SIDECAR config. cont.

- interacts with EGSE via double-buffering
- works in multidevice system (see FSIM slide)
  - allows synching with other devices
- Vref tied to ground for internal temperature compensation
- 60 Hz solved by use of regulated PS, better grounding
  - now using separate supplies for analog, digital because of hint of digital noise

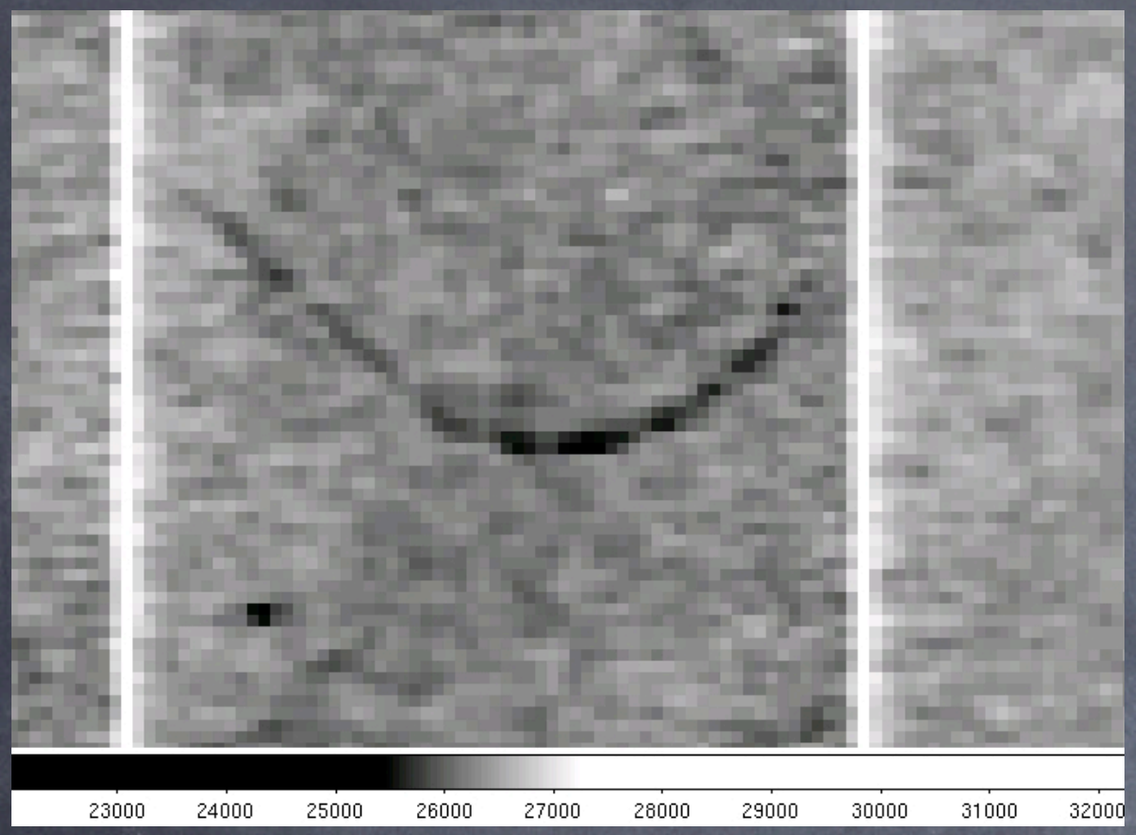
Some teething problems...

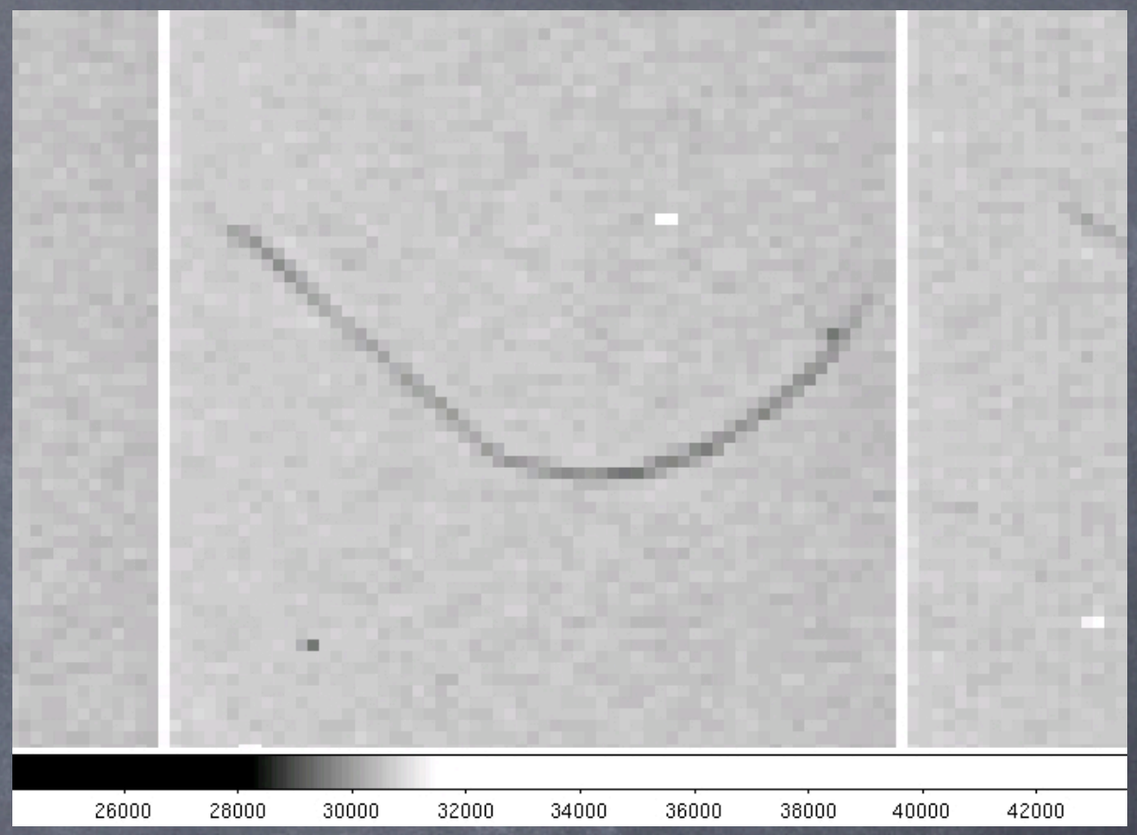
- Along with the usual disk failure, bee in nitrogen line, etc.:
- had to adjust internal timing to read/write science memory for recent SIDECARs (bit flipping problem)
- couldn't ship data from science memory while acquiring at 140 K/25 MHz
  - could read fixed pattern
  - discovered we were using too much current on LVDS
    - LVDS spikes getting into Vdd? (don't have dedicated VDDIO/VSSIO)

Analog bias settings

- For preamps/ADCs and for H2RG
- "Old" internal settings tuned warm plus default H2RG biases: ~0.6 W
- "New" internal settings tuned for cold plus ~Cal Tech H2RG biases: 0.3 W; no output source follower
  - measure electronic gain externally warm, internally with reference voltages and Vreset, all consistent
  - had to adjust Vbiasgate (see below)
  - can't run stably at gain=4(>) w/large signal

"smile" cosmetic

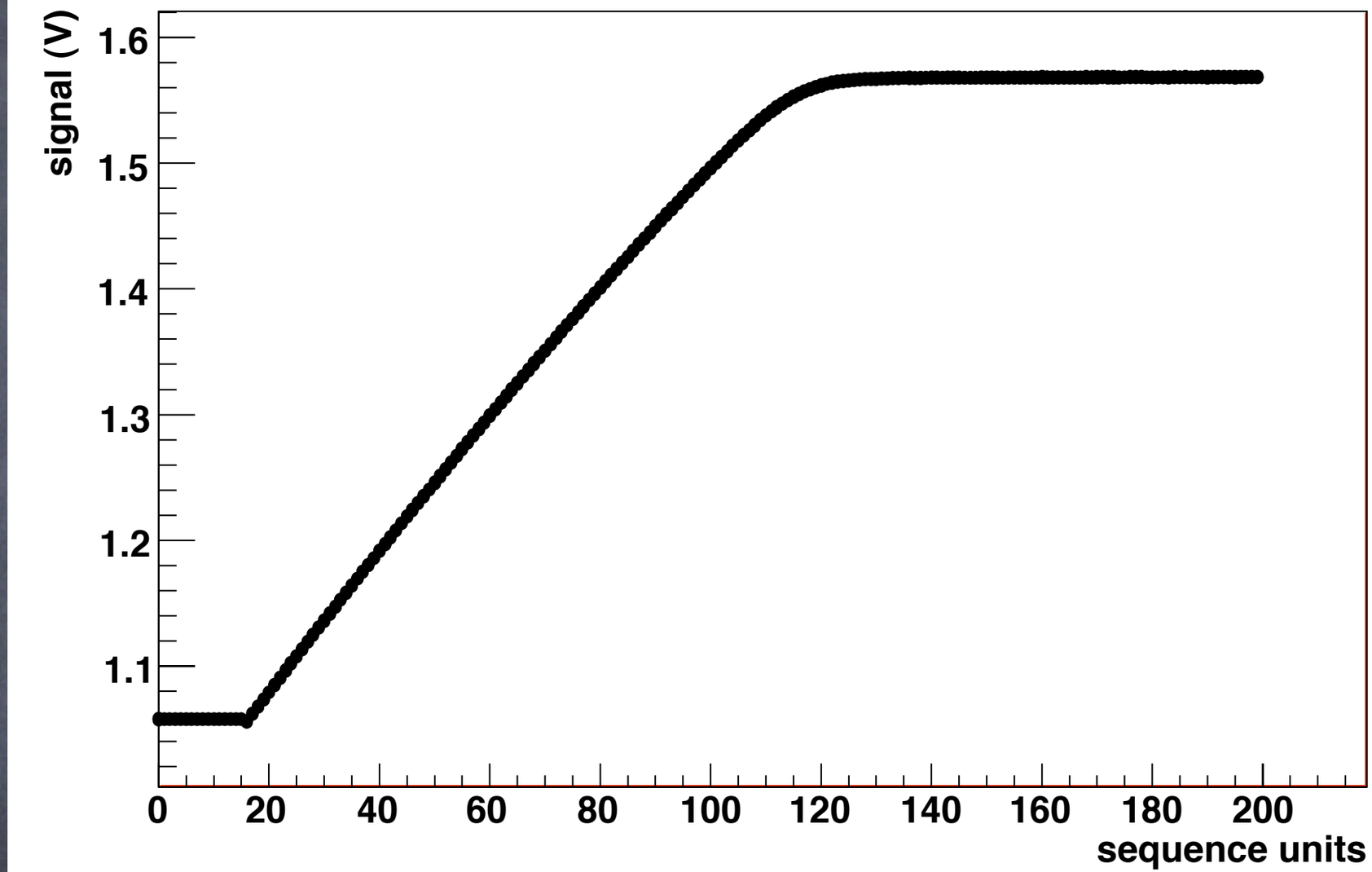




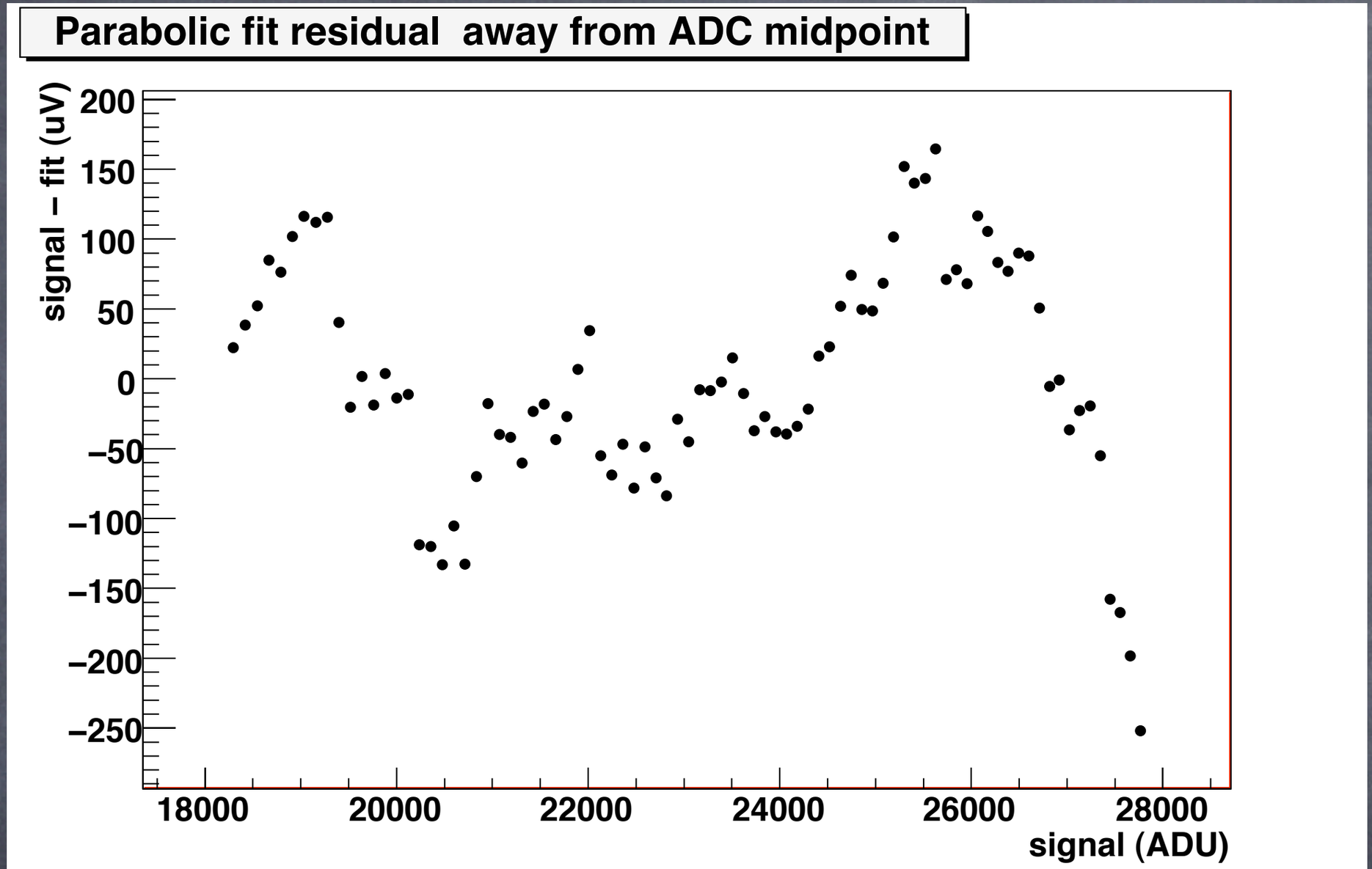
Tuning: adjusted Vbiasgate

Some early data

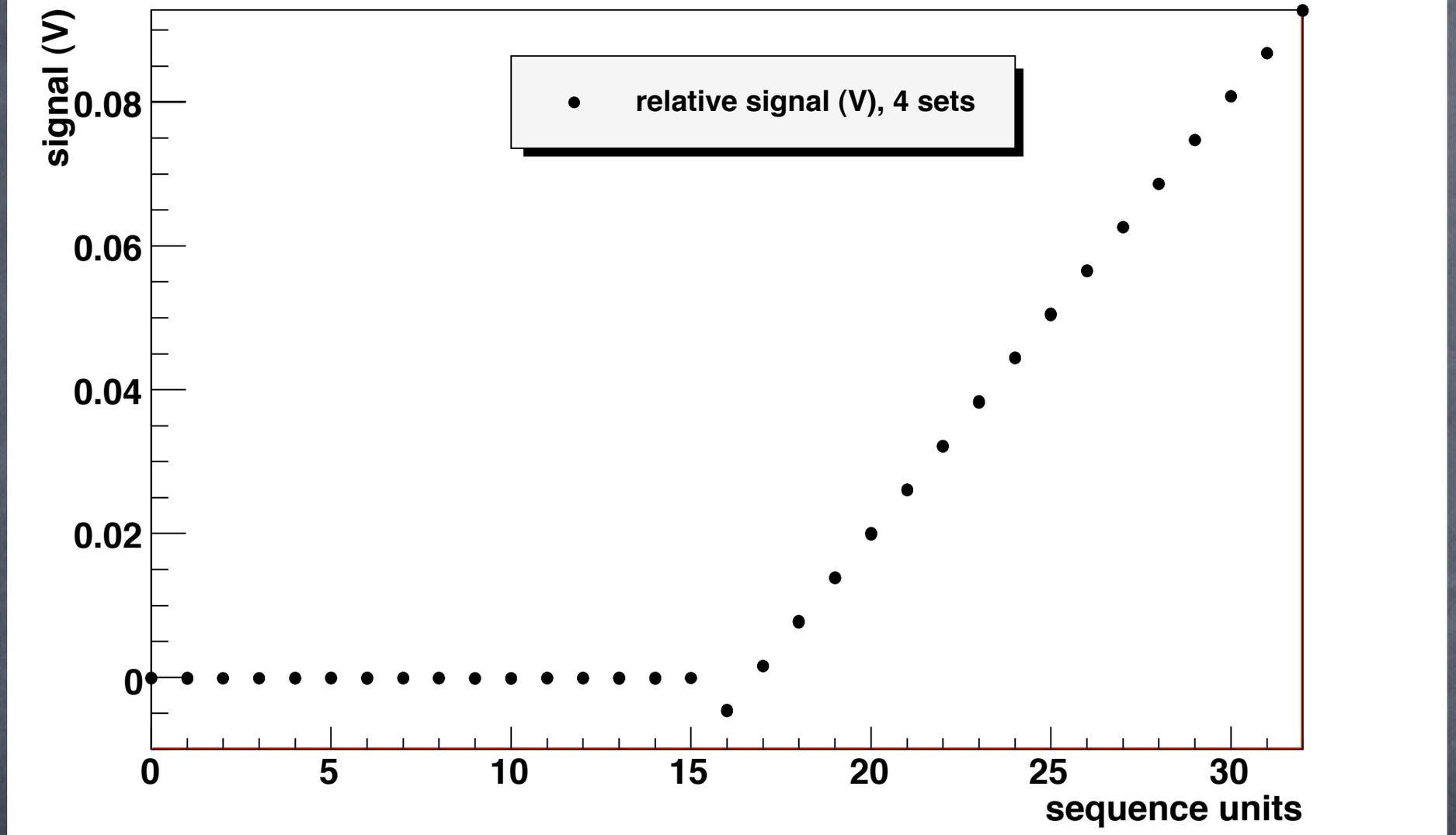
- 'The best way to test your electronics is the way you're going to use it'
  - setting up suite to exercise/test/ understand readout system



Well depth shape


Parabolic fit residual away from ADC midpoint
signal – fit (uV)
200
150
100
50
0
–50
–100
–150
–200
–250
18000
20000
22000
24000
26000
28000
signal (ADU)

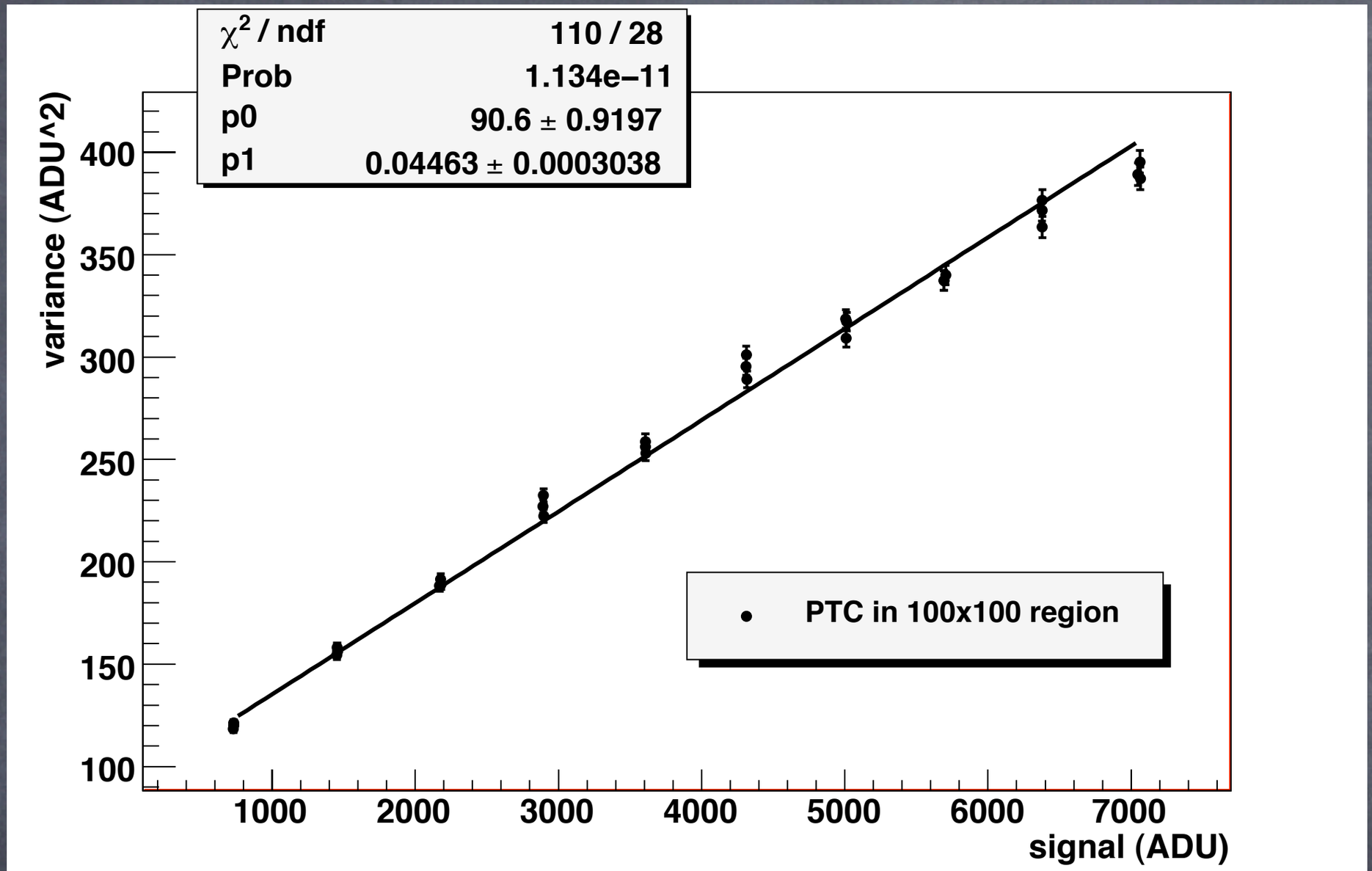
Linearity



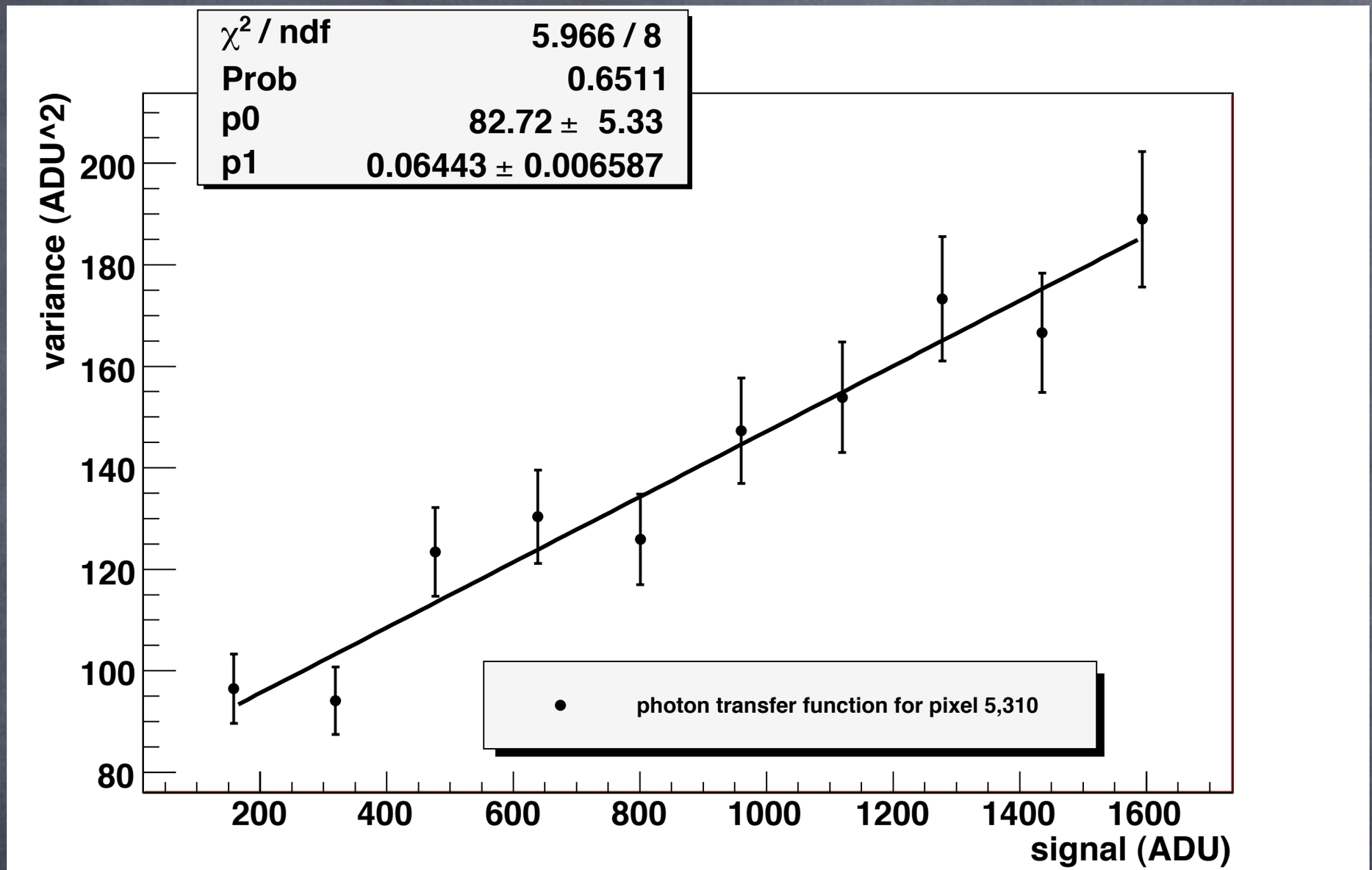
Detector in reset

First non-reset frame

Odd post-reset behavior

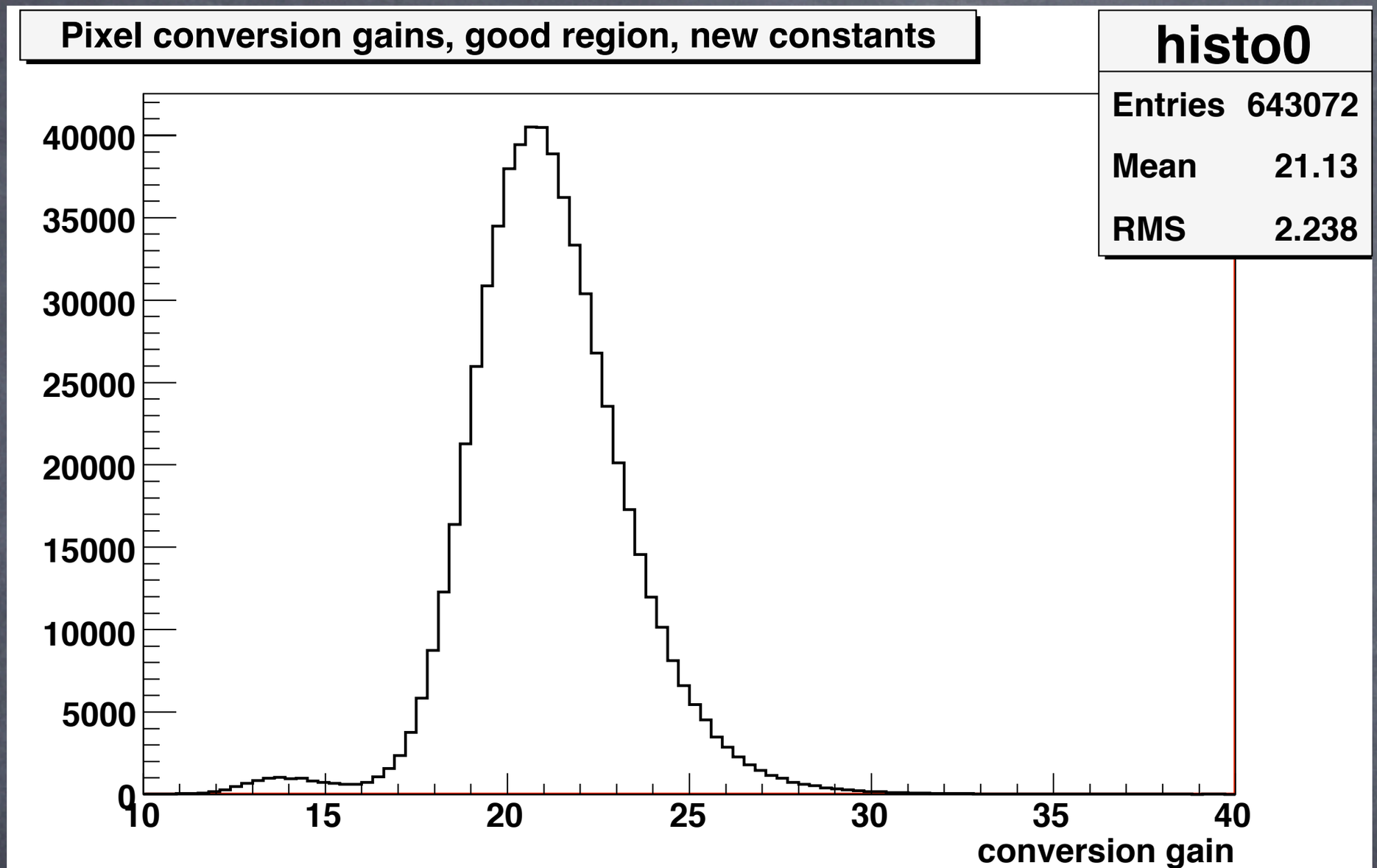


Spatial photon transfer curve



4k fits files - easy to acquire, handle

Sample single pixel PTC



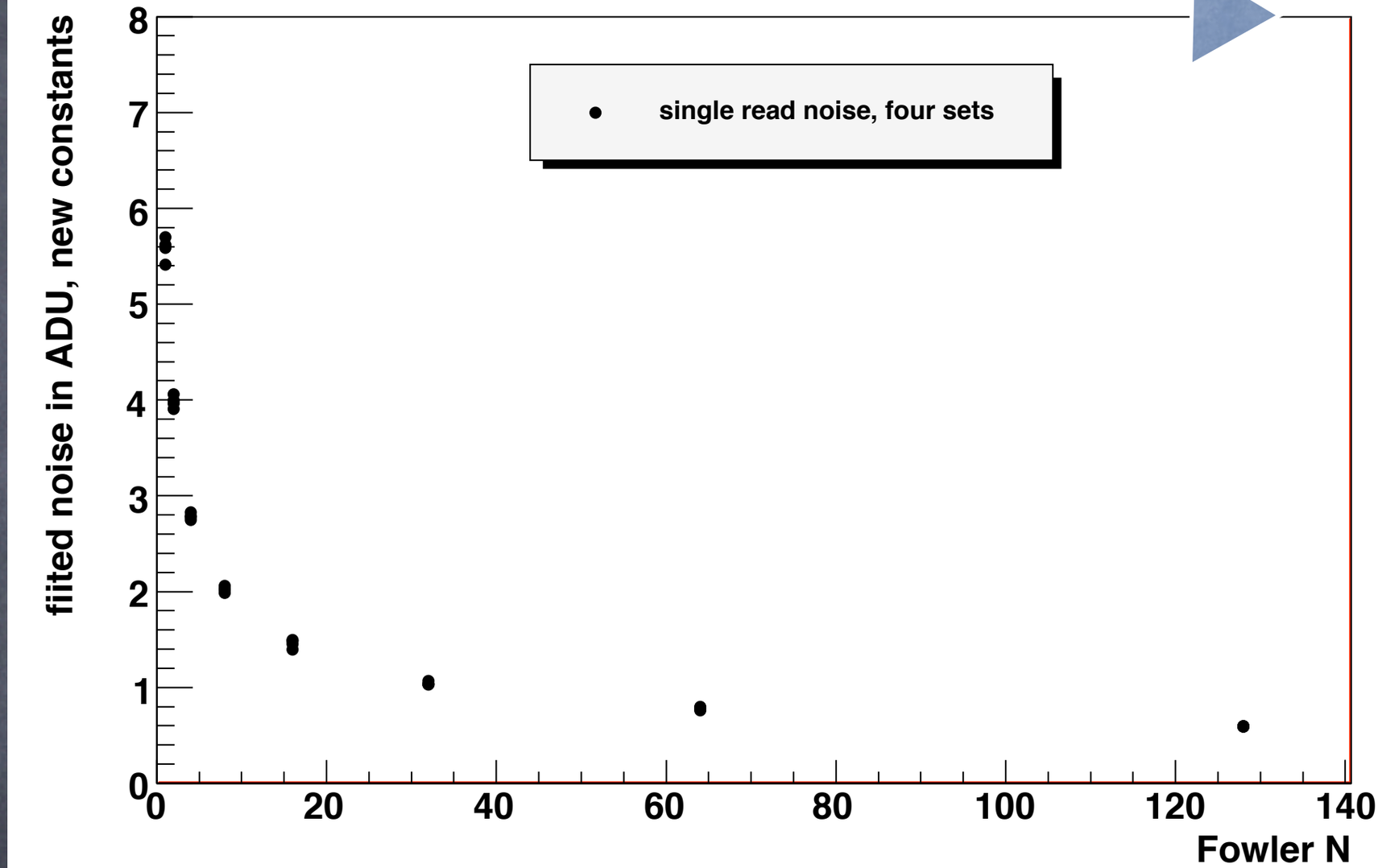
Temporal photon transfer curve results

(agrees with spatial PTC)

Noise studies (prelim.)

- check of window mode vs 32-channel readout noise
  - two-channel wide window vs same pixels in strip
  - measured "dark"
    - switch off unused array processors in window mode to reduce digital noise
    - need to repeat with unused ADCs turned off
- dependence on gain, other configurations
  - -> understand total system noise and behavior
- Always quote single-read noise equivalent below

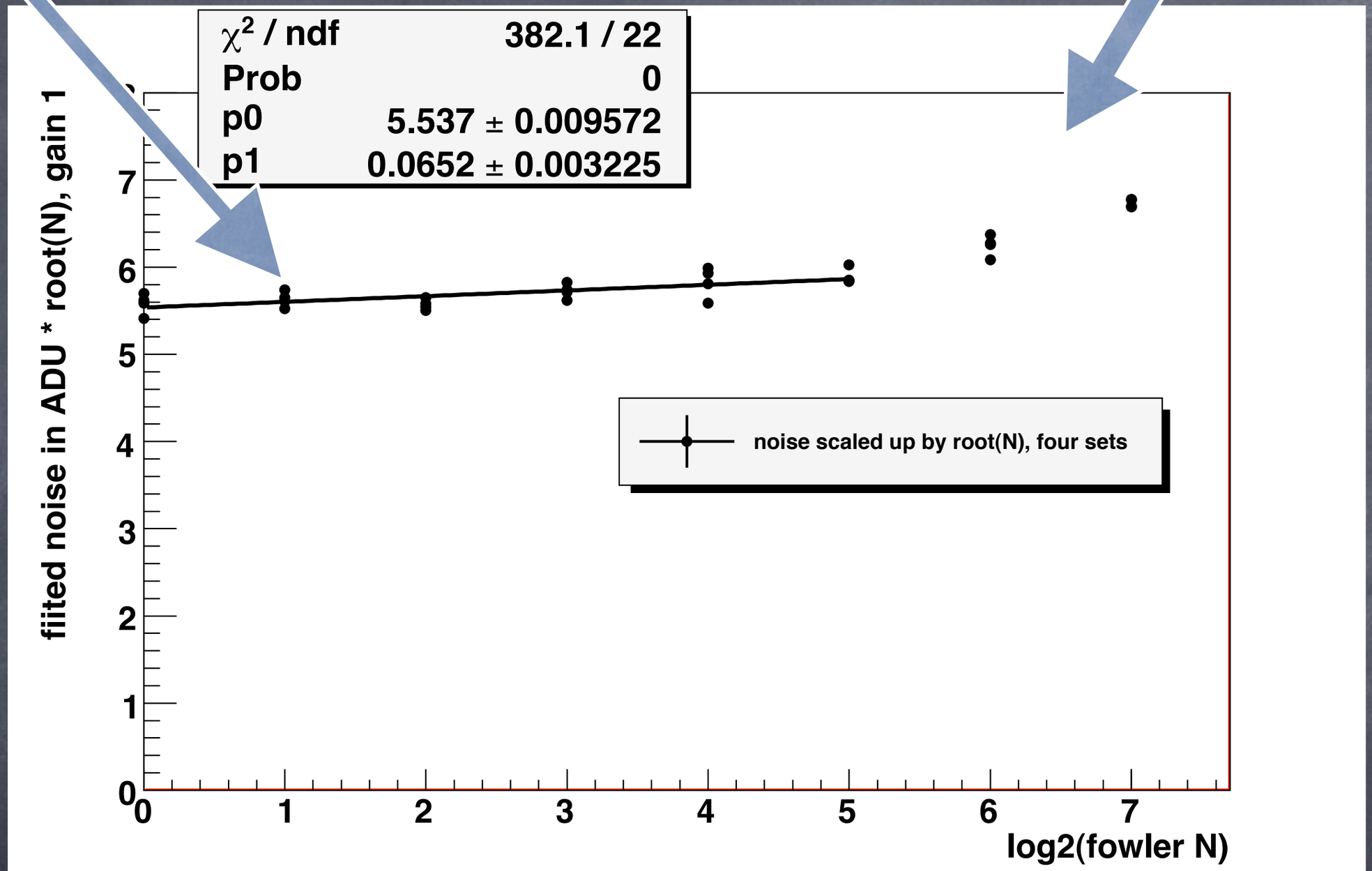
Measured "dark", subtracted average signal



Noise scales as expected with Fowler N
(in good region of detector)

Flat line -> expected scaling

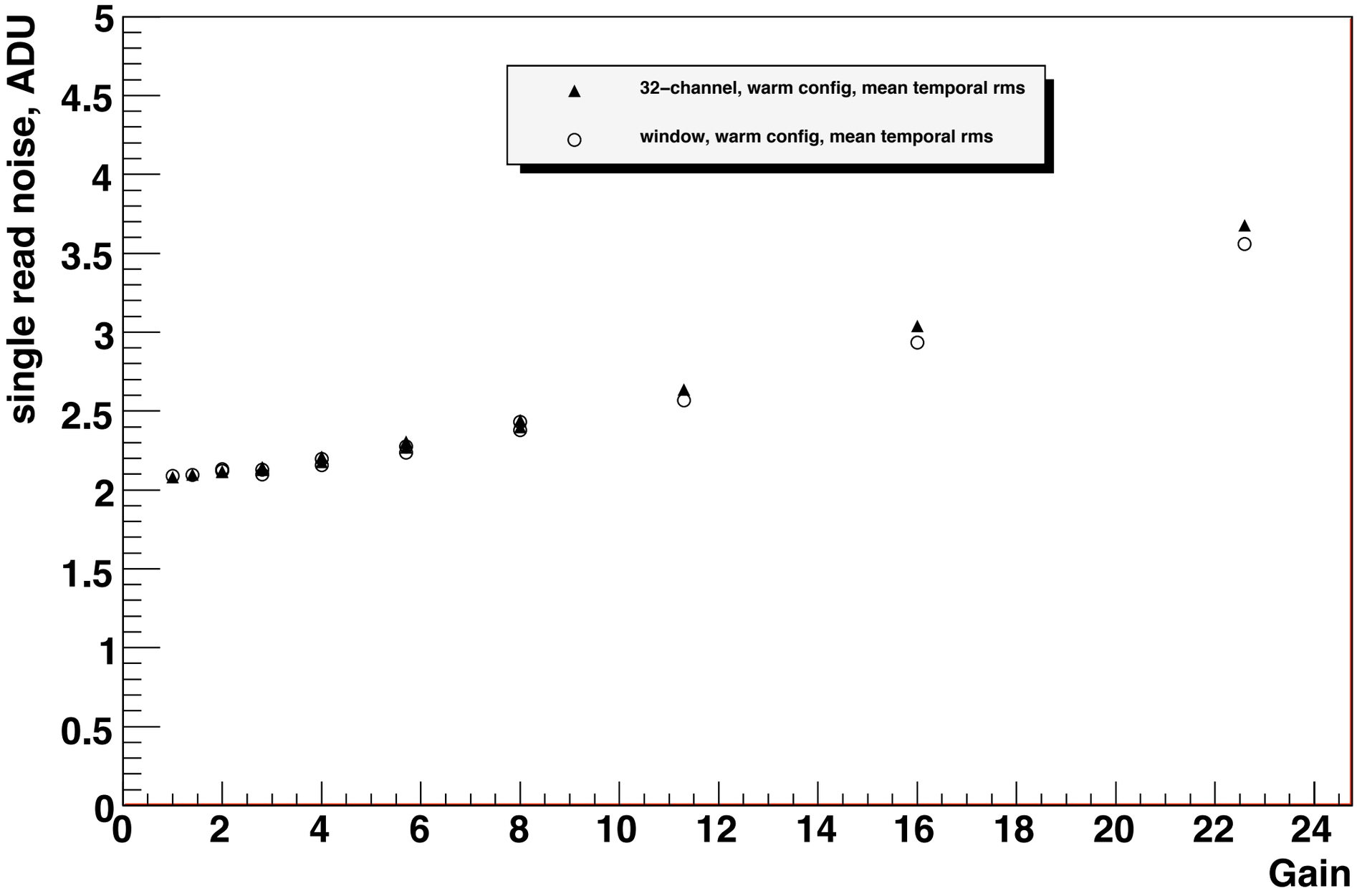
Measured dark, subtracted average signal, but still have some shot noise at high N



Noise scales as expected with Fowler N (in good region of detector)

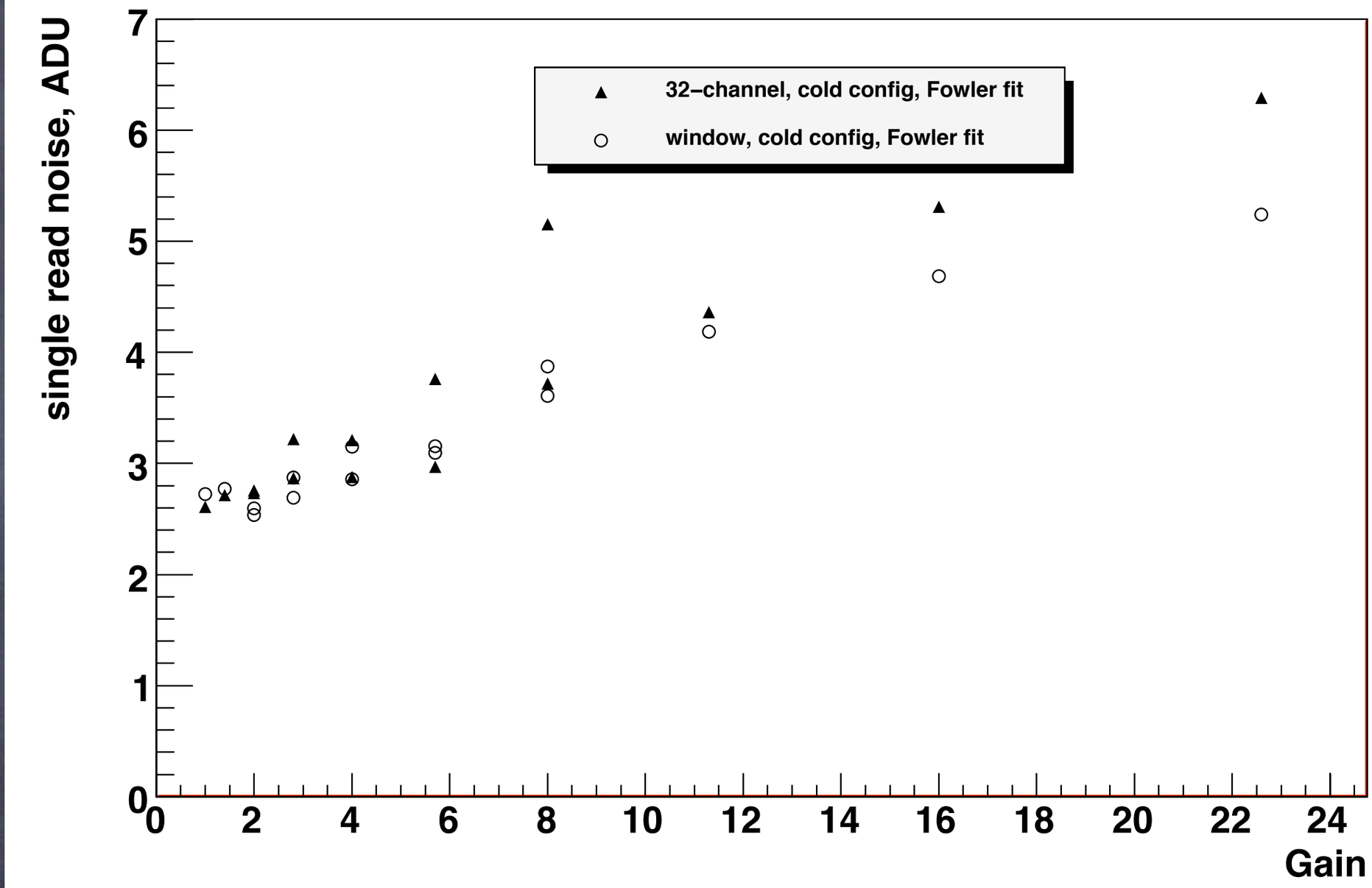
E.g., no apparent heating when shipping data

Noise vs gain, grounded inputs, old constants



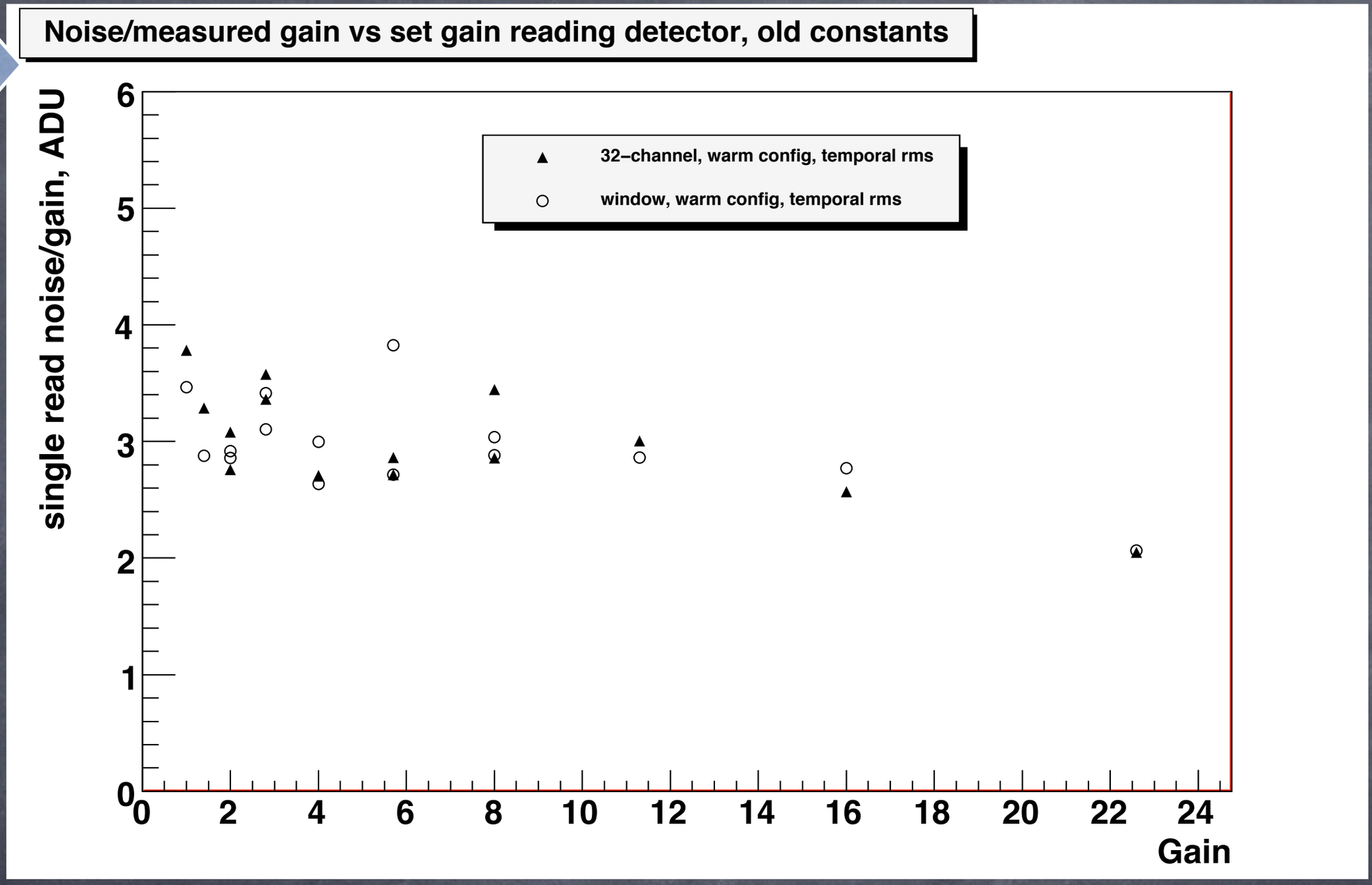
Internal noise in 32-channel mode comparable to single-channel (window) mode with old constants

Noise vs gain, grounded inputs, new constants



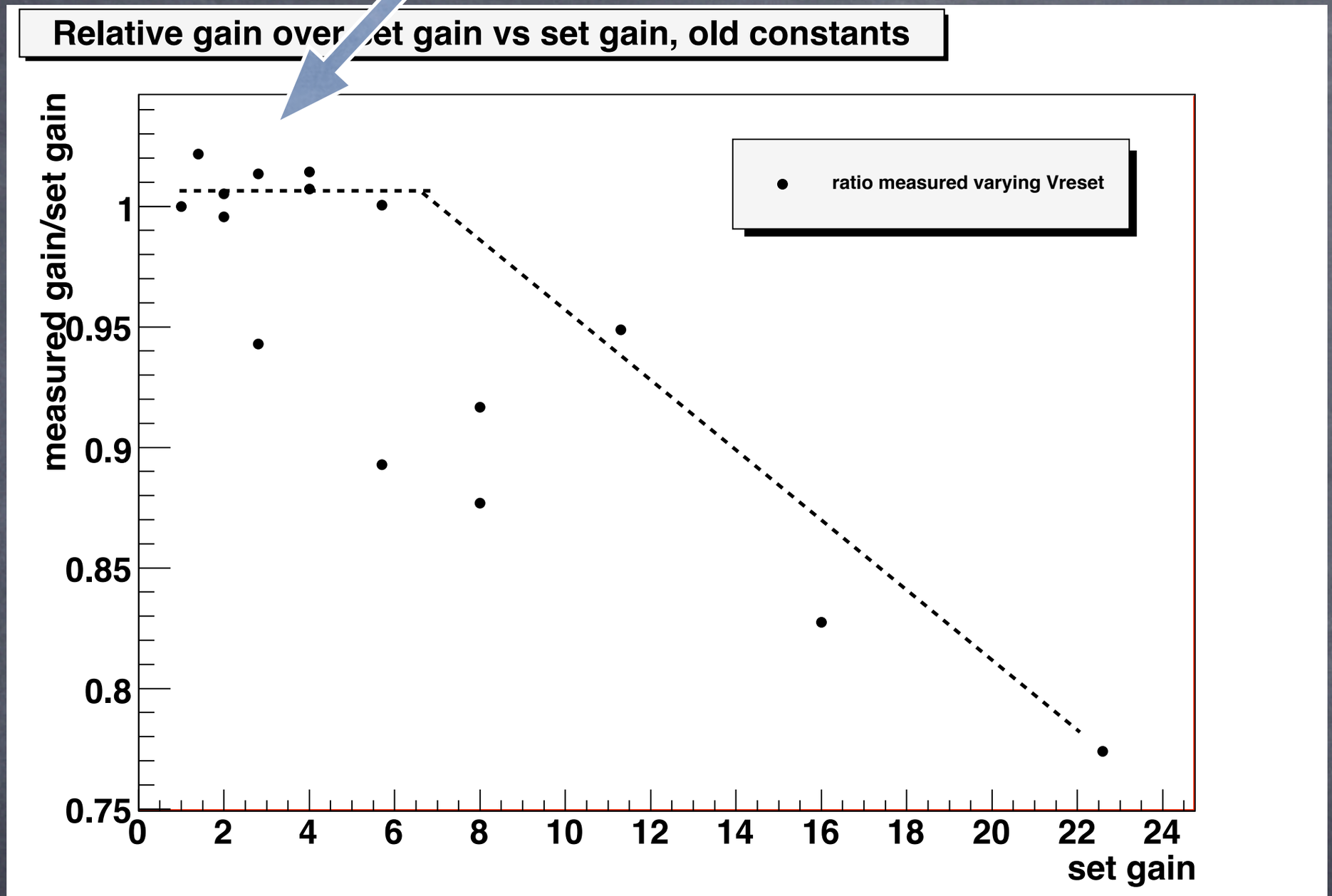
Internal noise in 32-channel mode worse at high gain wrt to single-channel (window) mode with new constants

n.b. corrected ratio



Detector noise in 32-channel mode comparable to single-channel (window) mode

we'll operate here



Measured gain/set gain vs set gain

Summary

- SLAC EGSE in use at 3-4 institutions for JDEM R&D
- active development for system tests, detector studies
- Have working cryogenic SIDECARs at SLAC
  - will soon be used for LBNL focal plane tests
- Optimizing µcode, settings for low power, noise