& CMOS

CCD Image Sensors for Astronomy

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DALSA Professional Imaging
Eindhoven, The Netherlands

October 13th, 2009

Outline

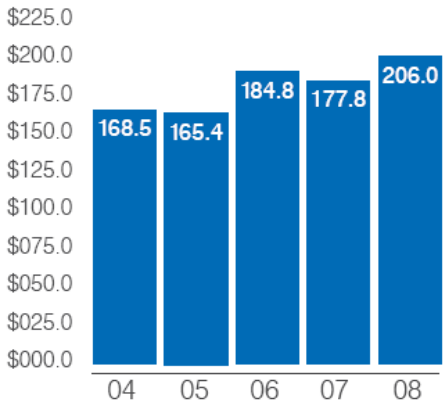
- DALSA Corp.
- CCD Image Sensors
  - Architecture
  - Ultra-low dark current
  - Backside thinned devices
- CMOS Image Sensors
  - Wafer-scale
  - Radiation hardness
- Summary

DALSA Corp at a Glance

- Established in 1980
- Headquarters in Waterloo ON, Canada
- Listed at Toronto Stock Exchange
  - Stock Symbol: DSA (TSX)
  - Shares Outstanding: ~20M

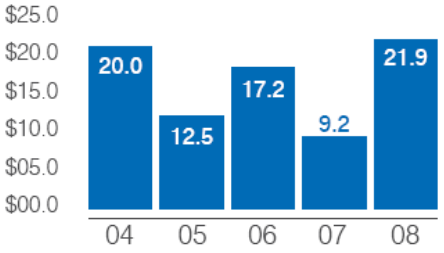
Revenue

from continuing operations ($ in millions)

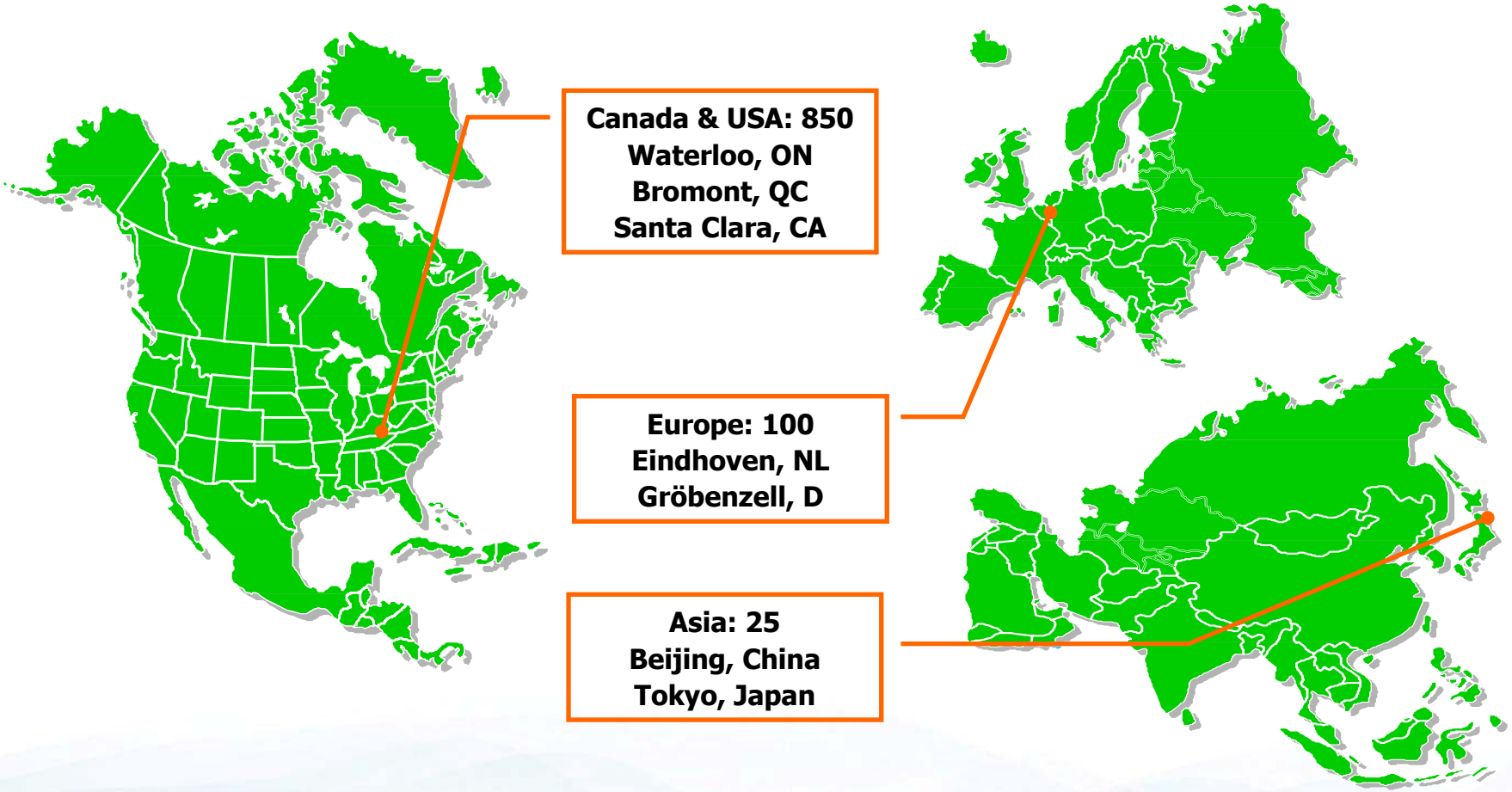


Net Income

from continuing operations ($ in millions)



DALSA Corp Overview



Canada & USA: 850
Waterloo, ON
Bromont, QC
Santa Clara, CA

Europe: 100
Eindhoven, NL
Gröbenzell, D

Asia: 25
Beijing, China
Tokyo, Japan

DALSA Corp – Our Businesses

- **Semiconductor fab - Bromont, Canada**
- **CCD & CMOS image sensors**
- **Digital cameras**
- **Vision processors & software**

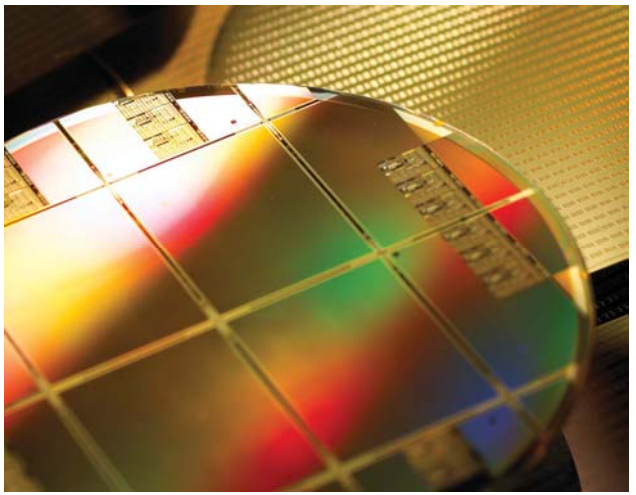
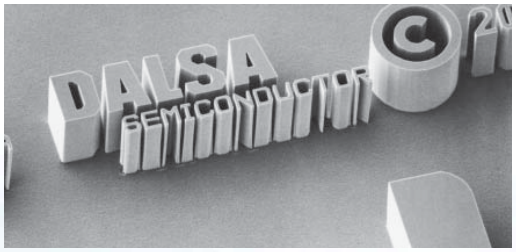


Image sensors



MEM technology

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- Semicondcutor fab - Bromont, Canada
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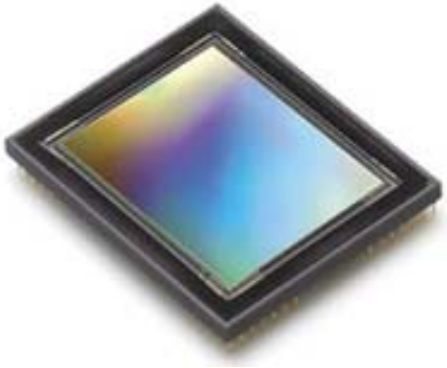
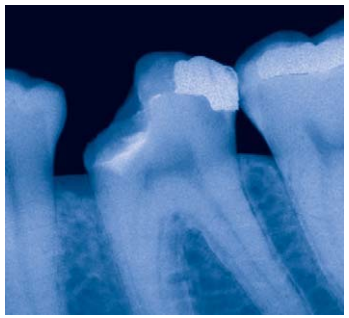
- Vision processors & software

Professional DSC



Broadcast
& video

DALSA Corp – Our Businesses



- Semiconductor fab - Bromont
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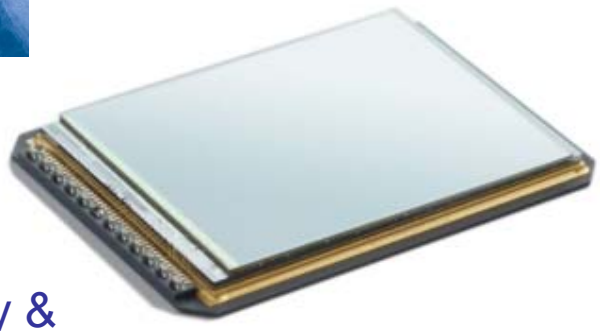
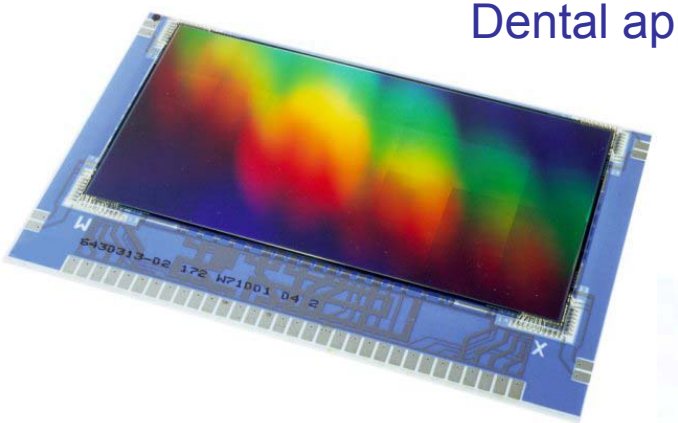
- Vision processors & software



Medical X-ray &
Dental applications



DALSA Corp – Our Businesses

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- **CCD & CMOS image sensors**
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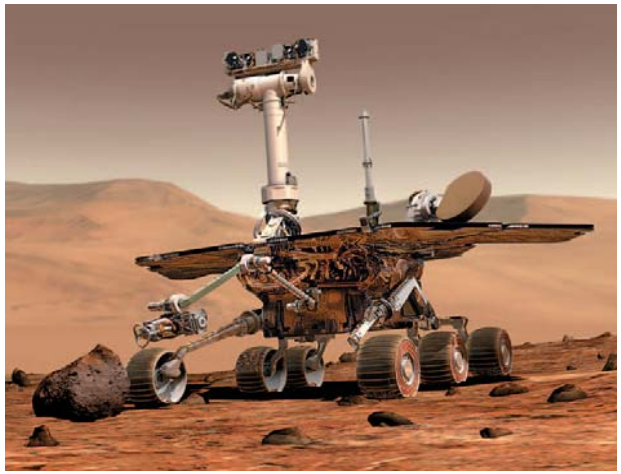
- Vision processors & software



Scientific
& Space

Aerial
Photogrammetry

DALSA Corp – Our Businesses

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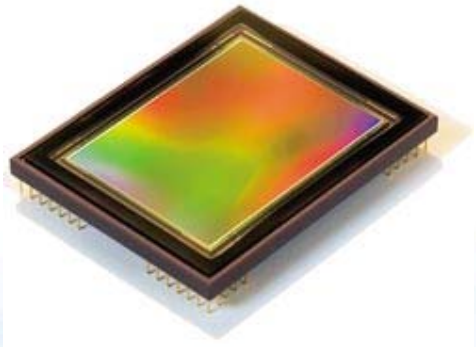
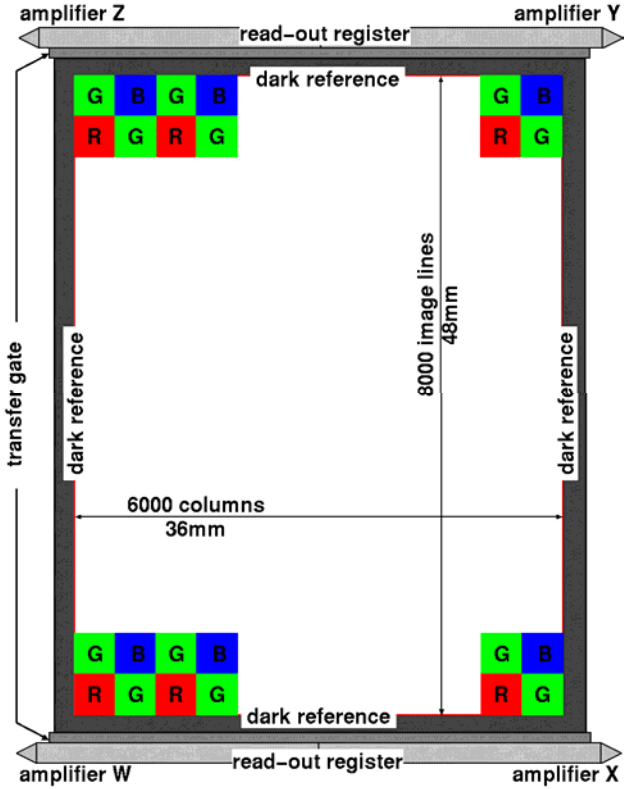
Outline

- DALSA Corp.
- **CCD Image Sensors**
  - **Architecture**
  - Ultra-low dark current
  - Backside thinned devices
- CMOS Image Sensors
  - Wafer-scale
  - Radiation hardness
- Summary

CCD Image Sensor Architecture

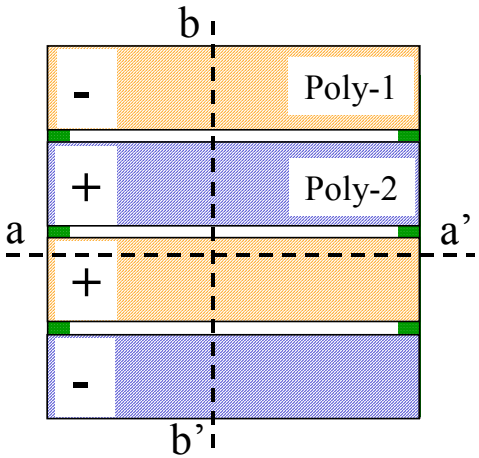
- FF- & FT-CCD
- Bi-directional registers
- Multiple readout amplifiers
- 1…22…60… Mpixels
- Colour & monochrome
- Up to 100 MHz pixel rate per output

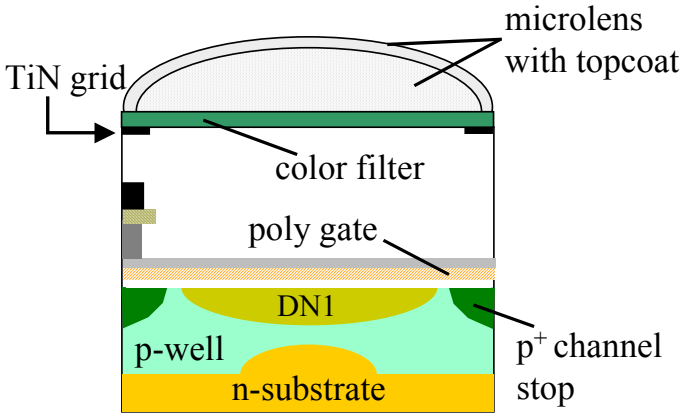




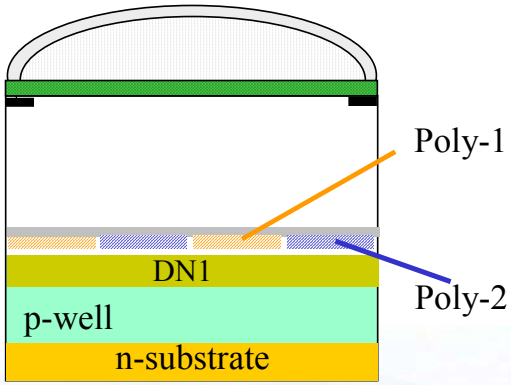
Manoury *et al.*, IEDM Tech. Dig. 2008, pp. 263

CCD Image Pixel Architecture (1)

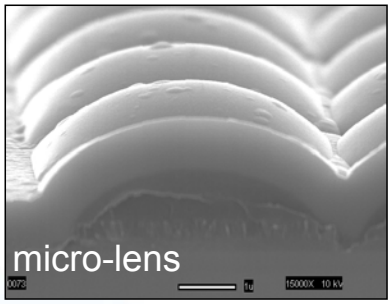




Cross-section a-a'

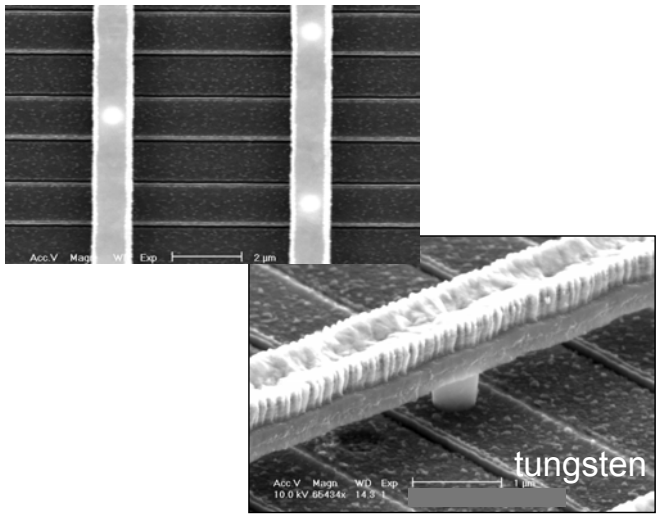


Cross-section b-b'



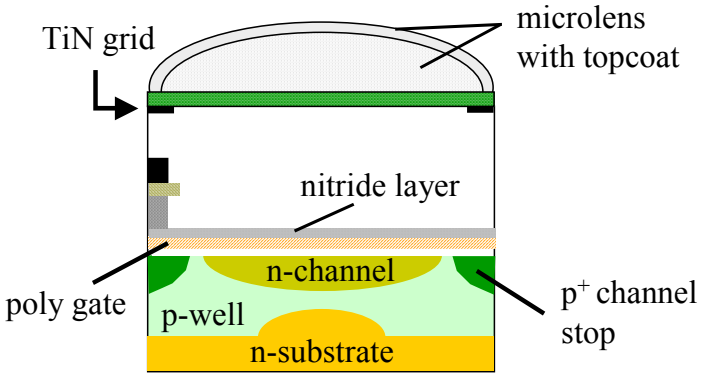
Gapless micro-lenses

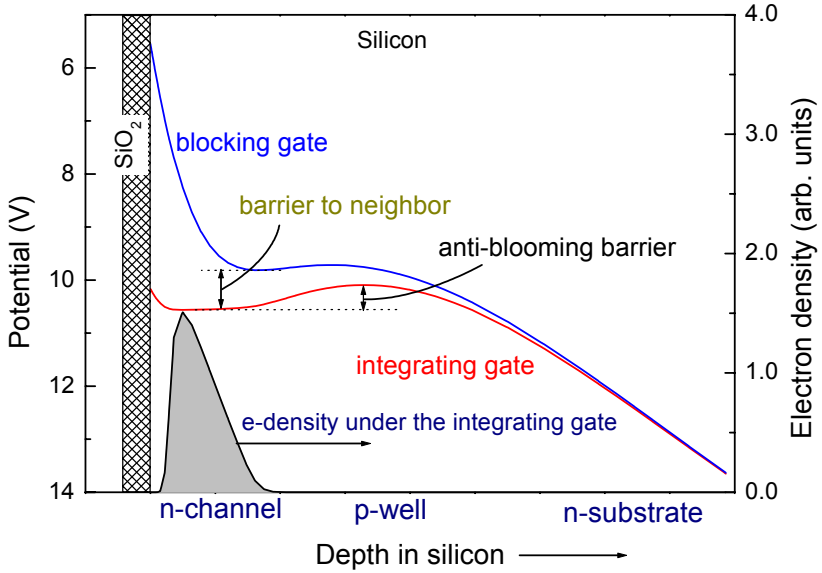
CCD Image Pixel Architecture (2)



- Thin membrane poly-silicon gate
  → High quantum efficiency
- Non-overlapping gates
  → Low RC
  → Reduced power dissipation
- Low-Ohmic interconnects
  → Fast charge transport
- Excellent pixel separation
  → High MTF

CCD Image Pixel Architecture (3)





- 4-phase buried-channel
- Vertical overflow drain to handle overexposure
- Low dark current
- High charge capacity
- Fast electronic shuttering

Bogaart *et al.*, Proc. SPIE **7250**, pp. 725 003 (2009)

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Dark Current in Image Pixels

Dark current generation can be divided in three components:

$$I_{Dark} = I_{Surface} + I_{Depletion} + I_{Bulk}$$

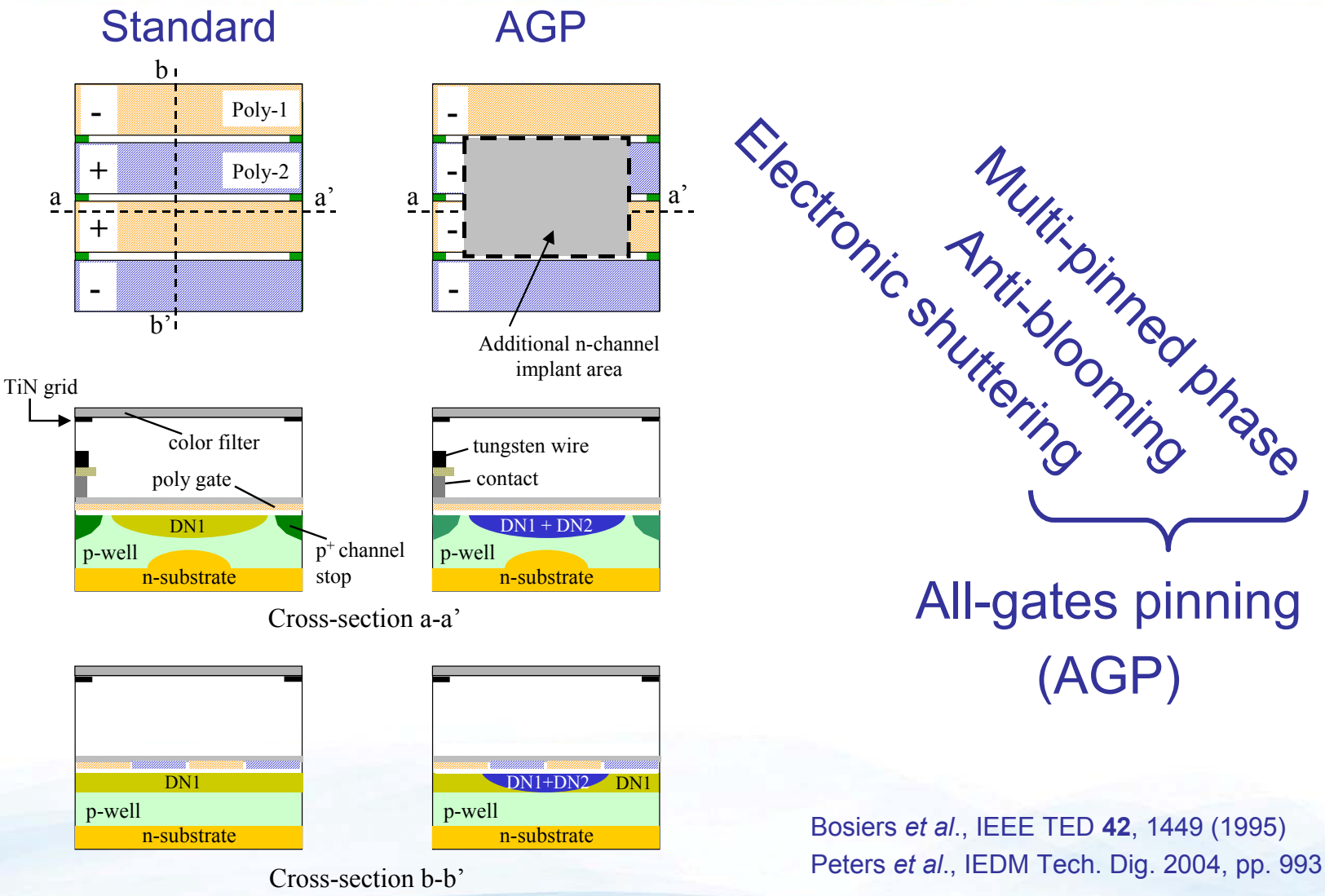
$$= qn_i\left(S_g + \frac{W}{\tau_g} + \frac{n_i D_n}{N_A L_n}\right)$$

Suppression

- $I_{Surface}$: interface of the buried channel biased into inversion
  $\rightarrow$ MPP
- I_{Bulk}: built-in potential barrier reduces carrier diffusion
  $\rightarrow$ vertical anti-blooming

Bogaart *et al*., IEEE TED (2009) accepted

CCD image sensors - Ultra-low dark current (1)

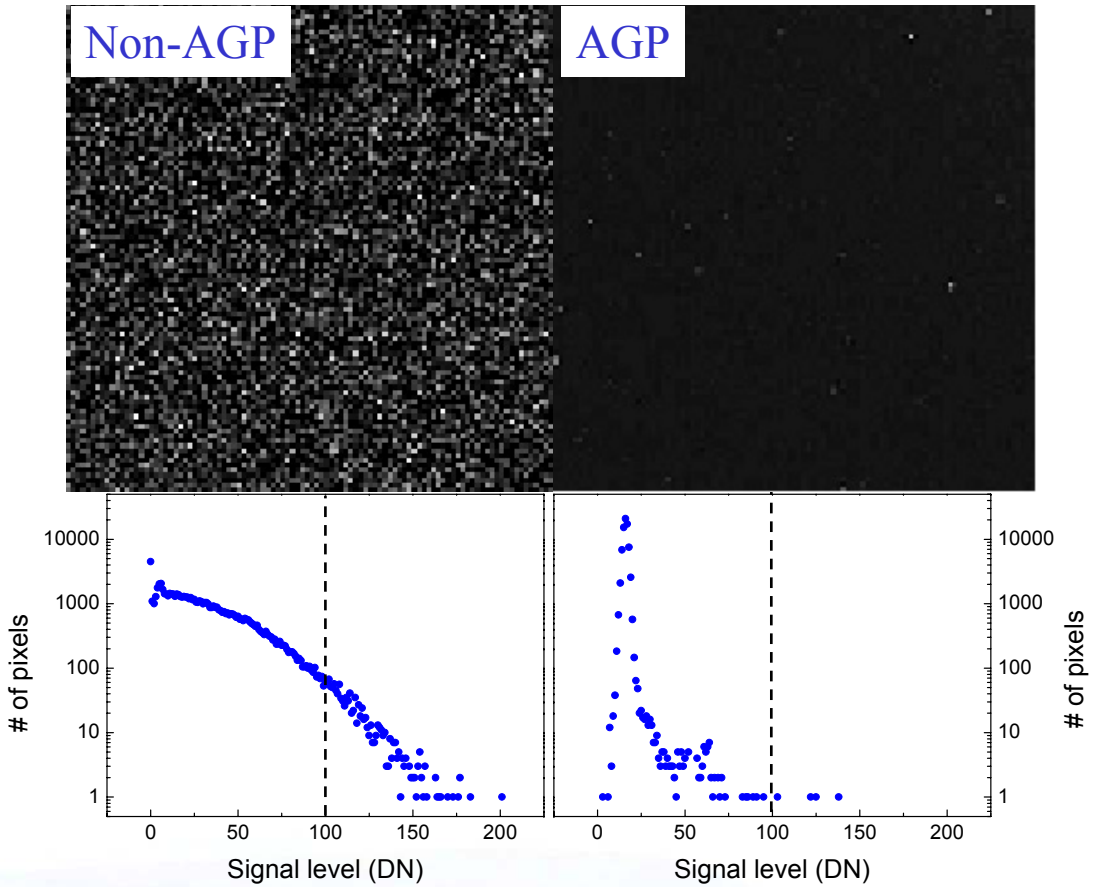


Electronic shuttering
Anti-blooming
Multi-pinned phase

All-gates pinning (AGP)

Bosiers *et al.*, IEEE TED **42**, 1449 (1995)
Peters *et al.*, IEDM Tech. Dig. 2004, pp. 993

CCD Image Sensors – Ultra-low dark current (2)

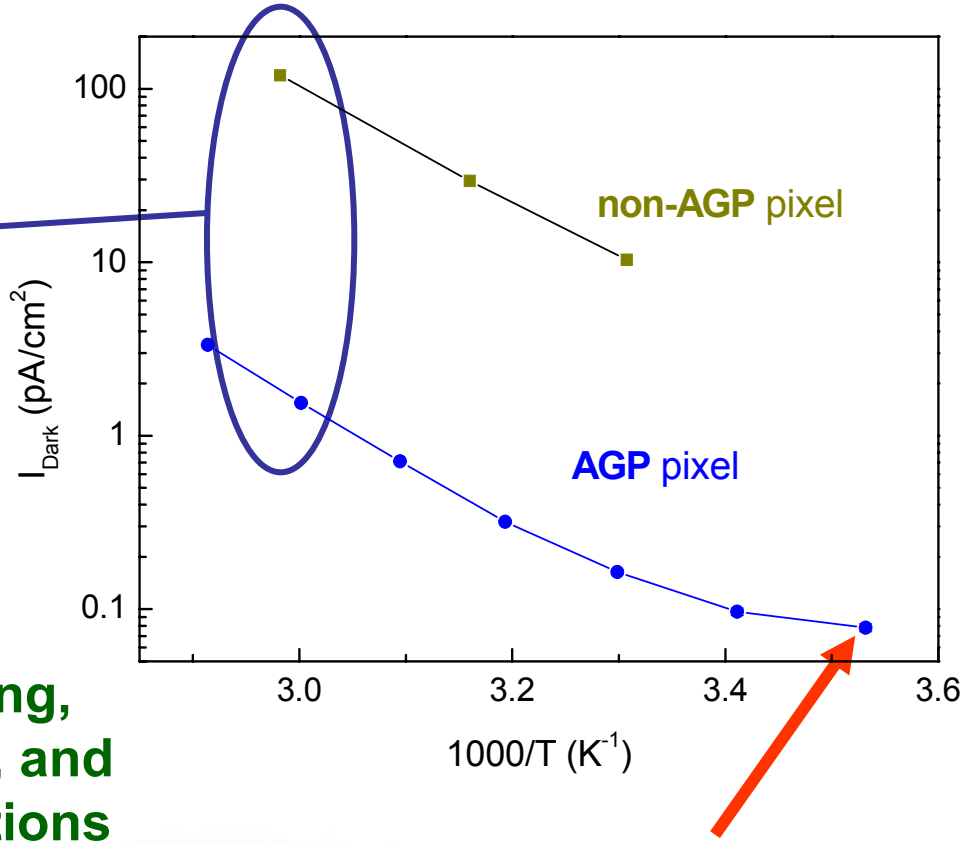


Dark images at room temperature with 6 s integration time
(equally contrast enhanced)

CCD Image Sensors – Ultra-low dark current (3)

80x reduction

Dark current over full well factor (DCFF) improved 28x



Allows low-light imaging, long integration times, and astronomical observations at elevated temperatures

80 fA/cm^2 @ 10 °C

Bogaart *et al.*, IEEE TED (2009) accepted

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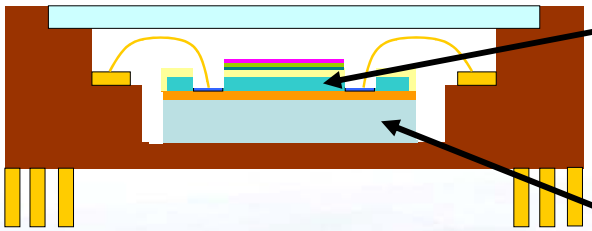
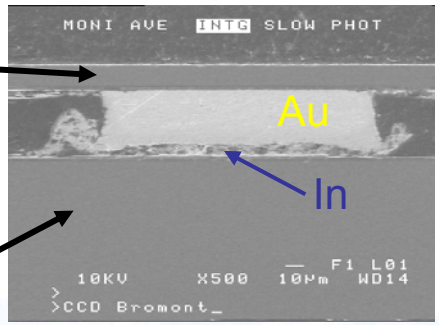
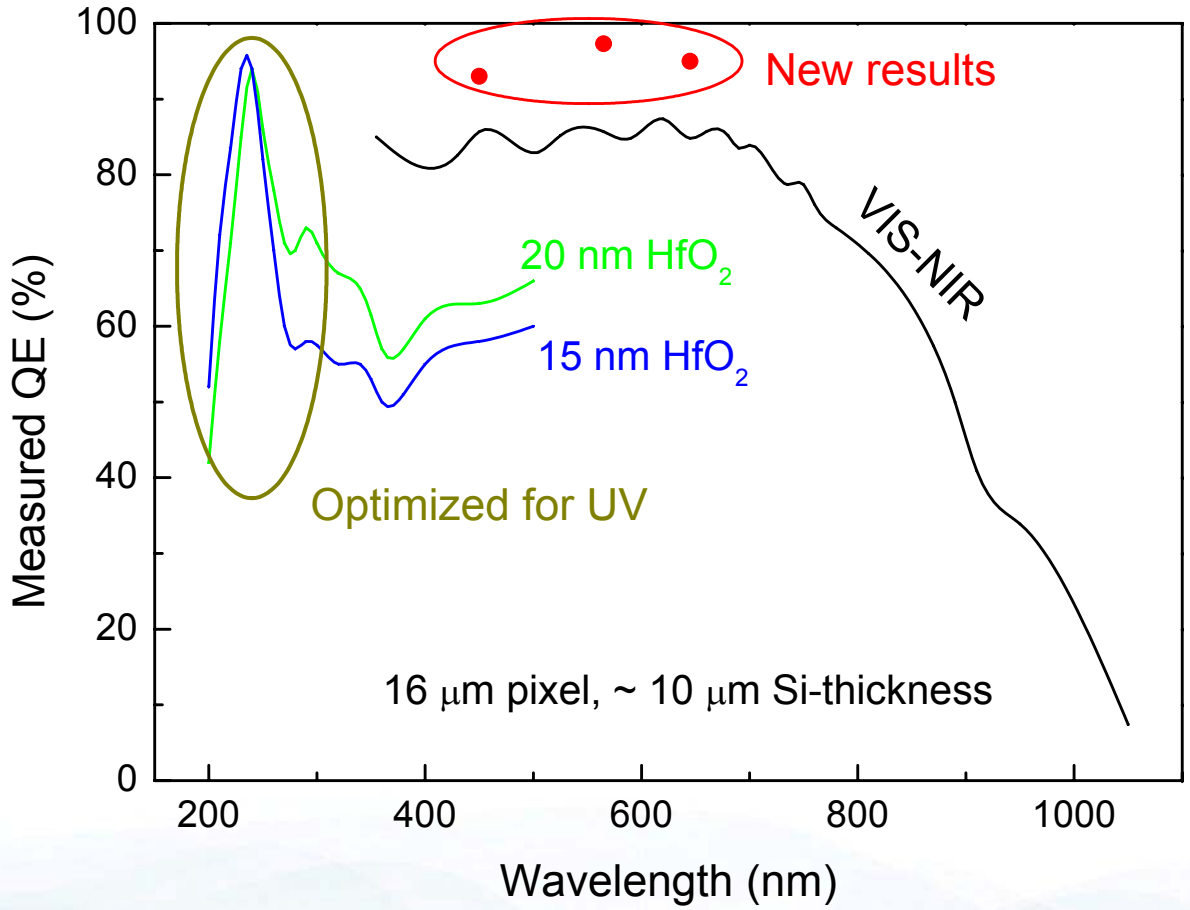
CCD Image Sensors - Backside thinned devices (1)

- Backside thinning: p^--epi on p^+ and SOI substrates
- Die thinning up to 10 × 10 cm^2 devices
- Wafer level thinning on 6″ wafers
- Si-thickness ~ 8..12 μm
- In-bumps, OK at cryogenic temperatures





CCD Image Sensors - Backside thinned devices (2)



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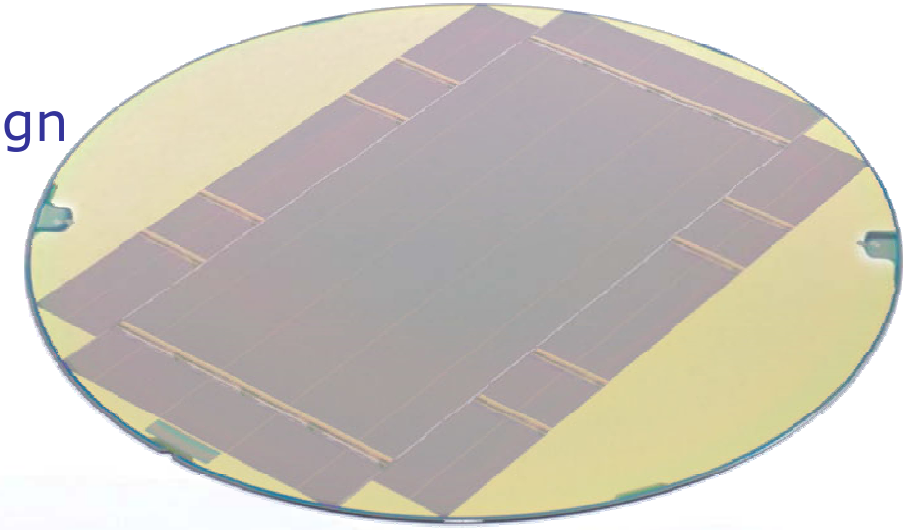
CMOS Image Sensors – Wafer-scale (1)

- 8” wafer, p-substrate
- 77 x 145 mm^2 active area
- 33.55 µm pixel pitch
- 2,304 x 4,320 resolution
- Buttable on three sides
- Radiation-hard pixel design

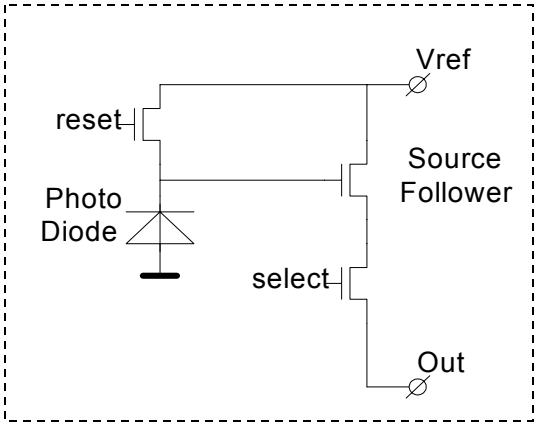


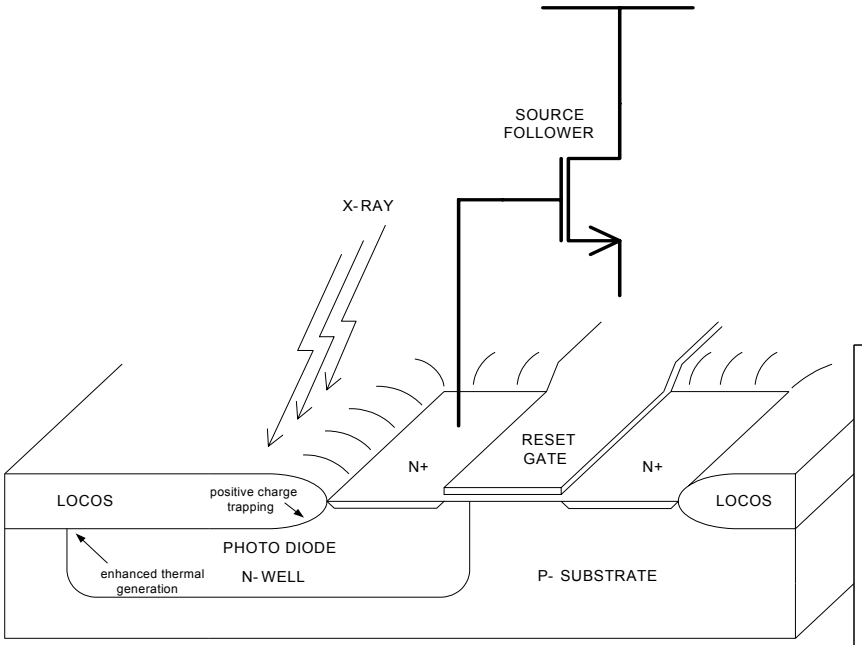
CMOS Image Sensors – Wafer-scale (2)

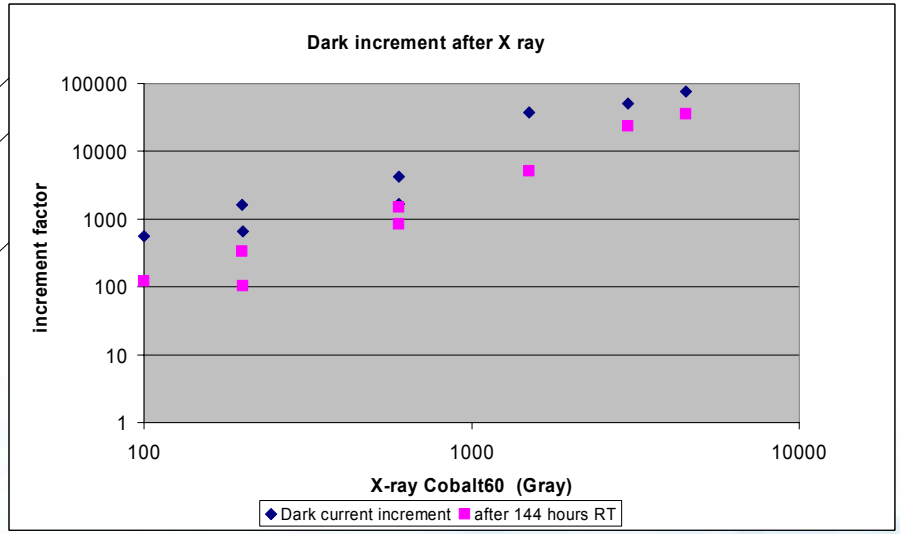
- 2 x 3 CMOS sensors tiled to CsI-coated FOP
- 231 x 290 mm^2 active area
- 6,912 x 8,640 resolution (60 Mpixel)

CMOS Image Sensors – Radiation hardness (1)

Classical Pixel

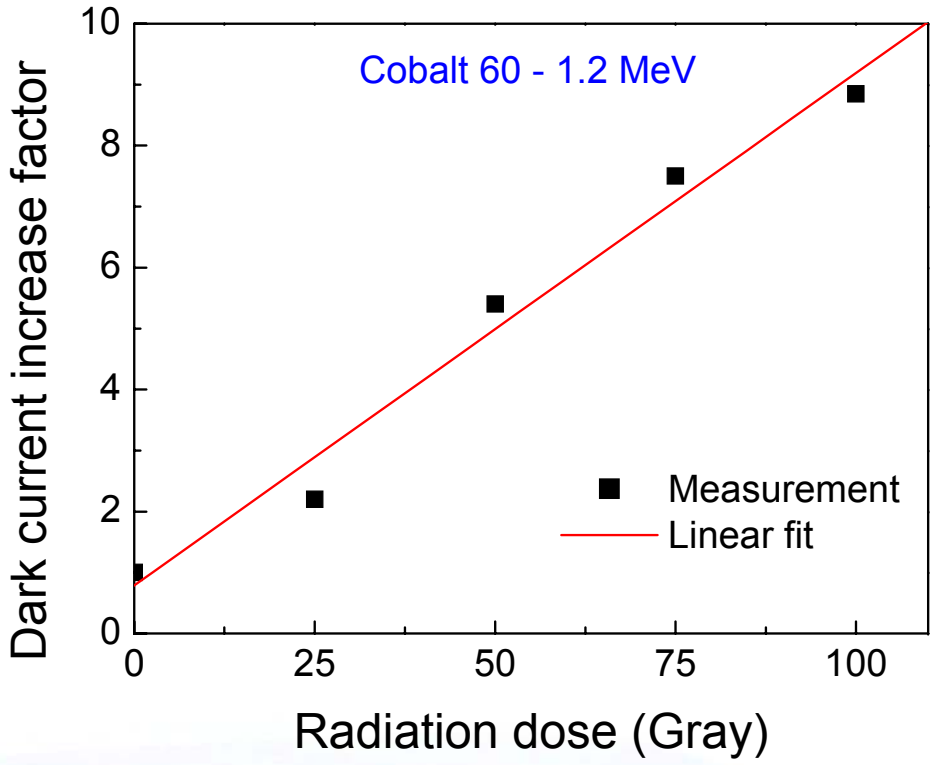






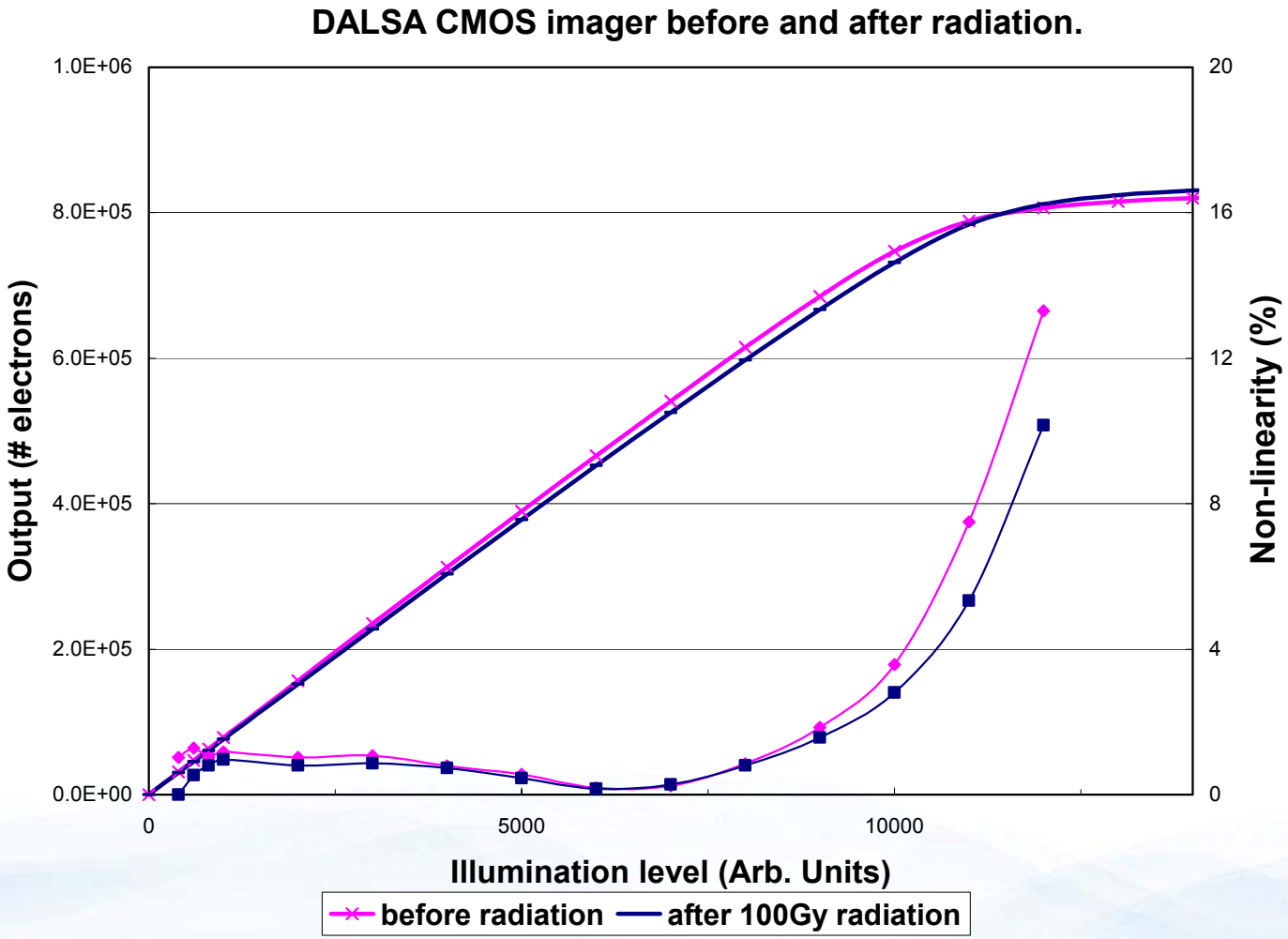
CMOS Image Sensors – Radiation hardness (2)

Radiation Hard PPD Pixel



100x better radiation hard

CMOS Image Sensors – Radiation hardness (3)



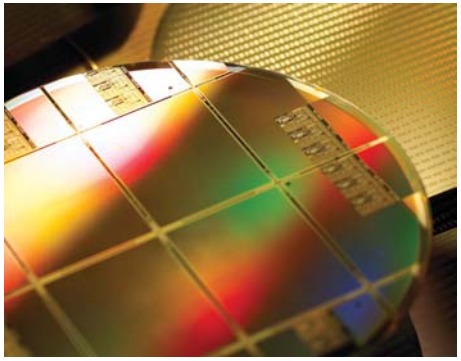
Summary

- World record ultra-low dark current CCD image sensor with All-Gates Pinning
  - » 1.5 pA/cm^2 @ 60 °C
  - » 0.08 pA/cm^2 @ 10 °C
- Dark current over full well factor (DCFF) improved 28x (6 μm pixel)
- Charge transport efficiency, anti-blooming, and electronic shuttering performance are not compromised

- Die level – 10x10 cm^2 – and 6” wafer level BST CCD
  - » UV – QE 94% @ 240 nm
  - » VIS – QE 97% @ 565 nm

- 8” Wafer scale buttable CMOS image sensor
- PPD pixel design, radiation hardness 100x better

Thank you
for your attention



Info: www.dalsa.com/sensors/
E-mail: erik.bogaart@dalsa.com