Backside-Illuminated, high QE, 3e- RoN, fast 700fps, 1760x1680 pixels CMOS Imager for AO with highly parallel readout

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ABSTRACT

The success of the next generation of instruments for 8 to 40-m class telescopes will depend upon improving the image quality (correcting the distortion caused by atmospheric turbulence) by exploiting sophisticated Adaptive Optics (AO) systems. One of the critical components of the AO systems for the E-ELT has been identified as the Laser/Natural Guide Star (LGS/NGS) WaveFront Sensing (WFS) detector. The combination of large format, 1760x1680 pixels to finely sample (84x84 sub-apertures) the wavefront and the spot elongation of laser guide stars, fast frame rate of 700 (up to 1000) frames per second, low read noise (< 3e-), and high QE (> 90%) makes the development of such a device extremely challenging. Design studies by industry concluded that a thinned and backside-illuminated CMOS Imager as the most promising technology. This paper describes the multi-phased development plan that will ensure devices are available on-time for E-ELT first-light AO systems; the different CMOS pixel architectures studied; measured results of technology demonstrators that have validated the CMOS Imager approach; the design explaining the approach of massive parallelism (70,000 ADCs) needed to achieve low noise at high pixel rates of ~3 Gpixel/s ; the 88 channel LVDS data interface; the restriction that stitching (required due to the 5x6cm size) posed on the design and the solutions found to overcome these limitations. Two generations of the CMOS Imager will be built: a pioneering quarter sized device of 880x840 pixels capable of meeting first light needs of the E-ELT called NGSD (Natural Guide Star Detector); followed by the full size device, the LGSD (Laser Guide Star Detector). Funding sources: OPTICON FP6 and FP7 from European Commission and ESO.

Keywords: Adaptive Optics Detector, AO Wavefront Detector, Wavefront Sensor, L3Vision CCD, CCD220, CMOS Imager, CMOS Image Sensor, LGSD, E-ELT.

1. INTRODUCTION

ESO has a long history of developing custom devices to meet the demanding requirements of Adaptive Optics (AO) wavefront sensing (WFS). Detectors with the required combination of fast frame rate, high quantum efficiency, low read noise, and large number and size of pixels are not available off the shelf and thus specialized custom developments are necessary.

This paper begins by reporting on the status of the current generation of optical AO WFS detector, the e2v[1] L3Vision CCD220 (the fastest/lowest noise AO detector to date), the excellent performance results of sub-electron read noise and extremely low dark current which are now being routinely achieved, and the deployment of a large number of camera systems on 2nd Generation VLT instruments.

Attention then focuses on the main topic of the paper, the E-ELT challenge and how advances in CMOS Imagers make them an attractive technology to solve the need for a large advanced Laser/natural Guide-Star WFS Detector, the LGSD, that has been identified as critical for the success of ESO's E-ELT. The paper continues by describing: a) the multi-

phased risk reduction plan for the development of the LGSD that will ensure detectors are available on-time, b) results of industrial design studies performed during 2007 including a comparison of the most promising technologies, c) results from two phases of CMOS technology demonstrators that were built and tested to validate and optimize the pixel, video processor and ADC design, their fulfillment of key requirements (especially read noise and speed), and scalability to full-size, d) the present phase (finishes 2013) of developing a Natural Guide Star Detector, NGSD, which is small enough to be a low cost scaled-down demonstrator to retire architecture and process risks, but large enough to be used for E-ELT first-light AO WFS systems.

2. DEPLOYMENT OF CCD220 ON CURRENT INSTRUMENTS AT ESO

ESO and JRA2 "Fast Detectors for Adaptive Optics" FP6[2][3] OPTICON network funded e2v to develop a compact Peltier cooled sensor, the CCD220, to meet the requirements of WFS for the 2nd Generation of VLT instruments (SPHERE, AOF – MUSE and HAWK-I).

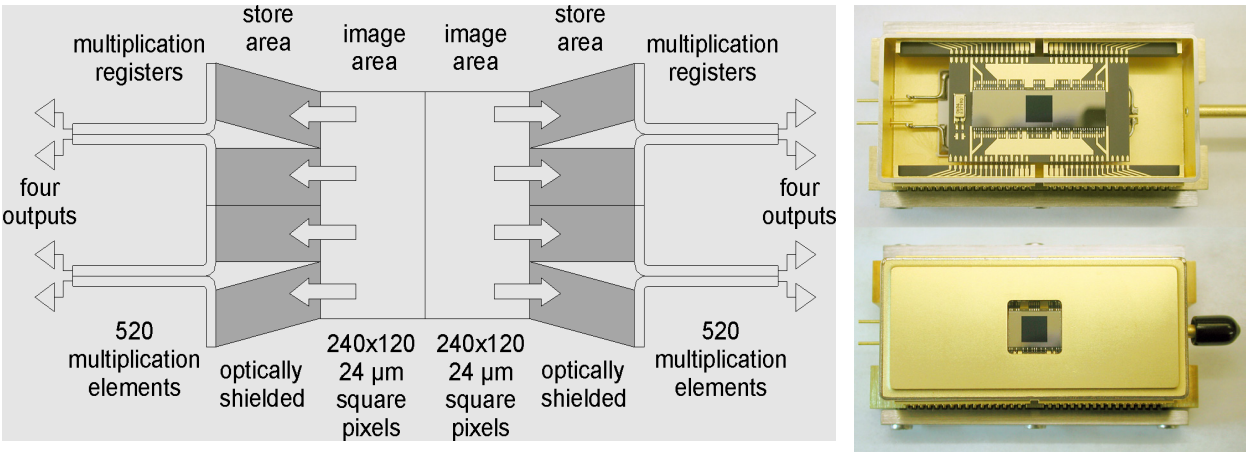

Figure 1. Left: Schematic of e2v 240x240 pixel L3Vision CCD220. Eight electron-multiplying (gain) registers enable sub electron noise at frame rates of 1500 fps. Right: Photograph of CCD220 package. The package contains an integral Peltier that can cool the CCD below -45°C to achieve < 0.04 e-/pix/frame total dark current at 100fps.

The CCD220[4][5][6] (schematic left in Figure 1) is a 24 µm square 240x240 pixels split frame transfer back illuminated L3Vision CCD. The image and store area (store is optically shielded) are built with 2-phase metal-buttressed parallel clock structures to enable fast line shifts in excess of 7 Mlines/s for total transfer time from image to store of 18 µs and low smearing of under 2% at 1,200 fps. Eight electron-multiplying gain L3Vision[7] registers operating at greater than 13 Mpixel/sec enable sub electron noise to be achieved at frame rates of 1,500 fps. With a measured output amplifier read noise of 80e- at unity gain and electron-multiplying gain of 1000, an overall effective read noise of under 0.1 e- (80 e-RON/1000 of gain register) is achieved.

The CCD220 is encapsulated in a 64 pin package (right in Figure 1) with a custom-designed integral Peltier cooler that has been verified[8][9][10] to cool the CCD below -45°C to achieve the required < 0.04 e-/pix/frame dark current at 100fps. The package is sealed and back-filled with 0.9 bar of Krypton gas to minimize heat transfer to the outside.

As part of JRA2, a consortium of French institutions IPAG-LAM-OHP, developed a low noise state of the art controller, called OCam[12] (photo left Figure 2); one was loaned to e2v for testing the production of CCD220s and another used at ESO for device characterization. Using OCam as their test camera, e2v have tested and delivered to ESO twenty science grade CCD220 devices that meet specifications: of these 16 are standard silicon and four are Deep Depletion. The thicker silicon Deep Depletion devices provide much sought after higher QE in the "red" (Figure 3) for instruments that use Natural Guide Star (NGS) WFS: SPHERE and AOF tiptilt.

The exceptional performance of the devices has now been confirmed at ESO and the results shown in Table 1 are typical. Previous problems of high Dark Fixed Pattern and read noise that was earlier reported have now been fixed with an improved design of the HV Clock generator. The e2v L3Vision EMCCD multiplication register requires a HV Clock of up to 50V switching at pixel rate.

Figure 2. Left: Close-up photo of the OCam test camera. Right: Image of OCam team (Left to right: Christian Guillaume, Jean-Luc GACH, Philippe Feautrier, and Philippe Balard) taken by the OCam camera with CCD220 cold and with L3Vision multiplication gain.

Table 1. Typical performance of science grade "standard silicon" and "Deep Depletion" e2v CCD220 measured at ESO.

Requirement	Measured Result	Specification
Frame Rate (fps)	> 1500	>1200
Read noise at gain of 1000 and 1500fps	< 0.1e-	< 1.0e-
Image Area Full Well (e-)	> 200k	>5,000
Serial Charge Transfer Efficiency	0.99999	> 0.9998
Cosmetic (number of traps bright and dark defects)	0	< 25
Dark Current at 1200fps and -40ºC (e-/pixel/frame)	< 0.01	< 0.01
Dark Current at 100fps and -40ºC (e-/pixel/frame)	< 0.02	< 0.04

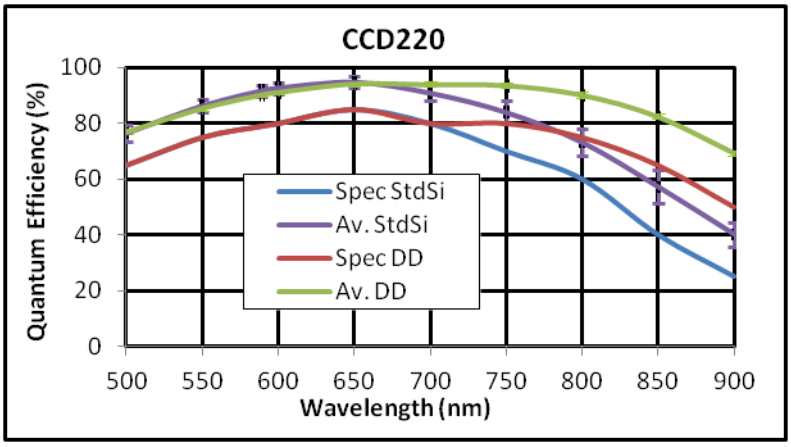

Figure 3. Measured average QE (e2v) of 16 Science Grade Standard Silicon (labeled Av. StdSi) and 4 Deep Depletion Silicon (labeled Av. DD) CCD220s compared to the contract specification. All are > 5% higher than the specifications. The > 20% higher QE in the "red" illustrate why the Deep Depletion are highly sought after for NGS applications.

For the scheduled deployment of the CCD220 on VLT instruments, ESO (contact Javier Reyes jreyes@eso.org for details) has developed an AO version of the New General detector Controller (AONGC). While the majority of the camera was developed in-house, AONGC[13][14] has re-used (through a technology transfer contract) the front-end analogue design developed by Flight Light Imaging[15]; a company setup to commercialize the OCam[16] camera.

Several advanced AONGC prototypes (Figure 4) are fully operational (meeting all performance specifications) and are in current use for instrument integration and advanced testing of SAXO[17] (the SPHERE Extreme adaptive optics system) and the VLT AO Facility. The final production model will go into production later this year.

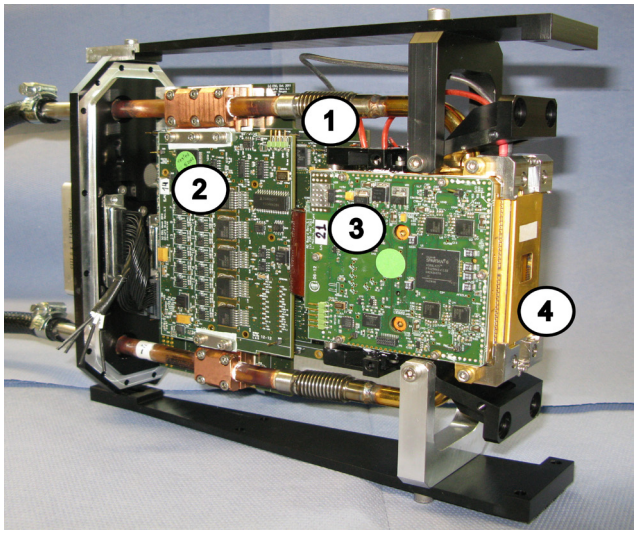

Figure 4. Left: Photograph of ProtoCam, a pre-series version of the AONGC camera developed at ESO. The camera is fully operational and meeting all performance specifications. The labels in the diagram refer to: 1) Main board, 2) Bias board, 3) Analog front-end boards developed by Flight Light Imaging, 4) CCD220.

3. THE FUTURE: THE E-ELT CHALLENGE

For WFS on the E-ELT, four different types of applications (Figure 5) for detectors have been identified:

1) InfraRed (IR) WFS and Tip-Tilt detector,
2) Optical < 240x240 pixels detector for low order AO, Shack Hartmann (SH) Quad-Cell, Pyramid, Tip-Tilt sensors, Guiding applications where an existing high performance detector such as the CCD220 is sufficient,
3) Optical Extreme Adaptive Optics (XAO) NGS pyramid WFS detector with a modest number of pixels (~240x240), but read out at extremely fast frame rate (2.5 to 3 kfps), ultra low read noise/dark current (< 1 e/pixel/frame), and high QE > 90% especially in the "red" (450-900nm),
4) Large optical Laser Guide Star (LGS)/Natural Guide Star (NGS) SH WFS detector with very large pixel format to sample the spot elongation, fast frame rate (700 fps), high QE (> 90%), and low noise (< 3e-).

ESO's development efforts for IR WFS and Tip-Tilt detectors are discussed in Finger et. al[20][21]. The tip-tilt/guiding detector can be met by existing CCD220 detectors (see section 2). For the XAO detector, there is the good possibility to operate the CCD220 gain/serial registers at 26Mpix/sec (double the tested speed) and thus achieve a frame rate of 2.5 kfps. This investigation will be carried out towards the end of the current characterization of the CCD220. The large optical LGS/NGS WFS detector is critical for the success of the E-ELT, and is the subject of the rest of this paper.

Spot elongation of LGS (Figure 6) is considered one of the major challenges of AO WFS systems of ELTs. The spot elongation is due to the finite thickness of the sodium layer and the offset between the laser projection point and the sub-apertures of a SH WFS. The elongation or spreading of the LGS image results in a decrease in the signal to noise ratio (SNR) resulting in an increase of the centroid error, and subsequently increased error of the wavefront phase reconstruction.

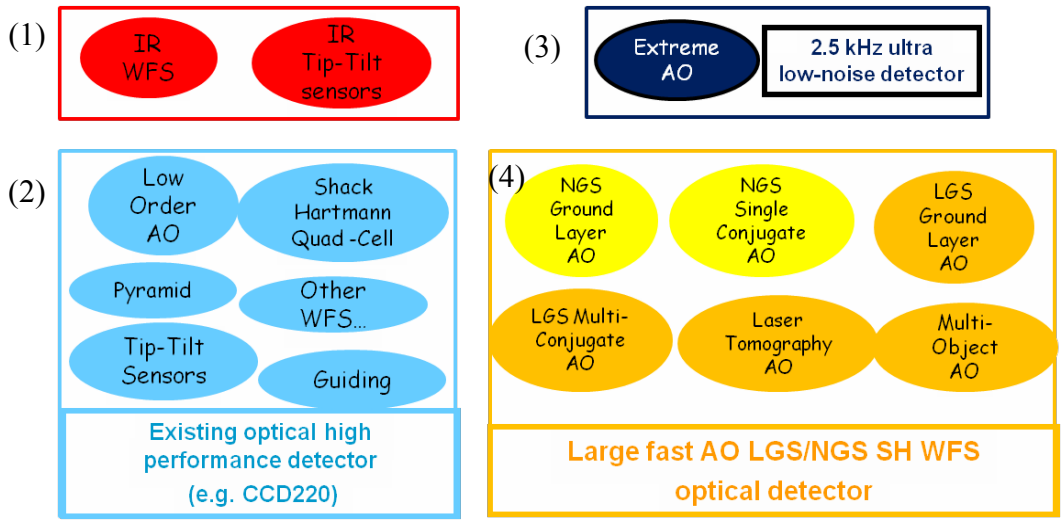

Figure 5. Diagram showing the breakdown, into four different application areas, of detectors for WFS on the E-ELT.

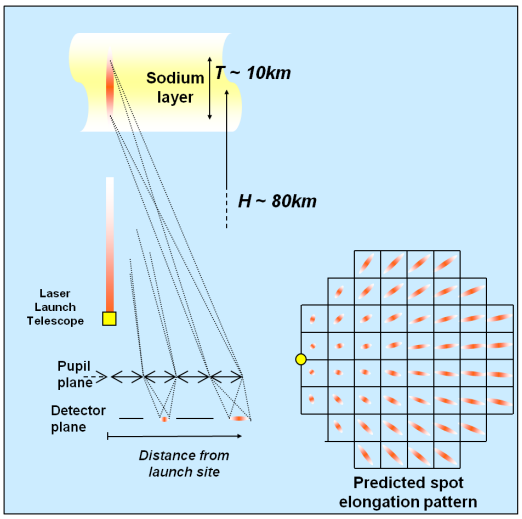

Figure 6. The spot elongation is due to the finite thickness of the sodium layer (10-15km) and the offset between the laser projection point and the sub-apertures of SH WFS. The LGS baseline design is to have the lasers projected from the telescope sides.

The current LGS WFS system for the E-ELT (an adapative Telescope) baselines the following: 1) 4 Continuous Wave (CW) Sodium LGSs projected from the sides of the telescope, 2) enough laser power to provide 1000 photons per sub-aperture per frame, 3) high spatial sampling up to 84 x 84 sub-apertures (goal of 126 x 126 for later upgrade) and 20 x 20 pixels per sub-aperture to adequately sample the spot elongation, and 4) high temporal sampling of 700 Hz.

From the top level science requirements, the following requirements for the large LGS/NGS AO WFS detector (LGSD) have been justified:

1) Minimum format size of 1680x1680 pixels,
2) Big pixels of 20-28μm, to ease the optical system design (mechanical alignment and stability), but small enough to avoid excessive dark current/counts, charge transfer inefficiency (image lag), or manufacturability problems,

3) Versatility of 100% fill factor for maximum flexibility; to make it possible to decide later to change laser projection site and/or mix of sub-apertures/pixels,
4) Low dark current and read noise such that total noise is < 3e- rms.
5) High QE over wavelength of 450-950nm (for NGS applications) and especially at 589 nm (LGS wavelength),
6) Equivalent exposure time of frame rates from 100fps to 700 fps with goal of 1000fps with slightly (gracefully) degraded performance,
7) Low read out latency (time between end of exposure and image available at output pin < 7 % of exposure time) so that corrections can be computed and applied as quick as possible after the exposure ends,
8) Detection signal limit of 4000e-/pixel; laser power will be limited so the system will be photon starved (expect only 1000 photons per sub-aperture per frame),
9) Good spatial characteristics, PSF < 0.8 pixel FWHM (Full Width at Half Maximum), to accurately determine where the photons arrived,
10) As cosmetically defect-free as possible; < 0.1% defective pixels,
11) Ease of use/compact size:
    a. Low pin count; goal < 200 pins,
    b. Integrated read-out electronics with all video processing (including DCS, noise bandwidth limiting, and programmable gain) and digitizing of signal (ADCs) on-chip,
    c. Digital serial data interface with minimal glue logic to the likes of RocketIO or SelectIO of Xilinix Vertex-6 or later series of FPGA. Preference for industry standard interface such as Low Voltage Differential Signal (LVDS) ANSI/TIA/EIA-644, Low Voltage Pseudo Emitter-Coupled Logic, LVPECL, or Current Mode Logic, CML.
    d. Integral Peltier cooled package for compact size, maintenance free, and minimal support equipment. As a Peltier cooler is not able to remove a large amount of heat at great efficiency, an upper limit on the power consumption of < 5W is imposed on the detector.

The development plan for the large LGS/NGS AO WFS detector is a multi-phased (a progressive risk retirement) development over ~ 10 year duration (Figure 7) to have detectors available on time for the first light AO systems of the E-ELT in 2023. The phases are: (1) Design Study to investigate possible technologies, (2) Technology Validation to retire pixel risks, (3) Natural Guide Star Detector (NGSD), a pioneering, first generation, ¼ size, scaled down demonstrator to retire architectural and process risks, (4) Laser Guide Star Detector (LGSD), the full scale development which should mostly be an engineering exercise, and (5) Production Run to manufacture 30-50 devices.

As part of the ELT design study (DS) program, a number of detector design studies were performed by industry during 2007. The studies showed that conventional CCD arrays, mosaics of CCDs or pnCCDs, and CCDs or silicon photodiodes (e.g. Teledyne HyViSI) bump bonded to CMOS read out structures: 1) will unlikely meet either the low read noise requirements and/or require cooling below 70K, or 2) suffer from serious trade-offs between power dissipation, noise, latency and read out speed, and/or from manufacturability issues. Other solutions such as 3-D integrated Focal Plane Arrays[18] were considered technologically immature.

The design studies identified four possible technologies[19]:

1) Back-Side Illuminated (BSI) CMOS Imager,
2) Front-Side Illuminated (FSI) CMOS Imager with advanced gapless microlenses,
3) APDs in linear or Geiger mode (SPADA – Single Photon Avalanche Diode Array),
4) Orthogonal Transfer WFS Electron Multiplying CCDs (OT WFS EMCCD).

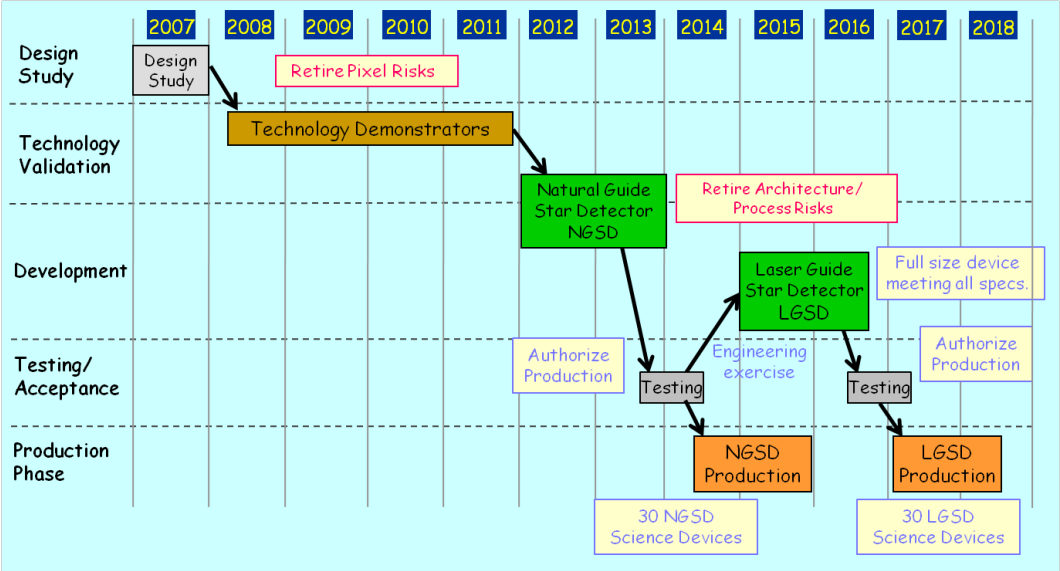

Figure 7. The multi-phase development plan of the large optical NGS/LGS WFS detector showing how risk is progressively retired; Design Study to investigate possible technologies, Technology Demonstrator to retire pixel risks, ¼ full size Scaled Down Demonstrator (NGSD) to retire architectural and process risks and to ensure devices are available on time for first light E-ELT instruments, the full scale development (LGSD) which should be mostly an engineering exercise, and finally production run to manufacture 30-50 devices.

For the pixel size, format size, and frame rate, BSI CMOS Imager was judged overall the most likely to succeed. Recent developments[22] in CMOS imagers have provided rapid improvement in performance where read out noise of 2-3 e-, dark current as low as 10 pA/cm^2 at room temperature, and QE > 80% have been demonstrated in prototypes[24][25][26][27] and commercially available detectors[28]. This type of performance now rivals CCDs.

The rapid progress has come about through several innovative improvements[29]: a) Pinned Photo Diode (PPD) that substantially reduce the dark current, b) high conversion gain (by reducing the sense node capacitance) that amplifies the signal above the noise and obtains effective low read noise of under 3e-, c) buried channel MOSFETs that reduce/eliminate random telegraph signal (RTS) noise and background flicker noise associated with the surface states in the source follower pixel and reset transistors, d) improvement in QE and pixel crosstalk of the CMOS imager by back-side illumination and building the sensor from thicker high resistivity silicon (> 10,000 ohm-cm), and high voltage 'substrate biasing' to efficiently collect charges generated deep within the silicon, without pixel crosstalk and consequential blurring, and to extend the wavelength response into the near red.

Conceptual block diagram (Figure 8) of the LGSD (BSI CMOS Imager) consists of a 1760 x 1680 square grid array of pixels addressed from either side and read out from both top and bottom. The central 1680x1680 pixels will be light sensitive while the outer 40 columns either side will be optically masked and used as reference pixels if required. Many rows of pixels are read in parallel to allow enough processing time per pixel to beat down the noise and the ADCs to digitize the signal. The data is multiplexed and transferred off-chip through fast LVDS digital interface. Calculations showed little difference in power consumption of including ADCs on-chip as opposed to using high speed analog drivers to transport the signal off-chip. Including ADCs on-chip provides a simple digital interface, and a better chance of achieving and maintaining low noise performance.

Many design trades exist. More rows read in parallel reduce the read noise, but at the expense of longer latency, greater silicon real estate area, longer higher capacitance signal drive lengths, and higher power dissipation. The optimum number of rows processed in parallel was determined to be 40; half each (20) at top and bottom. With forty rows read in parallel at 700fps, the pixel processing time is ~ 34µs. This is considered adequate time to do the video processing and digitize the signal to achieve < 3e- rms read noise while still meeting the low latency requirements.

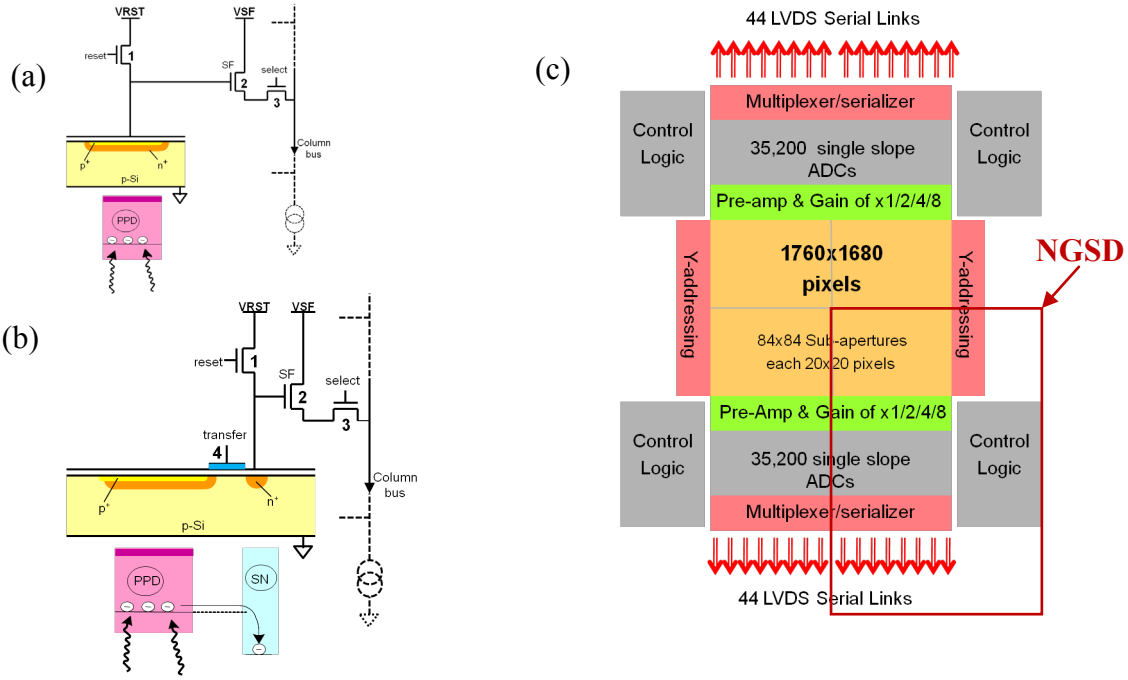

Figure 8. CMOS imager: (a) 3T PPD pixels, (b) 4T PPD charge coupled pixels, (c) e2v's conceptual block diagram of the LGSD built using BSI CMOS Imager. The outline of the quarter sized NGSD scaled down demonstrator is shown in red.

In the design of the ADCs, there are trades between: a) the type of ADC, b) the number, c) the conversion rate, d) the silicon real estate area, and e) power dissipation. While several types[23] (cyclic, successive approximation, and single slope) of ADCs have been used in high speed CMOS imagers, a column parallel single slope[22] ADC is preferred for its small size, simplicity, robustness, low noise, and excellent differential non-linearity (DNL). One of the disadvantages of the single slope ADC is the trade between resolution and clocking rate. Each n-bit ADC conversion requires 2^n clock periods. Complicated techniques such as non-linear [23] and multiple slope[23] ramps have been proposed to overcome this trade. However, by analyzing the LGS spot illumination patterns (Figure 9), one notes that apertures close to the laser launch site have the signal contained within a few pixels while those far away have the signal spread over many. An acceptable compromise is to have a 9-bit resolution ADC combined with regions that can be programmed with different gains. Sub-apertures close to the launch site can then be programmed with low gain where detecting high signal is important while those far away can have a high gain where low read noise is more important.

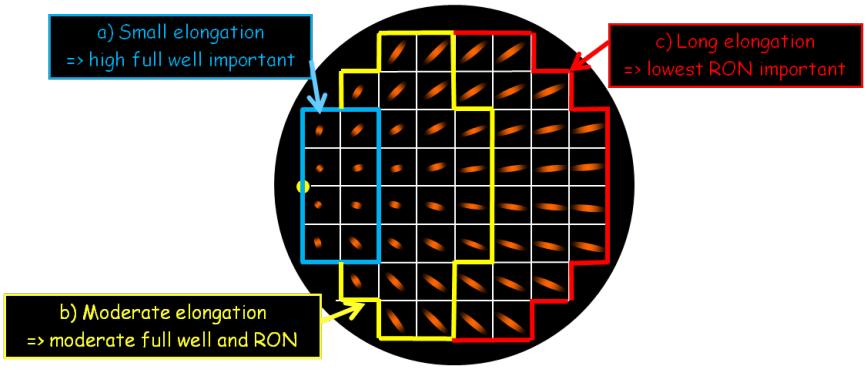

Figure 9. Why 9-bit resolution ADCs combined with regions that can be programmed with different gains is an acceptable compromise. Image shows a typical spot elongation pattern for side projected laser. Three different regions are identified: a) region of small elongation where detecting high signal is important, b) region of moderate elongation where moderate signal detector limit and read noise are acceptable, c) region of long elongation where lowest read noise (RON) is important.

Serial LVDS lines (with no coding) operating at 220MBaud were chosen to transfer the data off-chip. Eighty-eight lines are required to handle the 18.6Gbaud (= 1760 x 1680 pixels x 700fps x 9 bits conversion) bit rate of the LGSD. The NGSD being quarter sized only require 22. This solution was considered the best conservative trade between the number of package pins, serial data rates, data transmission reliability, and power dissipation. With the proposed use of two supply pins per line, 352 (88*4) package pins will be required for the serial interface in the LGSD. During NGSD evaluation, the possibility of transmitting data at higher bit rates (e.g. doubling to 440MBaud) will be tested to investigate whether the number of lines and thus pins can be considerably reduced in the LGSD.

4. TECHNOLOGY VALIDATION

During 2008 and 2009, several manufacturers built and tested (as part of the ELT DS) technology (pixel) demonstrators (TD) of CMOS Imagers to assess and validate various CMOS technologies, their capability to meet key requirements (especially of image lag, read noise, and speed), and scalability to full-size devices. The TDs consisted of arrays of pixel variants that tested and compared performance of 3T and 4T pixels, and different geometries and threshold voltages of the pixel transistors, in order to find the most suitable 24µm pixel for the application. In the case of the 4T pixel, extra implants in the photodiode were investigated to see if these could improve the transfer of charge (reduce image lag) from the photodiode to sense node. Up until this time, very little was known about the image lag performance of large 24µm pixels, as most other applications in the literature were interested in much smaller (6µm or less) pixels. In addition, the TDs included testing of critical elements of the video processing and ADC circuits.

Measured result of read noise of < 3e- rms at the required pixel speed was very promising. Both 3T and 4T (Figure 8) pixel architectures achieved the required performance. However, 4T pixels were preferred over the 3T as the former only require a single ADC conversion when coupled with an analog DCS (aDCS) circuit, while the latter requires two conversions (reset+signal) to implement digital DCS (dDCS). Power consumption and complexity of the ADCs and multiplexer/serial data interface was already considered difficult without a doubling of the speed requirements (as in the case of the 3T pixel).

A second phase of technology validation took place during 2010 and 2011 to retire remaining pixel risks and to further optimize the pixel, video processing and ADC design. This phase consisted exclusively of 4T pixels. The Technology Validator (Figure 10) built by e2v technologies featured 60x60 4T pixels, 1200 (60 x 20 rows read in parallel) single slope ADCs, and a read out speed that is consistent with a frame rate of 700fps in the final device.

Measured results clearly validated the 4T pixel CMOS imager approach by reporting read noise of < 3e- rms at the required pixel speed, low image lag of < 0.1%, and good linearity to full well of > 4000e-. Pixel conversion gains were in excess of 100µV/e-. The best pixel, video processing, and ADC design was found to go forward to the NGSD phase

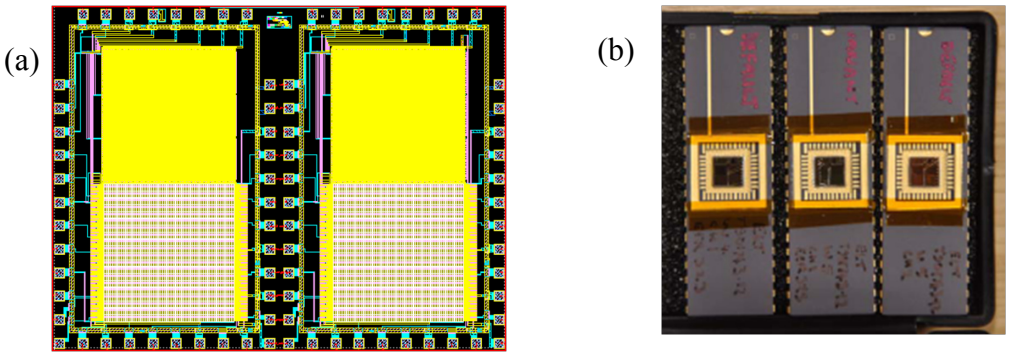

Figure 10. The Technology Validator built by e2v technologies: (a) chip mask layout, (b) Photograph of devices tested. The device featured 60x60 4T pixels, 1200 (60 x 20 rows read in parallel) single slope ADCs, and a read out speed that is consistent with a frame rate of 700fps in the final device.

5. NGSD/LGSD DESIGN

At the start of 2012, the go ahead was granted to e2v, with Caeleste[11] as design sub-contractor, to develop the quarter sized (880x840pixels) Natural Guide Star Detector (NGSD). This development was funded by FP7[2] OPTICON network and ELT DS. The purpose of the NGSD was twofold: a) to retire architecture and process risks without the high

costs of stitching (required for the final device) or custom Peltier packages; i.e. to be a low cost (relatively) scaled-down demonstrator, and b) to be large enough (> 672x672 pixels) to be able to be used as a detector for first light AO systems on the E-ELT (requiring 8x8 pixels per sub-aperture and 84x84 sub-apertures). The NGSD (see Figure 8 for comparison of NGSD and LGSD) is designed to meet all requirements of the final full size device, the LGSD, except for the pixel format size.

The reader is referred to Figure 11 and Figure 12 to help with the understanding of the following description of the read out of the NGSD/LGSD. Twenty complete rows of pixels (one row of sub-apertures) are read in parallel at the bottom in the case of the NGSD and at both top and bottom (40 pixel rows in total) for the LGSD. Each pixel in these 20 rows (1760*20 in case of LGSD) is read out through its own pre-amplifier, comparator and double data buffer (Register A and B). The pre-amplifier has four programmable gains of x1, x2, x4, and x8 that can be set on a granularity of a single sub-aperture (20x20pixel sub-array). The comparator and Register A along with the common ramp generator and Gray Code Counter implement the single slope ADC. For pipelining purposes, so that data can be serialized and transmitted off-chip while a fresh sample is taken, the ADC data is copied at the end of the conversion to a second Register B so that it is ready to be serialized during the next sub-aperture read period. The pre-amplifier gain, Y-address, and various programmable options of the next sub-aperture to be read are up-loaded through a SPI serial link during the current sub-aperture read. Rows of sub-apertures can thus be addressed sequentially (normal mode) or in any random order (e.g. for reading a sub-region) and gains of each sub-aperture can be independently updated on the fly. For each 40 columns of pixels (two columns of sub-aperture widths), a shift register serializes the 20 rows of pixel data one row at a time using a 110Mhz Double Data Rate (DDR) clock, and transmits the data off-chip through one of the 22 (NGSD) or 88 (LGSD) 220MHz LVDS serial links. A 40 bit LRC40 checksum (detects single bit errors) is calculated each read cycle and can be optionally appended to the data stream.

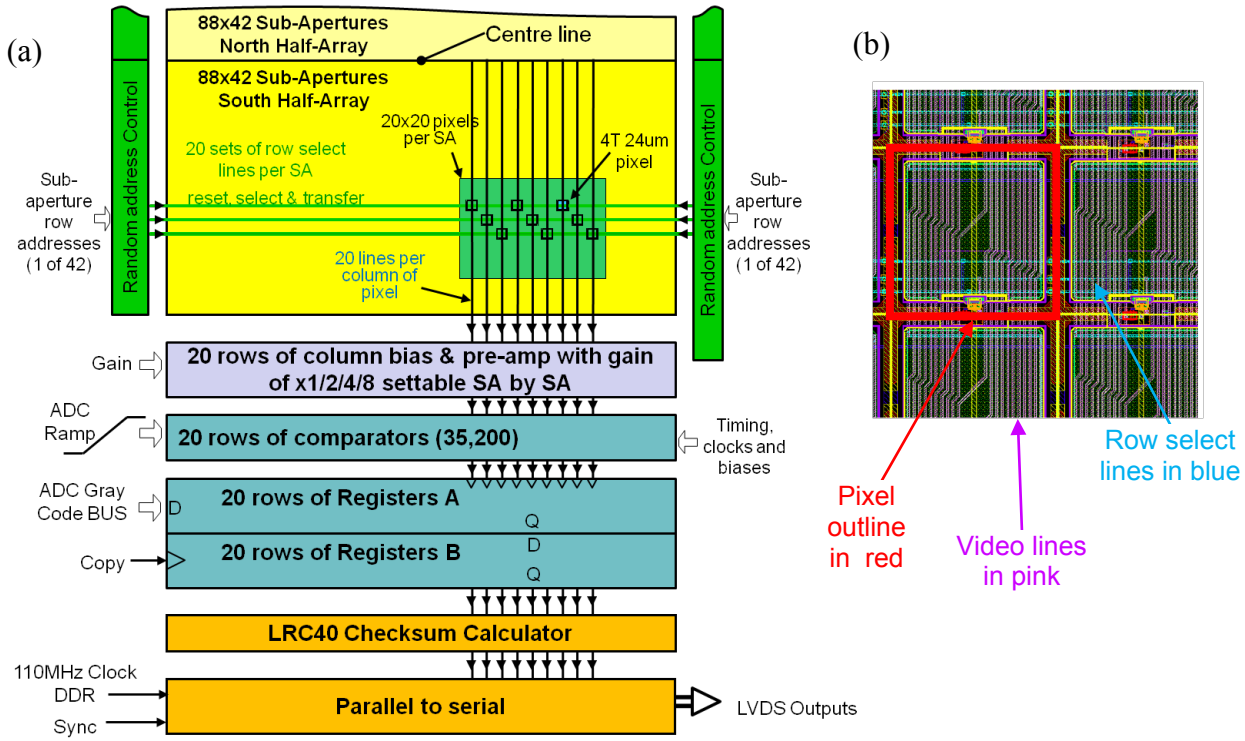

Figure 11. a) Block diagram of the layout of the read out of NGSD/LGSD. b) Layout of the pixel showing the three pixel select lines (reset, select and transfer) and the 20 long video lines that run the length of chip up and down from the center lines.

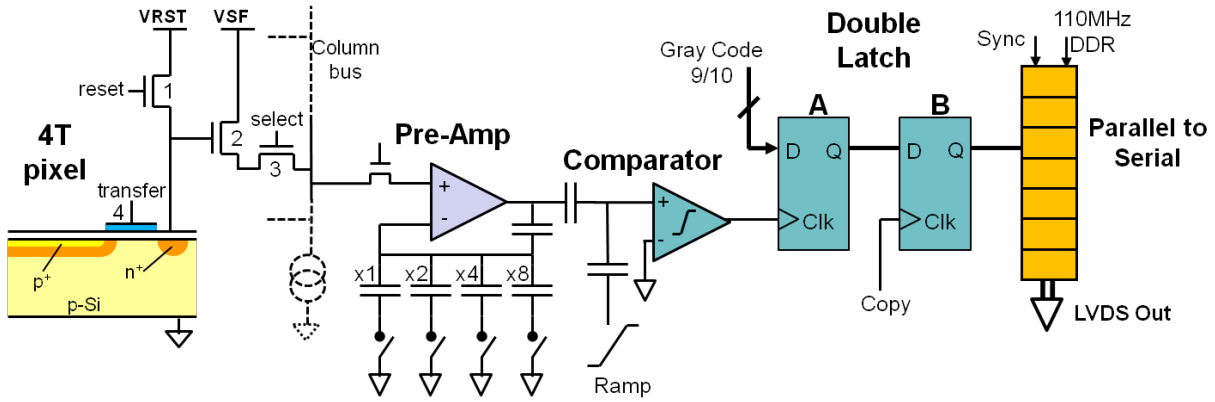

Figure 12. Details of the video processing chain showing pixel, pre-amp, single slope ADC (consisting of comparator, Register A, Gray Code counter, and ramp generator,) and serializer (parallel to serial converter).

To ensure testability of the NGSD, a Mixed Boundary Scan technique is used to program the possibility of injecting and observing signals at various points in the video chain of a column of pixels. This will provide the capability to separately characterize individual components of the video chain, or, if performance issues occur isolate the fault to a particular component. Digital test patterns can be generated to check the serial data transmission and confirm correct operation of the Gray Code counter and associated control circuitry. These same digital test patterns can be used to test the operation of the camera electronics during its development or confirm operation of the camera in the field.

The LGSD will be ~ 45mm x 50mm in size and thus will require stitching. The NGSD will not need to be stitched, and thus, is designed to fit within a single reticle of 25.5mm x 32.5mm. However, the NGSD is designed with stitching in mind (in order to be a true demonstrator), and will follow the stitching plan of Figure 13. Stitching blocks are in chunks of 22x42 sub-apertures, and thus, devices of smaller and larger (especially in the row direction) size can be made from the same reticle set.

Stitching poses many challenges to not only take into account where the stitching lines run, but in placement of

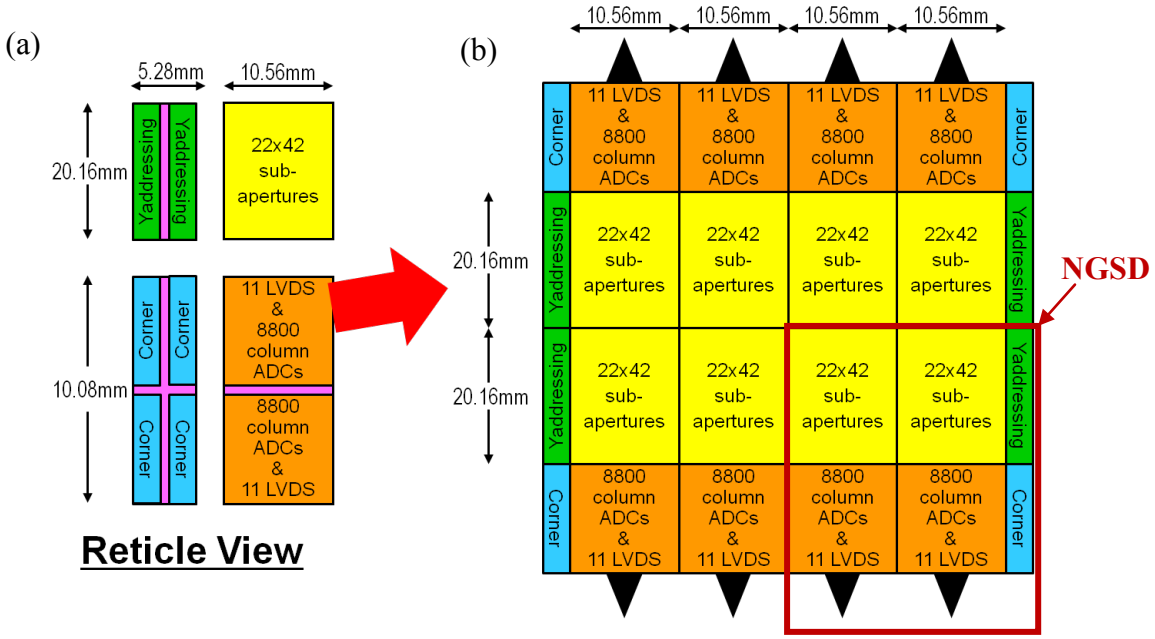

Figure 13. The proposed stitching plan: a) The four reticles from which the whole device on the right can be manufactured, b) Stitching layout of LGSD. NGSD is shown in red. Note that the NGSD will not be stitched.

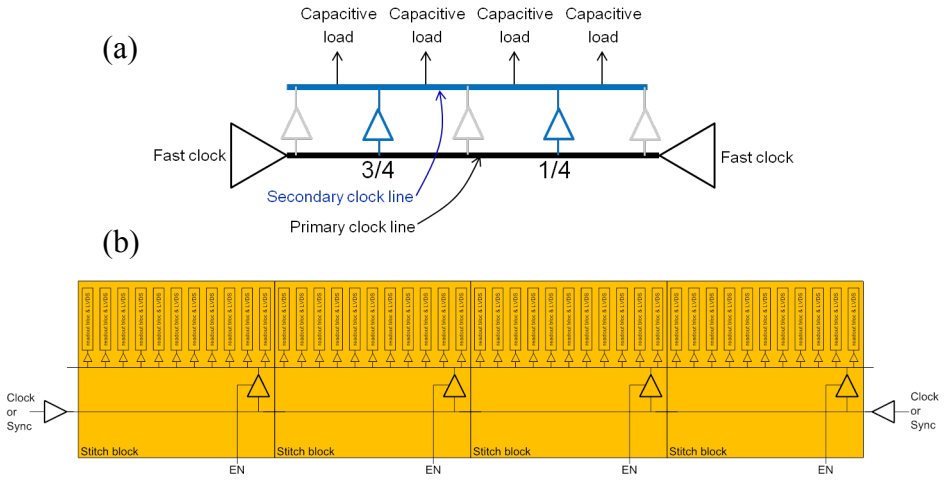

Figure 14. Design of routing of 110MHz fast clocks to keep skew below 0.25ns: a) proposed modified clock tree to distribute the signals; b) detailed implementation.

components. For example, analysis showed a clock tree design was the best way (lowest skew) to distribute the fast 110MHz clocks of the serial interface. To implement this in a stitched design, it was necessary to use a modified scheme (Figure 14) where redundant buffers were inserted in the design, and these need to be enable/disabled as needed depending on the position of the stitch block.

The schematic design of the NGSD is complete and layout has started. Fabrication is scheduled for late autumn with devices available early next year. To ensure that devices are available for first light of the E-ELT, a possible production run of ~15 NGSD devices is envisaged. Upon successful demonstration of the NGSD, the full scale device will be developed (mainly an engineering exercise by this time) followed by a production run of 30-50 LGSD devices.

Also as part of FP7, the same team (Figure 2) as that which designed and built OCam[12] together with the ESO controller design team[14] is performing a controller/camera design study. It is proposed to have a prototype version ready in time for testing the first delivered NGSD devices.

6. SUMMARY

This paper has reported on the excellent measured performance of the current generation of AO WFS detectors at ESO, the e2v L3Vision CCD220, and its deployment in a large number of camera systems on 2nd Generation VLT instruments. The cameras are an AO version of ESO's successful New General detector Controller, AONGC.

Preparation work for the next challenge, the E-ELT, is well advanced. CMOS Imager has been identified as the best technology to fulfill the requirements of the large optical 1680x1680 pixels LGS/NGS WFS detector. A multi-phase, progressive risk reduction development plan should guarantee that devices are available on-time that meets specifications. Measured results of < 3e- read noise at speed, and good image lag and linearity of Technology Demonstrators using 4T pixels and single slope ADCs have clearly validated the CMOS imager approach. The best pixel design and ADC that meet the requirements has been found and is being used in a first generation, 880x840 pixels, quarter-scale device, the NGSD. ESO has formed a good partnership with e2v and Caeleste to develop the detector. The schematic design of the NGSD is complete and layout is proceeding. Fabrication is scheduled for late autumn with devices available early next year.

7. ACKNOWLEGEMENT

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