European Southern Observatory

GIRAFFE

CCD Detector Systems
Detector design and performance report

Version 1.02

VLT-TRE-ESO-13730-2765

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Change Record

Issue/ Revision	Date	Section/Page affected	by	Reason
1	10-June-01 to 25-April-02	All	C.CAVADORE	First release

List of Abbreviations

ADC	Analog to Digital Converter
ADU	Analog to Digital Unit
ATM	Asynchronous Transfer Mode
BOB	Broker for Observation Blocks
CCD	Charge Coupled Device
CFC	Continuous Flow Cryostat
COM1	Commissioning 1
DSP	Digital Signal Processor
EMI	Electromagnetic Immunity
EPER	Extended Pixel Edge Response
FIERA	Fast Imager Electronic Readout Assembly
Gbps	Gigabit/second
IC-LCU	Instrument Control LCU
ICS	Instrument Control System
kps	kilopixel/port/second
LAN	Local Area Network
LCU	Local Control Unit
LRU	Line Replaceable Unit
Mps	Megapixel/port/second
MTBF	Mean Time Between Failures
MIDAS	Image processing software package
ODT	Optical Detector Team
PRISM	Image processing software package
RTD	Real Time Display
TBD	To Be Defined
WS	Workstation

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1 Introduction

This document is meant as a short introduction to the Optical Detector System for GIRAFFE for the ESO Very Large Telescope. It describes the basic hardware and the performance of the system. All additional information can be found in the GIRAFFE Detector Preliminary and Final Design Reviews documents (VLT-TRE-ESO-13740-0000) and will not be repeated in this document.

1.1 Purpose

This document shall be used as a reference document for hardware and the performance of the system i.e. components, readout noise, implemented readout modes, measurements. As reference, one should read the following documents relating to :

1. FIERA CCD software manual : VLT-MAN-ESO-13640-1388 : http://www.eso.org/projects/vlt/sw-dev/wwwdoc/MAR2001/VLT-MAN-ESO-13640-1388/Output/NewFrontCover.html
2. FIERA Software Maintenance Manual: VLT-MAN-ESO-13640-1707
3. FIERA Hardware Manual and System Manual are VLT-MAN-ESO-13640-1844 and VLT-MAN-ESO-13640-1845 respectively
4. EEV44-82 General tests report and performances : http://www.eso.org/projects/odt/EEV-report/EEV44-General-perfs.html
5. PULPO user manual : http://www.eso.org/projects/odt/pulpo/pulpo.html

2 CCD dimensions and data format

Figure 1.1-1 shows how the data of the EEV44-82 are laid out for modes 1, 3, 5 to 7 (see next section for mode definition) on. The 2x2 binning image formed is shown in figure 1.1-2.

There are 50 overscan, 50 prescan pixels visible on the image (RTD display at LCU level, no geometric transformation, all readout modes), 2048 photosensitive columns and 4096 photosensitive rows in binning 1x1, 2048 photosensitive rows in binning 1x2. All the readouts are performed from the **right port**.

The left port can be used as a backup solution in case of problems with the right port :
In that case, the readout patterns located at $INS_ROOT/SYSTEM/COMMON/CONFIGFILES/ccdFg must be modified accordingly. The video cable has to be moved from channel 1 to channel 0. Also keep in mind that the FIERA video board has only one channel with an implemented ADC.

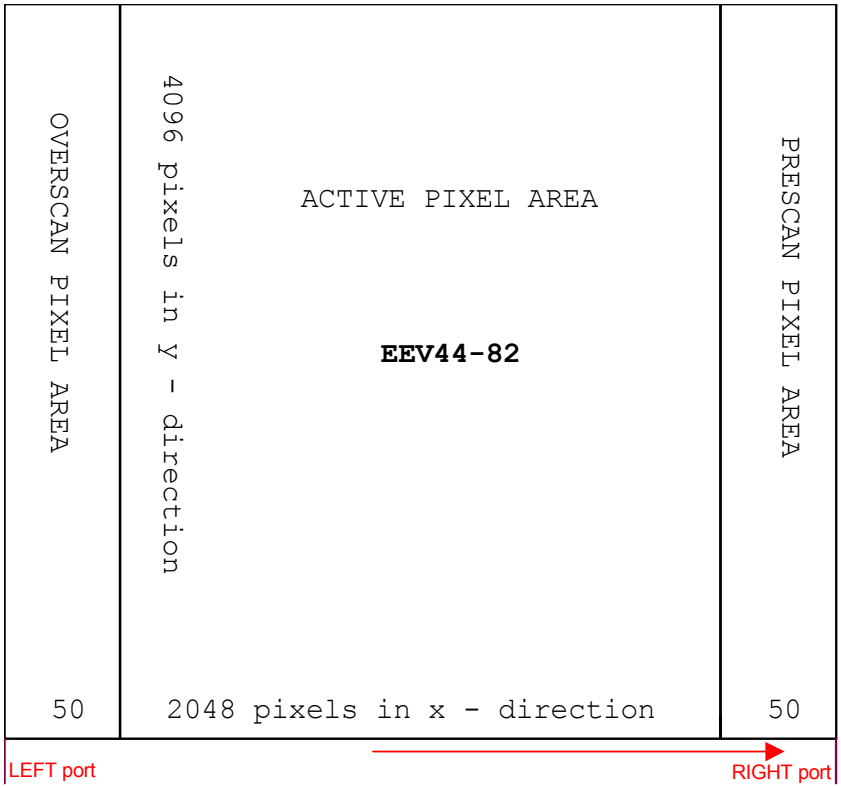


Figure 1.1-1 CCD data layout, 1x1 binning modes

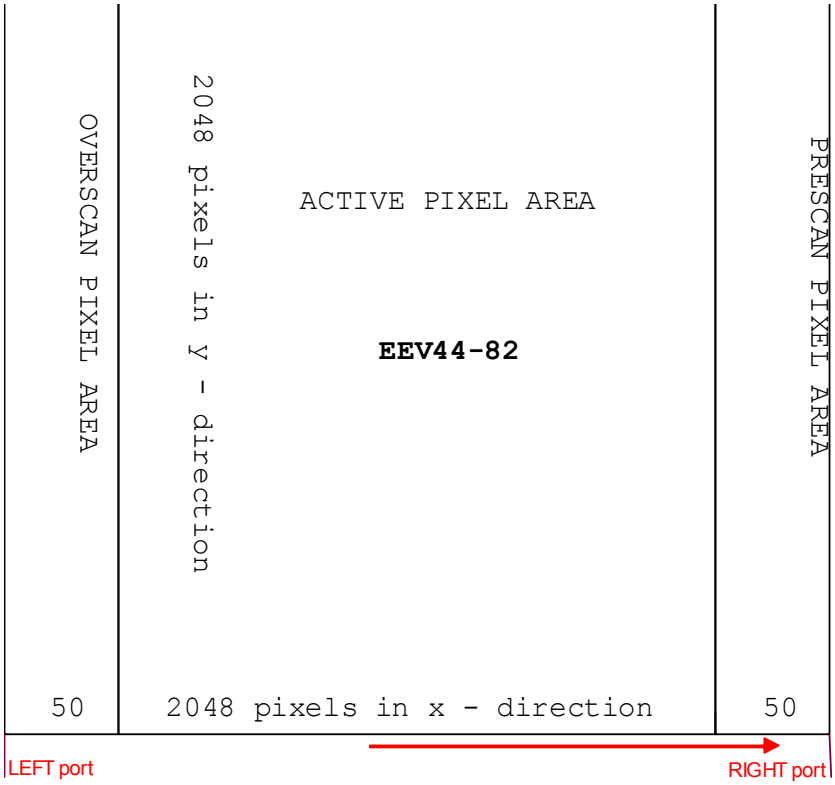


Figure 1.1-2 CCD data layout, 2x2 binning modes

3 GIRAFFE detector – Gain and readout modes

All the pixels are readout from a single port (RIGHT port). Slightly worse performance is obtained from the left port. Mode 7 is an engineering mode that is not offered for science purposes.

GIRAFFE modes	Displayed mode name	Mode description	Image size (Pixels)				Sequences [1]	Readout time (s) [2]
			Prescan	Over-scan	Width	Height		
0	**none**	-	-	-	-	-	-	-
1	**50kpx_1x1_HG**	50,000 pixels per second, 1x1 binning, High gain mode	50	50	2048	4096	***Read_50_1x1.wsq***	190.2
2	**50kpx_1x2_HG**	50,000 pixels per second, 1x2 binning, High gain mode	50	50	2048	2048	***Read_50_1x2.wsq***	97.4
3	**225kpx_1x1_HG**	225,000 pixels per second, 1x1 binning, High gain mode	50	50	2048	4096	***Read_225_1x1.wsq***	42.7
4	**225kpx_1x2_HG**	225,000 pixels per second, 1x2 binning, High gain mode	50	50	2048	2048	***Read_225_1x2.wsq***	22.1
5	**225kpx_1x1_LG**	225,000 pixels per second, 1x1 binning, Low gain mode	50	50	2048	4096	***Read_225_1x1.wsq***	42.7
6	**225kpx_1x2_LG**	225,000 pixels per second, 1x2 binning, High gain mode	50	50	2048	2048	***Read_225_1x2.wsq***	22.1
7	**625kpx_1x1_LG** *(Engineering mode, not offered)*	625,000 pixels per second, 1x1 binning, Low gain mode	50	50	2048	4096	***Read_625_1x1.wsq***	24.2

Bias value table :

GIRAFFE modes	Displayed mode name	Mode description	Offset value [3] ADUs (+/- 1)
1	**50kpx_1x1_HG**	50,000 pixels per second, 1x1 binning, High gain mode	***279***
2	**50kpx_1x2_HG**	50,000 pixels per second, 1x2 binning, High gain mode	***279***
3	**225kpx_1x1_HG**	225,000 pixels per second, 1x1 binning, High gain mode	***181***
4	**225kpx_1x2_HG**	225,000 pixels per second, 1x2 binning, High gain mode	***181***
5	**225kpx_1x1_LG**	225,000 pixels per second, 1x1 binning, Low gain mode	***156***
6	**225kpx_1x2_LG**	225,000 pixels per second, 1x2 binning, Low gain mode	***156***
7	**625kpx_1x1_LG**	625,000 pixels per second, 1x1 binning, Low gain mode	***212***

3.1 Bias spatial stability

[1] Files can be found at $INS_ROOT /SYSTEM/COMMON/CONFIGFILES/ccdFg
[2] Does not include transfer to Instrument Workstation (overhead is about 10-15 sec)
[3] Measured 11th April 2002 at 148K

Bias exposures show some ramp-up effect, along the Y-axis and are stable from readout to readout (2-3 adus). The previous plots where made by median stacking horizontally pixels. High gain mode stands for 0.6 e-/ADU whereas Low Gain modes stand for 2.2 e-/ADU. All measurements were recorded in Garching (Feb 2002).

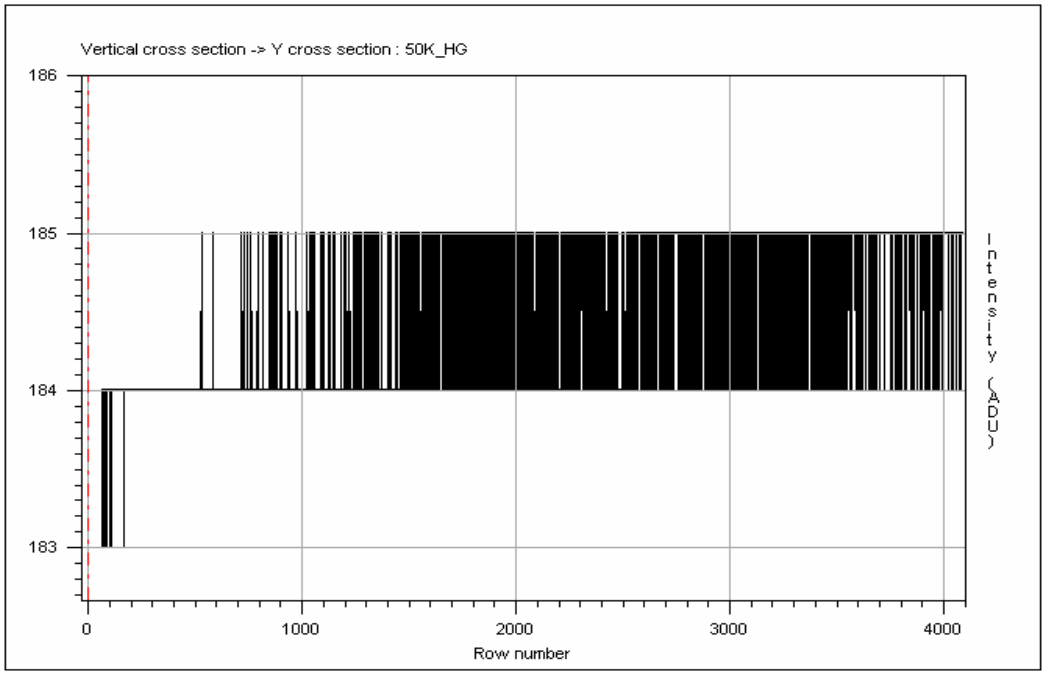


Figure 3.1-1 Bias stability during readout, 50Kpx at High gain

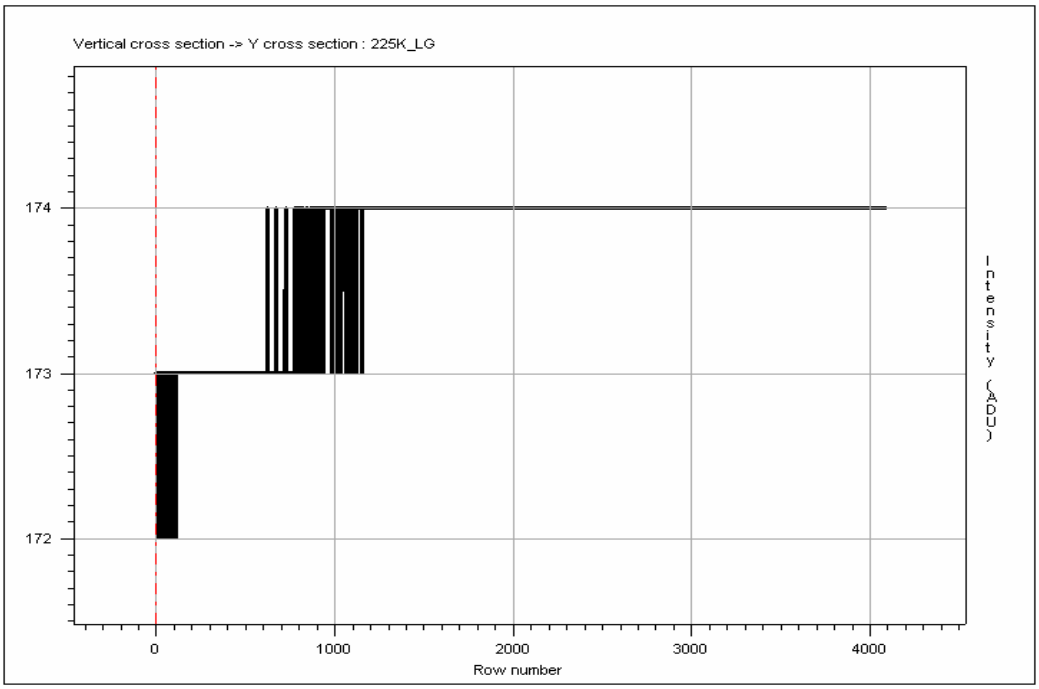


Figure 3.1-2 Bias stability during readout, 225Kpx at Low gain.

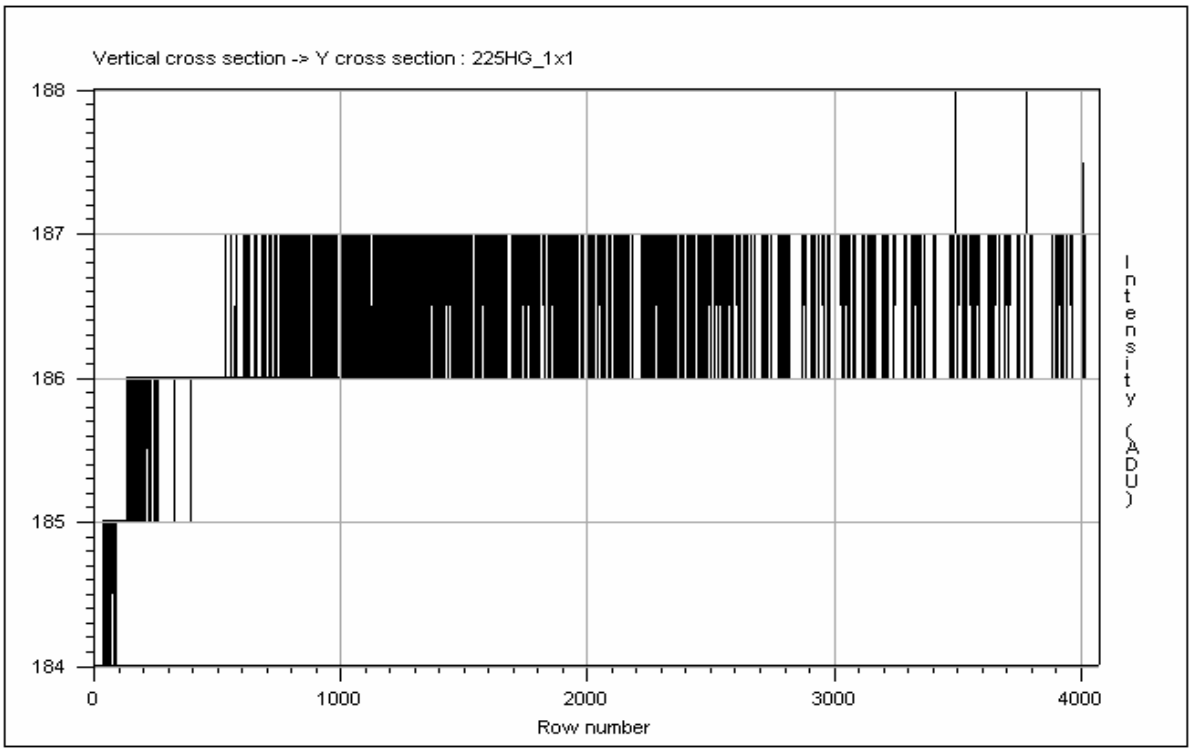


Figure 3.1-3 Bias stability during readout, 225Kpx at High gain

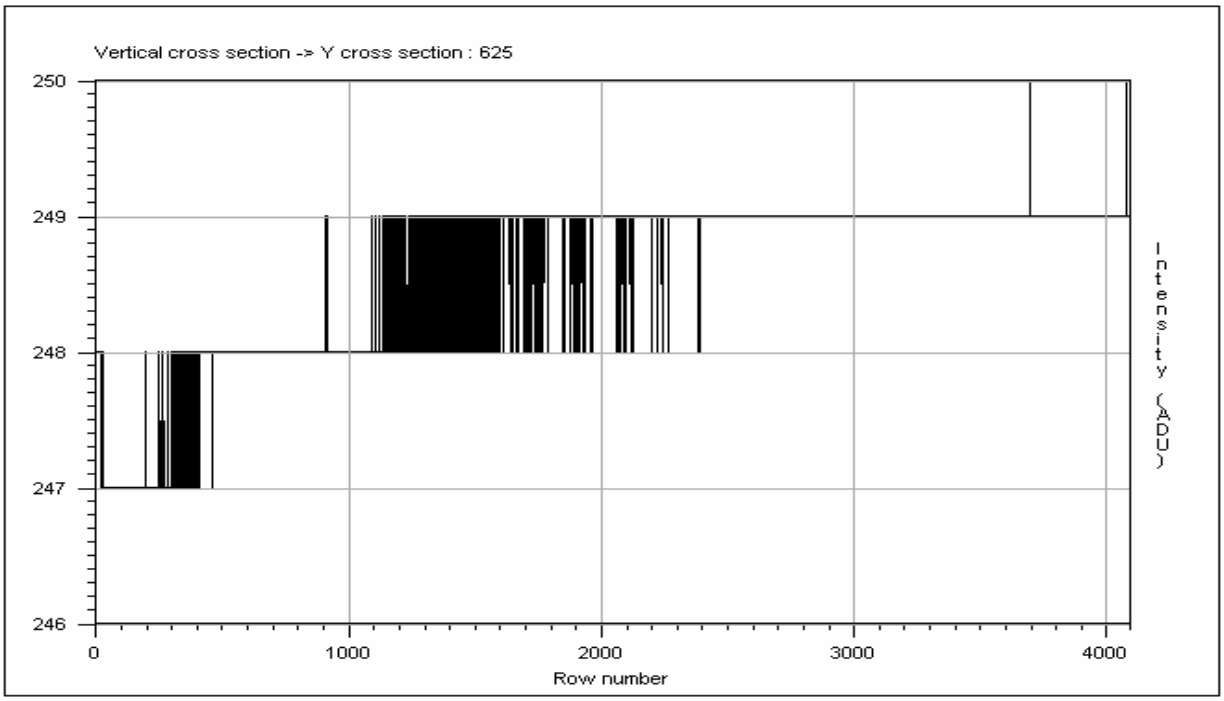


Figure 3.1-4 Bias stability during readout, 625Kpx at Low gain.

4 Detector system components

4.1 System components overview

Figure 4.1-1 Overall system

4.2 Grounding Scheme

To ensure good noise performance and a system free of noise pick-up, ground loops must be eliminated. More particularly no direct earth/ ground connections are allowed between the FIERA power supply box and the FIERA detector head electronics. The thick power cable has its shield connected only to the power supply box, not the detector electronic box. Also, the detector head box temperature sensor cable must not have the shield connected in both sides. Another source of noise is the CFC LN2 exhaust valve switch during operation. If the cable is too close to the preamp box, this can inject noise pattern to the system. To remedy noise pattern injection from the LN2 exhaust valve, one has to ensure that the cable that provides the pulse, is far away from the preamp box and a free-wheel diode is installed at the pins of the CFC exhaust valve.

5 Cryogenic parameters

5.1 CCD temperatures

	Temperature (°Celsius)	Temperature (°Kelvin)	Notes
CCD Table	-127.3	144	At 140K, CTE degradation is visible, 144K is fine and a good trade off. **This is set up by the Pulpo.dat file when Fiera starts up.**
Actual CCD temperature	-120	150	There is an offset of 7 degrees between the CCD carrier table and the CCD surface (silicon).
CFC cold plate temperature	-155	123	Set by the CFC controller
Electronic box shut down temp	40	313	Set by Hardware

The next images (Figure 5.1-1) show how CTE degrades by lowering too much the operating temperature. The readout port used was the right port (readout from left to right).

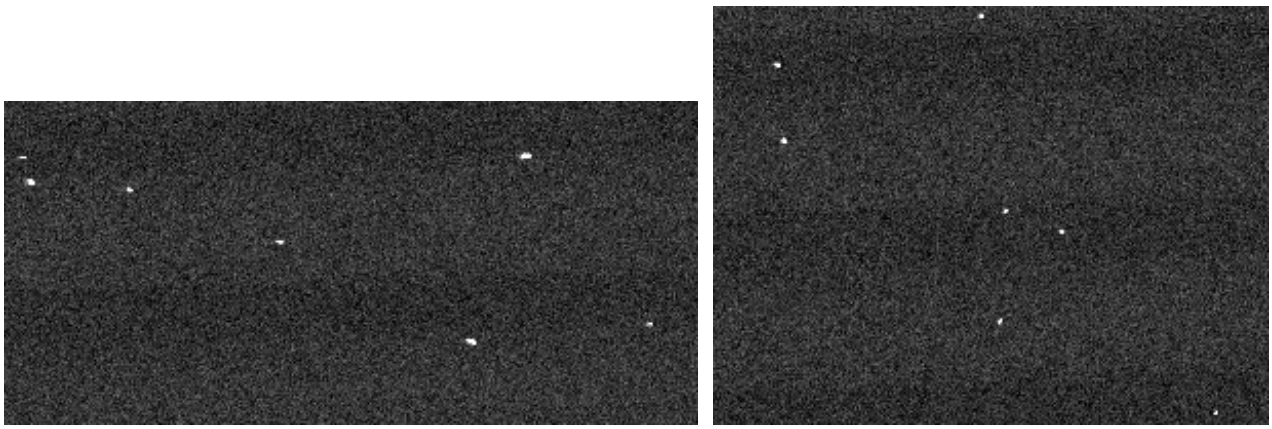


Figure 5.1-1, At 140K, the right side of the CCD is fine, whereas the left side already shows incipient cosmic hits trailing.

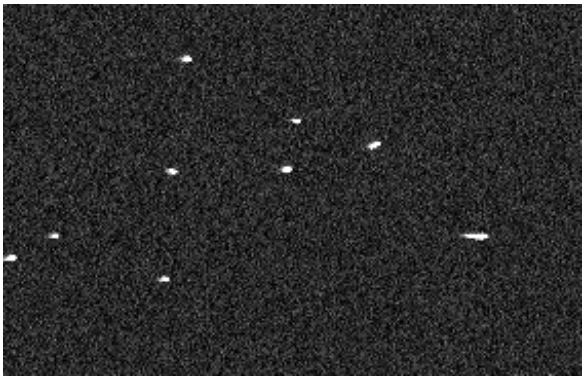


Figure 5.1-2, at 138K,

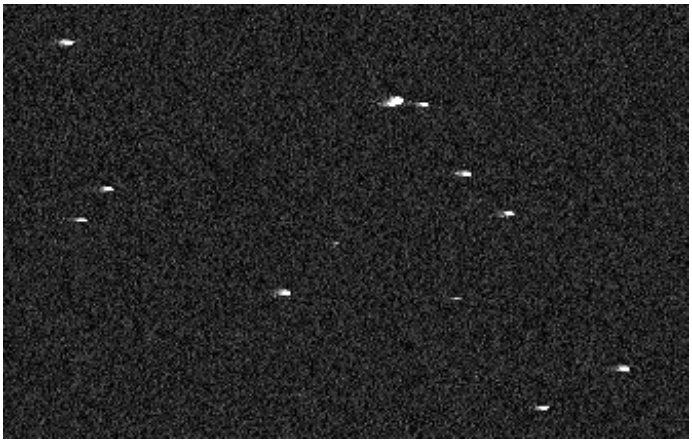


Figure 5.1-3, at 130K

5.2 Telemetry and alarms

These values are intended to set alarm levels at the ICS level. They are supposed to provide alarms when the CCD and the Detector head box temperatures are out of range.

CCD temp min:	145 K
CCD temp max:	155 K
Detector head box, temp min:	273 K
Detector head box temp max:	308 K

6 Fiera detector head electronics and hardware setup

6.1 Video board

	EEV left amp	**EEV right amp**	**Not used**	**Not used**
Videobrd 0	**Channel 0**	**Channel 1**	**Channel 2**	**Channel 3**
Gain0	2 e-/ADU	2 e-/ADU	default	default
Gain1	0.6 e-/ADU	0.6 e-/ADU	default	default
Resistors (gain0)	R 43= 300R // 270R = 142R	R 47 = 300R // 270R = 142R	default	default
Resistors (gain1)	R 42 = 36R	R 46 = 36R	default	default
Filter 0	C21=100pF (τ = 150ns)	C25=100pF (τ = 150ns)	default	default
Filter 1	C22= 220pF (τ = 500ns)	C26= 220pF (τ = 500ns)	default	default
Filter 2	C23= 1nF (τ = 1500ns)	C27= 1nF (τ = 1500ns)	default	default
Filter 3	C24 =2nF= C374 (τ = 3000ns)	C28 = C375 (τ = 3000ns)	default	default
Offset setting	0 to 5 Volts	0 to 5 Volts	default	default

The current video board installed is #59 (June 2001), only one channel is used (currently **1**), the other channel (**0**) could be used, but it **NEEDS** the clock patterns to be modified accordingly to be able to read from that output. No ADCs have been installed in channels 2 and 3.

6.2 Clock driver board

SIMM	DAC	PHASE	OUTPUT RESISTOR
0	BRD_CLKDRV0 CLKDRV_DAC0	SWL	50R
1	BRD_CLKDRV0 CLKDRV_DAC1	SWR	50R
2	BRD_CLKDRV0 CLKDRV_DAC2	RF3	50R
3	BRD_CLKDRV0 CLKDRV_DAC3	RF2L	50R
4	BRD_CLKDRV0 CLKDRV_DAC4	RF1L	50R
5	BRD_CLKDRV0 CLKDRV_DAC5	RF2R	50R
6	BRD_CLKDRV0 CLKDRV_DAC6	RF1R	50R
7	BRD_CLKDRV0 CLKDRV_DAC7	DG	50R
8	BRD_CLKDRV0 CLKDRV_DAC8	IF1	10R
9	BRD_CLKDRV0 CLKDRV_DAC9	IF2	10R
10	BRD_CLKDRV0 CLKDRV_DAC10	IF3	10R
11	BRD_CLKDRV0 CLKDRV_DAC11	empty	10R
12	BRD_CLKDRV0 CLKDRV_DAC12	FRL	10R
13	BRD_CLKDRV0 CLKDRV_DAC13	FRR	10R

The current clock board installed is #45 (June 2001).

6.3 Other boards and parts

Communication board	:	default	(no modifications)
Bias board	:	default	(no modifications)
Power supplies	:	default	(+15V 4A; -15V 4A; +30V 1A; +24V 5A; +5V, 3A)
DSP board (40 MHz)	:	default	(no modifications)
Benner board	:	default	(no modifications)
Sparc computer	:	Intermediate flat SPARC prototype Ultra Iii 440Mhz, the Sparc can be accessed thru the RS232 console thru TTYA or thru the Ethernet RJ45 port at IP=134.171.5.158, this Sparc includes an ATM board that is attached to the Paranal's network.	

6.4 CCD operating voltages

The file's path and name are : $INS_ROOT/SYSTEM/COMMON/CONFIGFILES/volttable.def

```
##############################################################################
#Author :       Cyril CAVADORE
#CAMERA :       Giraffe   ( 1 EEV CCD)
#Purpose:       This is the global voltage definition table
#               European Southern Observatory (ESO)
#Date:          20.11.00
##############################################################################
#  GOBAL VOLTAGE DEFINITION TABLE
#
# This table defines the voltages, which will be applied to peripherals
# at initialization time. It also defines the high and low limits, which may
# be set for these voltages
##############################################################################
# BRD_ID  PERIPH_ID            LOW    HIGH    TOLERANCE     INIT_VAL
#
# Anabias voltages are in 0.001 volts
#
##############################################################################
#  BIASBRD 0 is for the EEV CCD-44 in the mosaic
##############################################################################
# BRD_ID  PERIPH_ID            LOW    HIGH    TOLERANCE     INIT_VAL
```

```
# CONNECTOR P0 - A
# STANDARD CONFIGURATION FOR EEV44-82 CCDs

# BRD_ID  PERIPH_ID           LOW     HIGH    TOLERANCE      INIT_VAL
BRD_ANABIAS0 ANB_PRESET_VOLT_A       -3500   -1000   10000          -3500 #OG1R
BRD_ANABIAS0 ANB_PRESET_VOLT_B       -2500   -1000   10000          -2500 #OG2R
BRD_ANABIAS0 ANB_PRESET_VOLT_C       20000   26000   10000          23000 #ODR
BRD_ANABIAS0 ANB_PRESET_VOLT_D       11000   15000   10000          11000 #RDR
BRD_ANABIAS0 ANB_PRESET_VOLT_E       20000   26000   10000          25000 #JDR
BRD_ANABIAS0 ANB_PRESET_VOLT_F       20000   26000   10000          25000 #JDL
BRD_ANABIAS0 ANB_PRESET_VOLT_G       10000   23000   10000          18500 #DD
BRD_ANABIAS0 ANB_PRESET_VOLT_H        9000   15000   10000          11000 #RDL
BRD_ANABIAS0 ANB_PRESET_VOLT_I       20000   26000   10000          23000 #ODL
BRD_ANABIAS0 ANB_PRESET_VOLT_J       -2500   -1000   10000          -2500 #OG2L
BRD_ANABIAS0 ANB_PRESET_VOLT_K       -3500   -1000   10000          -3500 #OG1L


#The anabias board also has an opto isolated peripheral

BRD_ANABIAS0 ANB_OPTOOUT      0      32767   4              255


#
################################################################################
# Clock driver rail voltages are in 0.001 volts
#
################################################################################
#CLOCKDRIVER BOARD 0 is for the EEV CCD44 in the mosaic
################################################################################
#
#
# BRD_ID       PERIPH_ID        LOW        HIGH     TOLERANCE   INIT_VAL
#
#   CONNECTOR PO-A
#
BRD_CLKDRV0 CLKDRV_DAC0_LO     -6000      -5000     1000       -5000 #SWL
BRD_CLKDRV0 CLKDRV_DAC0_HI      5000       6000     1000        5000
BRD_CLKDRV0 CLKDRV_DAC1_LO     -6000      -5000     1000       -5000 #SWR
BRD_CLKDRV0 CLKDRV_DAC1_HI      5000       6000     1000        5000
BRD_CLKDRV0 CLKDRV_DAC2_LO     -6000      -5000     1000       -6000 #RF3
BRD_CLKDRV0 CLKDRV_DAC2_HI      5000       6000     1000        6000
BRD_CLKDRV0 CLKDRV_DAC3_LO     -6000      -5000     1000       -6000 #RF2L
BRD_CLKDRV0 CLKDRV_DAC3_HI      5000       6000     1000        6000
BRD_CLKDRV0 CLKDRV_DAC4_LO     -6000      -5000     1000       -6000 #RF1L
BRD_CLKDRV0 CLKDRV_DAC4_HI      5000       6000     1000        6000
BRD_CLKDRV0 CLKDRV_DAC5_LO     -6000      -5000     1000       -6000 #RF2R
BRD_CLKDRV0 CLKDRV_DAC5_HI      5000       6000     1000        6000
BRD_CLKDRV0 CLKDRV_DAC6_LO     -6000      -5000     1000       -6000 #RF1R
BRD_CLKDRV0 CLKDRV_DAC6_HI      5000       6000     1000        6000
BRD_CLKDRV0 CLKDRV_DAC7_LO     -6000      -5000     1000       -6000 #DG
BRD_CLKDRV0 CLKDRV_DAC7_HI      5000       6000     1000        6000
#
#     CONNECTOR PO-B
#
BRD_CLKDRV0 CLKDRV_DAC8_LO    -12000      -4000     1000       -8000 #IF1
BRD_CLKDRV0 CLKDRV_DAC8_HI     -2000       4000     1000        3000
BRD_CLKDRV0 CLKDRV_DAC9_LO    -12000      -4000     1000       -8000 #IF2
BRD_CLKDRV0 CLKDRV_DAC9_HI     -2000       4000     1000        3000
BRD_CLKDRV0 CLKDRV_DAC10_LO   -12000      -4000     1000       -8000 #IF3 Makes the line reset
BRD_CLKDRV0 CLKDRV_DAC10_HI    -2000       4000     1000        3000
BRD_CLKDRV0 CLKDRV_DAC11_LO    -0000      -0000     1000       -0000 #empty
BRD_CLKDRV0 CLKDRV_DAC11_HI     0000       0000     1000        0000
BRD_CLKDRV0 CLKDRV_DAC12_LO    -6000      -4000     1000       -6000 #FRL
BRD_CLKDRV0 CLKDRV_DAC12_HI     6000       8000     1000        6000
BRD_CLKDRV0 CLKDRV_DAC13_LO    -6000      -4000     1000       -6000 #FRR
BRD_CLKDRV0 CLKDRV_DAC13_HI     6000       8000     1000        6000



#
# Gain should be interpreted as follows
# There are two gains, gain1 is on the preamp, gain2 is on the video board.

# Gain1 =
#     3 == 1.5
#     1 == 2.25
#     0 == 3.0
#
# Gain2 =
#     0 = Minimum (2.5)
#     1 = Maximum (12.5)
```

```
#
# INIT VALUES, overridden by modes files,  High_gain_filtre_xxx.volt
# or Low_gain_filtre_xxx.volt


# BRD_ID  PERIPH_ID           LOW     HIGH    TOLERANCE      INIT_VAL

BRD_VIDBRD0 VID_GAIN1_CHAN0       0       3       0               1
BRD_VIDBRD0 VID_GAIN1_CHAN1       0       3       0               1
BRD_VIDBRD0 VID_GAIN1_CHAN2       0       3       0               1
BRD_VIDBRD0 VID_GAIN1_CHAN3       0       3       0               1

BRD_VIDBRD0 VID_GAIN2_CHAN0       0       1       0               0
BRD_VIDBRD0 VID_GAIN2_CHAN1       0       1       0               0
BRD_VIDBRD0 VID_GAIN2_CHAN2       0       1       0               0
BRD_VIDBRD0 VID_GAIN2_CHAN3       0       1       0               0

BRD_VIDBRD0 VID_FILT_CHAN0        0       3       0               0
BRD_VIDBRD0 VID_FILT_CHAN1        0       3       0               0
BRD_VIDBRD0 VID_FILT_CHAN2        0       3       0               0
BRD_VIDBRD0 VID_FILT_CHAN3        0       3       0               0

BRD_VIDBRD0 VID_TESTVID_CHAN0     0       1       0               0
BRD_VIDBRD0 VID_TESTVID_CHAN1     0       1       0               0
BRD_VIDBRD0 VID_TESTVID_CHAN2     0       1       0               0
BRD_VIDBRD0 VID_TESTVID_CHAN3     0       1       0               0

#
# Video Offsets are in 0.001 volts
#
# BRD_ID  PERIPH_ID           LOW     HIGH    TOLERANCE      INIT_VAL
#
# Overridden by *volt files, just for INIT

BRD_VIDBRD0 VID_OFFSET_CHAN0    0   65535    6553            0
BRD_VIDBRD0 VID_OFFSET_CHAN1    0   65535    6553            0
BRD_VIDBRD0 VID_OFFSET_CHAN2    0   65535    6553            0
BRD_VIDBRD0 VID_OFFSET_CHAN3    0   65535    6553            0
```

The current bias board installed is #35 (June 2001).

7 CCD system performance data

7.1 Gain and readout noise

The following table shows noise figure that have been measured in March 2002 (Garching HQ).

Mode	Readout speed [kHz]	Dynamic (ADC limited) [Ke-]	Readout port	Conversion factor [e^-/ADU]	Readout noise [e^-]
1	**50kpx_1x1_HG**	41	Right	0.63 ± 0.05	2.03 ± 0.09
2	**50kpx_1x2_HG**	41	Right	0.63 ± 0.05	2.03 ± 0.09
3	**225kpx_1x1_HG**	41	Right	0.58 ± 0.05	3.15 ± 0.09
4	**225kpx_1x2_HG**	41	Right	0.58 ± 0.05	3.15 ± 0.09
5	**225kpx_1x1_LG**	142	Right	2.18 ± 0.05	4.14 ± 0.09
6	**225kpx_1x2_LG**	142	Right	2.18 ± 0.05	4.14 ± 0.09
7	**625kpx_1x1_LG**	142	Right	2.21 ± 0.05	4.67 ± 0.09

The following table shows noise figure that have been measured in April 2002, at Paranal before COM1.

Mode	Readout speed [kHz]	Dynamic (ADC limited) [Ke-]	Readout port	Conversion factor [e^-/ADU]	Readout noise [e^-]
1	**50kpx_1x1_HG**	41	Right	0.63 ± 0.05	2.05 ± 0.09
2	**50kpx_1x2_HG**	41	Right	0.65 ± 0.05	2.10 ± 0.09
3	**225kpx_1x1_HG**	41	Right	0.61 ± 0.05	3.28 ± 0.09
4	**225kpx_1x2_HG**	41	Right	0.60 ± 0.05	3.34 ± 0.09
5	**225kpx_1x1_LG**	142	Right	2.25 ± 0.05	4.21 ± 0.09
6	**225kpx_1x2_LG**	142	Right	2.26 ± 0.05	4.17 ± 0.09
7	**625kpx_1x1_LG**	142	Right	2.30 ± 0.05	4.90 ± 0.09

All the plots were recorded at ESO, HQ, Paranal plots after installation are similar **(no noise pick-up).**

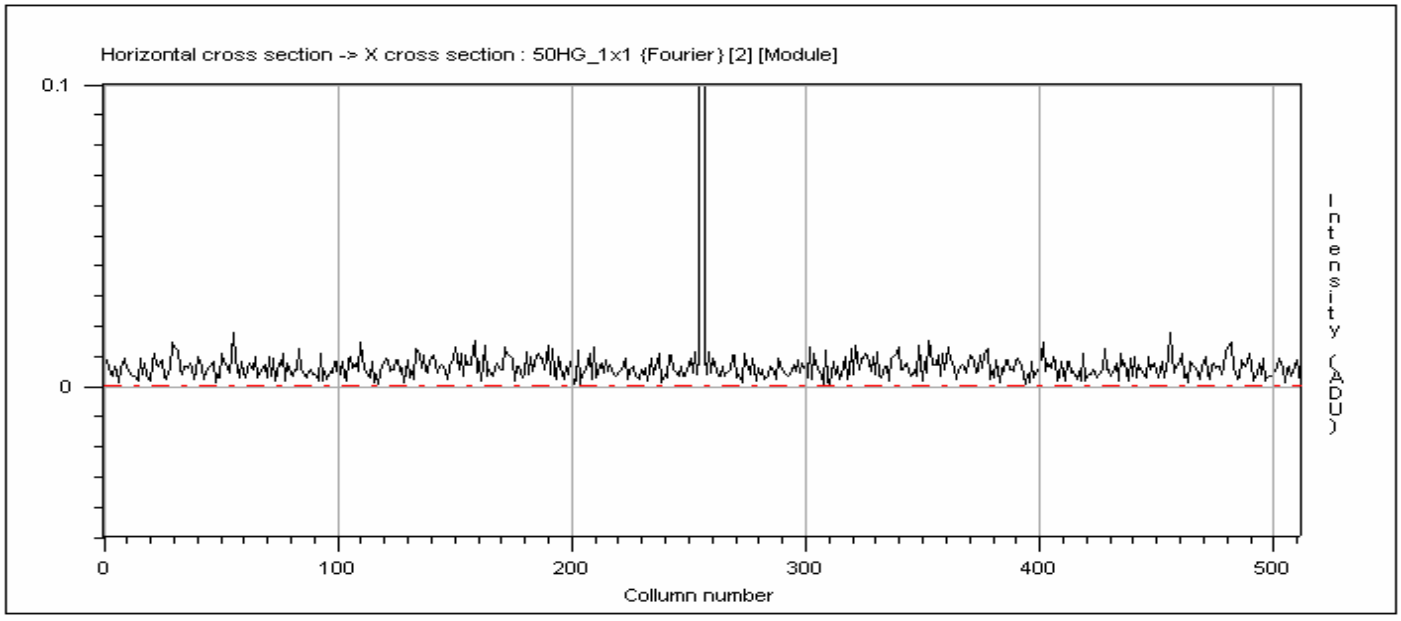


Figure 7.1-1 Noise power spectrum at 50Kpx/sec, 512x512 window, nothing but white noise is visible.

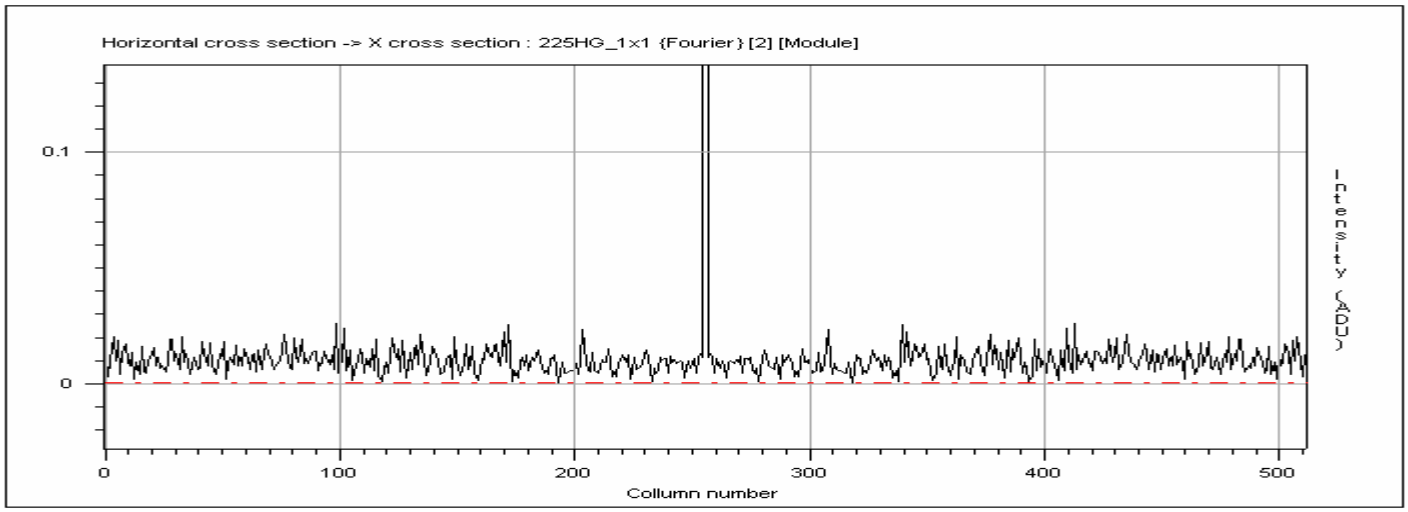


Figure 7.1-2 Noise power spectrum at 225Kpx/sec High Gain, 512x512 window.

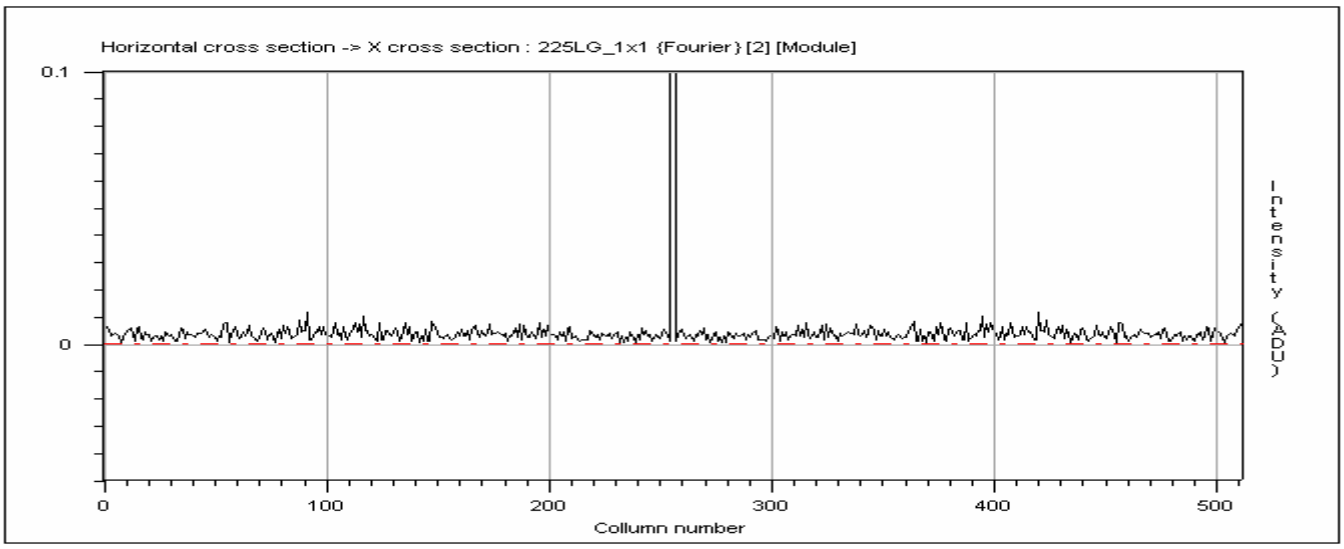


Figure 7.1-3 Noise power spectrum at 225Kpx/sec Low gain, 512x512 window.

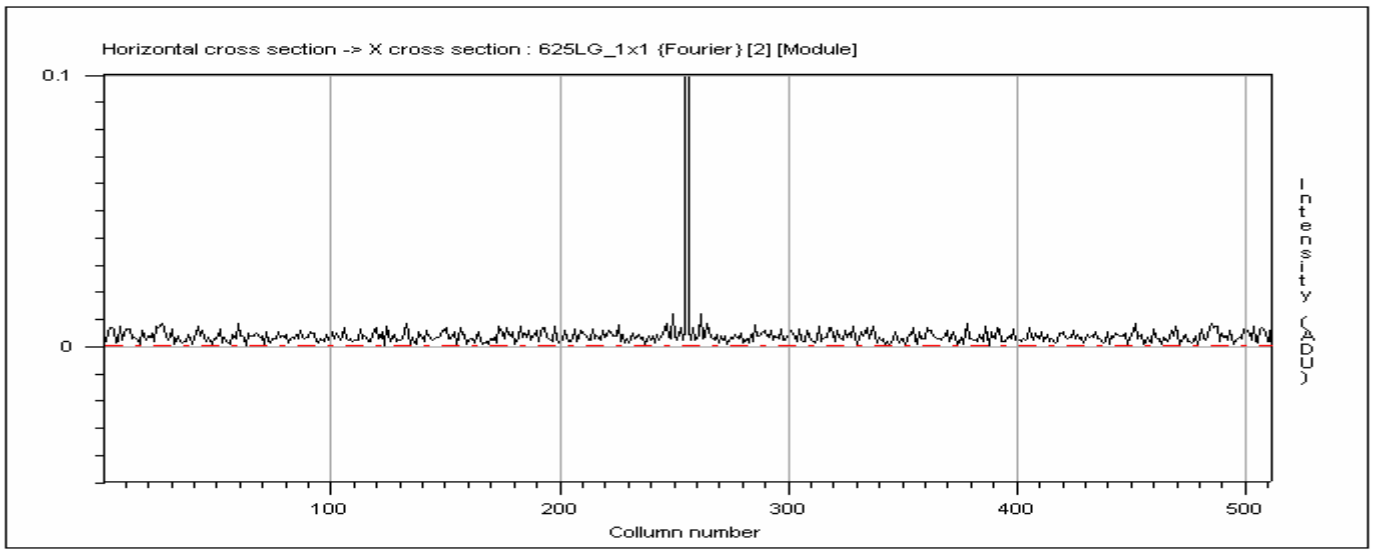


Figure 7.1-4 Noise power spectrum at 625Kpx/sec, 512x512 windo.

7.2 The scientific CCD (BRUCE)

7.2.1 CCD specification

CCD serial number	:	7173-3-1
CCD alias name	:	BRUCE
Type	:	EEV CCD-44 Back Ill. AR coated
Number of pixels	:	[H] 2048 [V] 4102
Number of outputs	:	2
Pixel size	:	15x15 µm
Channel potential voltage	:	11.8V
Intrinsic pixel full-well	:	150Ke-

7.2.2 Cosmetic defects

Cosmetic defects table			
Low level flat field			Mean number of electrons per pixel ≈ 3000
Type of defect	***Location (x,y)***		***Number of pixels affected***
Dark pixels	(451, 3893)- (1972, 2935) – (1287, 2127) – (1176, 1539) – (586, 398)		Single pixel, or cluster of 3x3
Hot pixels	416,1463		3 columns starting from these locations : column 416,417 and 418
Bias image			0 sec dark exposure
12000 pixels above 5σ			
Type of defect	***Location (x,y)***		***Number of pixels affected***
Hot pixels	416,1463		3 columns starting from these locations : column 416,417 and 418
Long exposure dark images			10 exp. of 1800 sec each
13108 pixels above 5σ			
Kind of defect		***Location X,Y***	***Number of pixels affected***
Hot pixels		416,1463	3 columns starting from these locations : column 416,417 and 418
Hot spot		1840, 4098	Charge injection on top of the image (see figure 7-2-6)
Horizontally aligned hot pixels		1839, 3833	5-10 pixels, aligned horizontally
Horizontally aligned hot pixels		212, 3828	5-10 pixels, aligned horizontally
Horizontally aligned hot pixels		1079, 3835	5-10 pixels, aligned horizontally
Horizontally aligned hot pixels		385, 3827	5-10 pixels, aligned horizontally
Horizontally aligned hot pixels		1929, 3832	5-10 pixels, aligned horizontally
Single pixels		-	Spread over the image

The following images (Figures 7.2-1 to 7.2-5) show full frame images (2x4K) where X=1 and Y=1 are located at the bottom left of the image. Y is horizontal and increases when going towards right. X is vertical, increasing towards up. The right readout port of the CCD is located at X=2048 and Y=1.

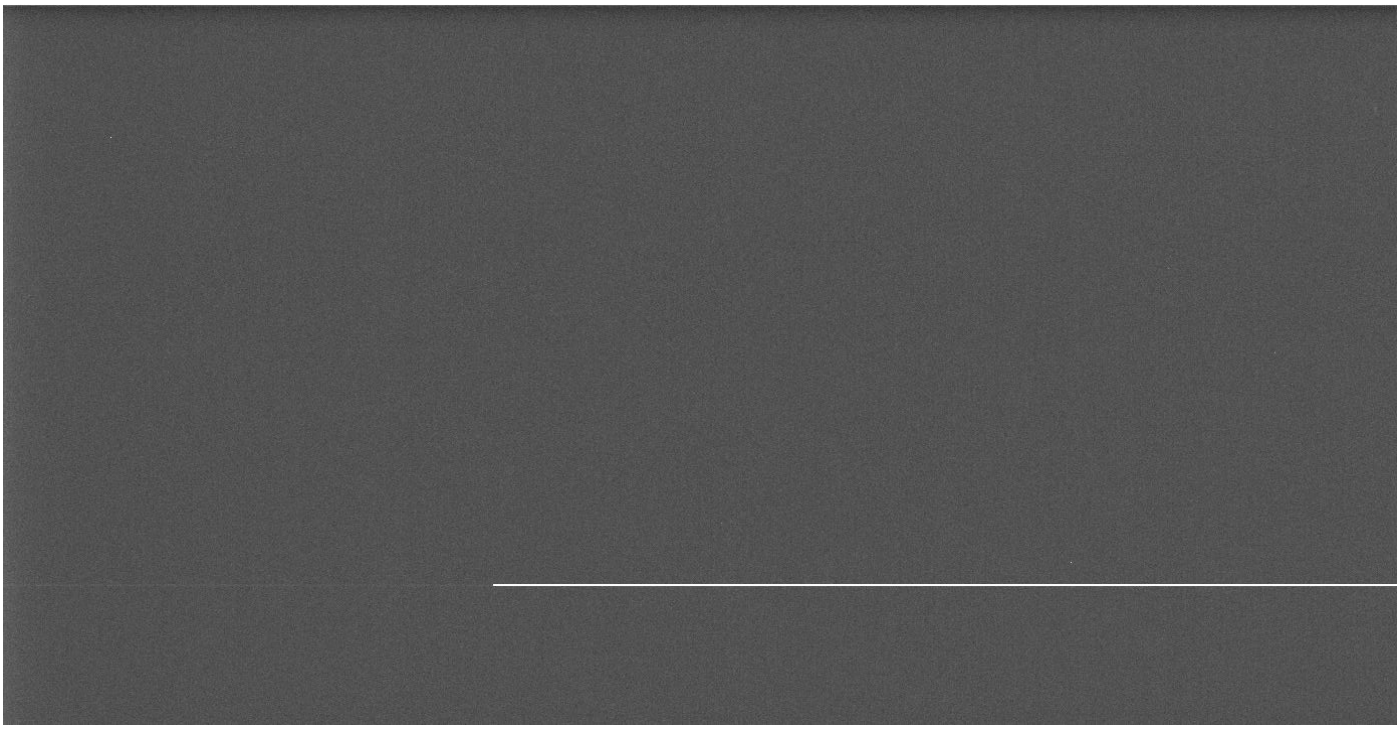


Figure 7.2-1 Full frame bias image

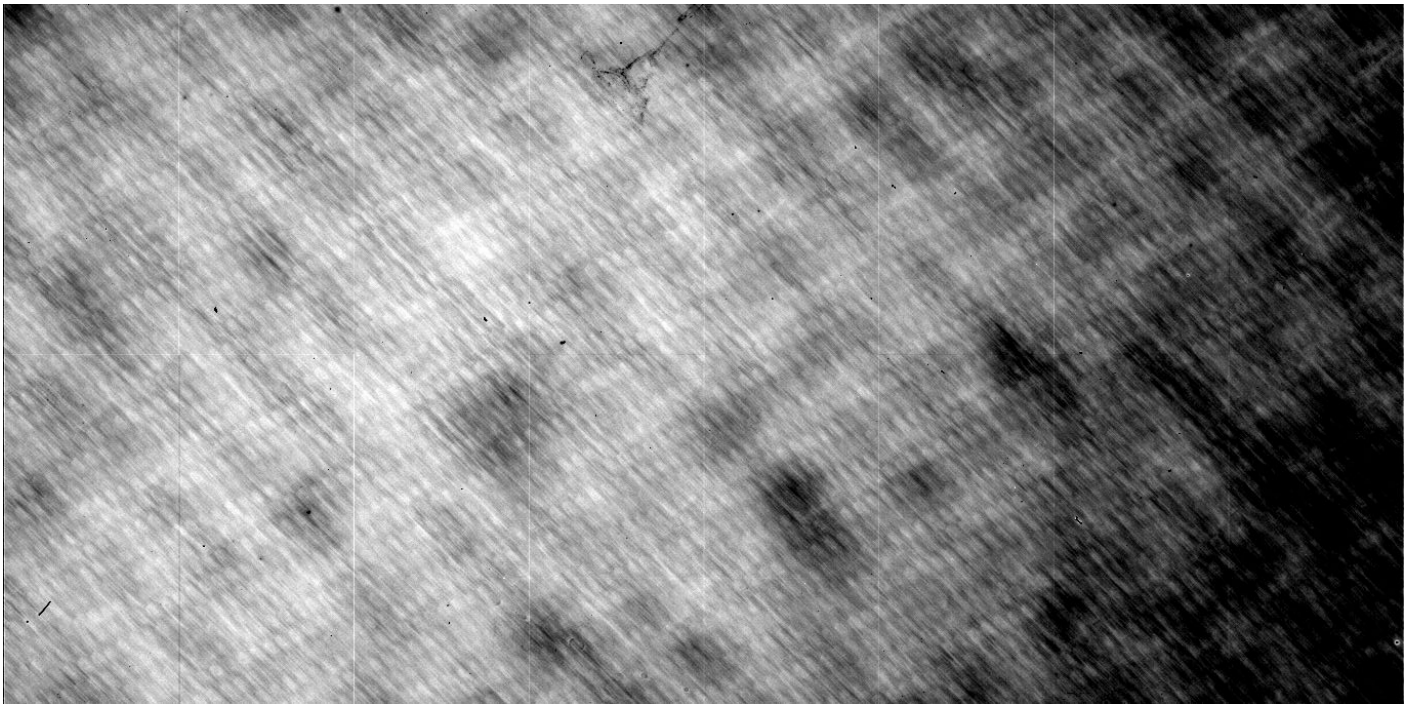


Figure 7.2-2 Full frame Flat field image, 350 nm, 5nm bandwidth.

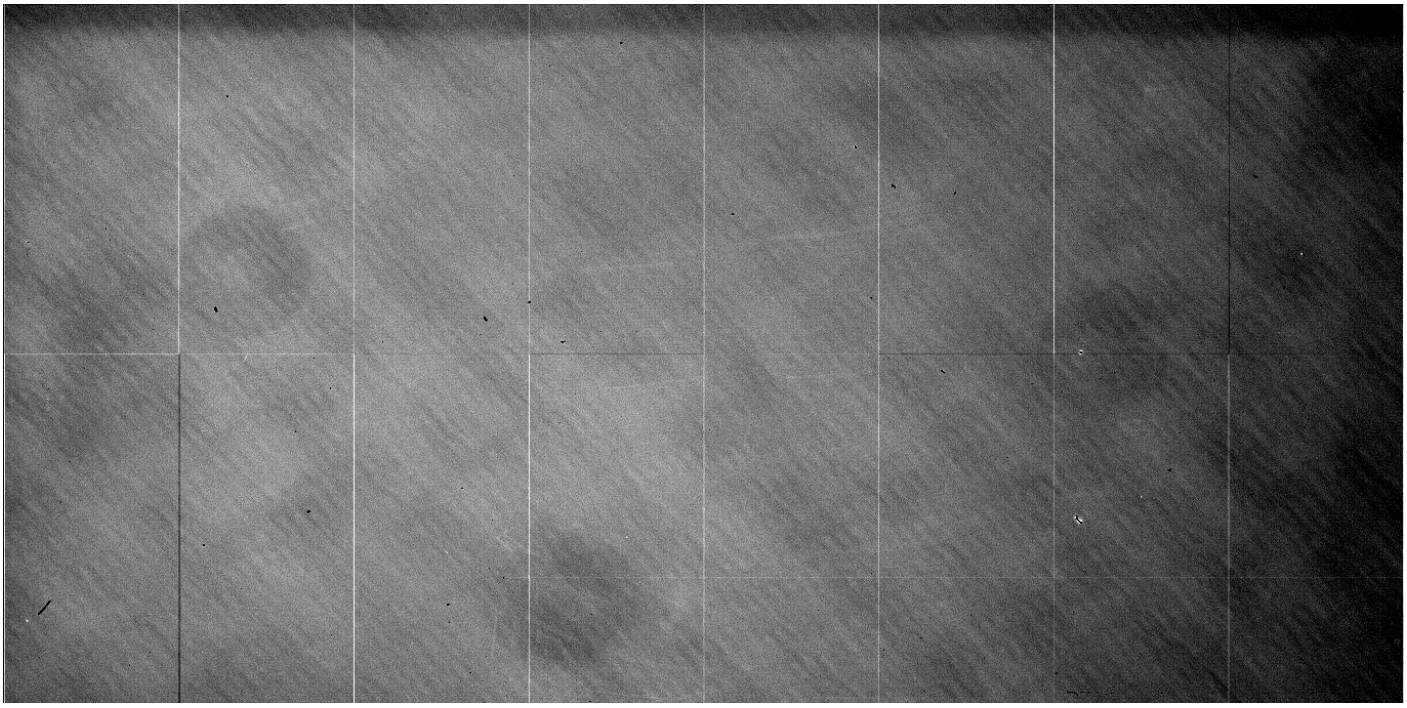


Figure 7.2-3 Full frame flat field image,600 nm, 5nm bandwidth

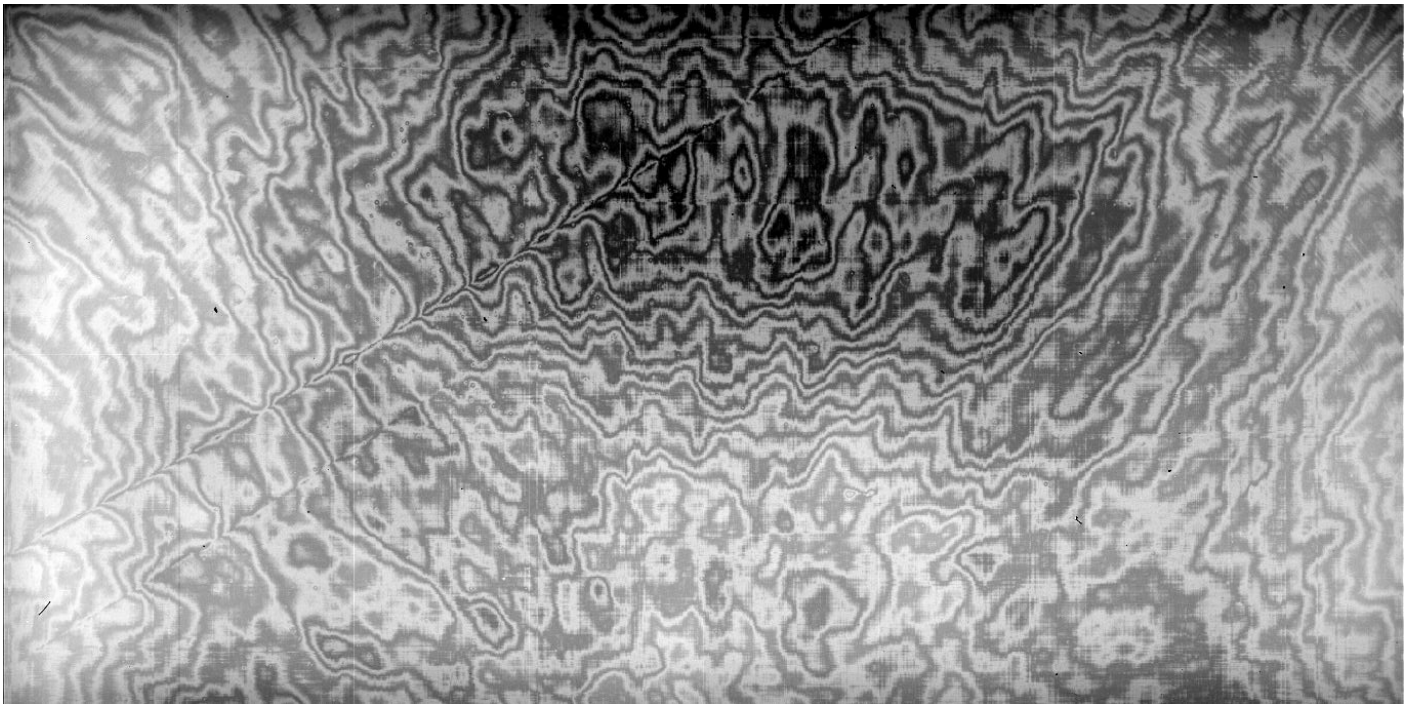


Figure 7.2-4 Full frame flat field image,900 nm, 5nm bandwidth.

Stitching and diamond pattern at lees than 350nm can be corrected by flat fielding. Fringing can be subtracted with sky night super flats.

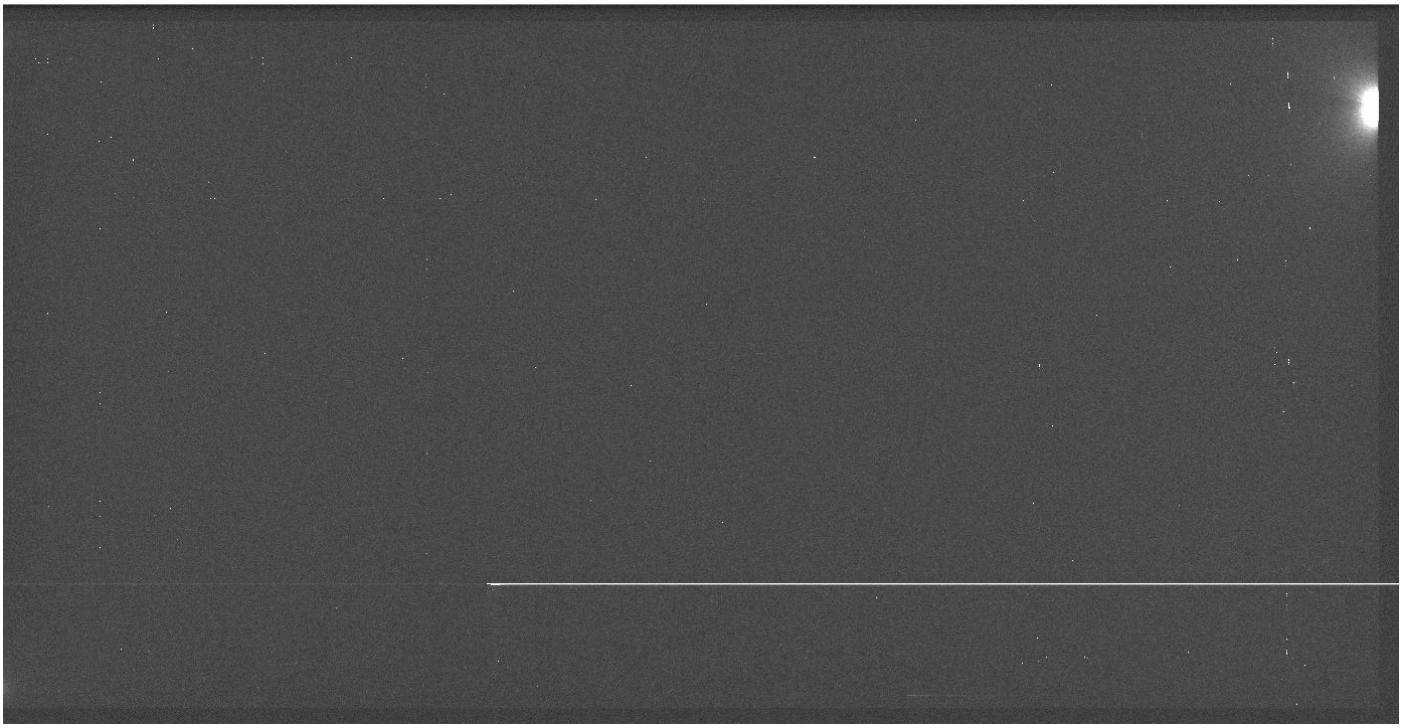


Figure 7.2-5, 4x3600s dark exposure median stacked.

Glowing at the CCD top section is visible in exposures longer than 60s, and is related to charge injection by the CCD guard ring. This charge injection is caused by a manufacturing defect on the CCD and cannot be recovered. This effect is proportional to the exposure time and also exhibits a dependency on temperature. The figure 7.2-6 shows this effect on a 600x300 pixels sub window image where X and Y are Cartesian oriented. After installation at Paranal (April 2002), this effect seems to have disappeared (Figure 7.2-8). No explanation at that date.

Figure 7.2-6, 7200s, 0.58e-/ADU, top right glowing at X=1844,Y= 4096

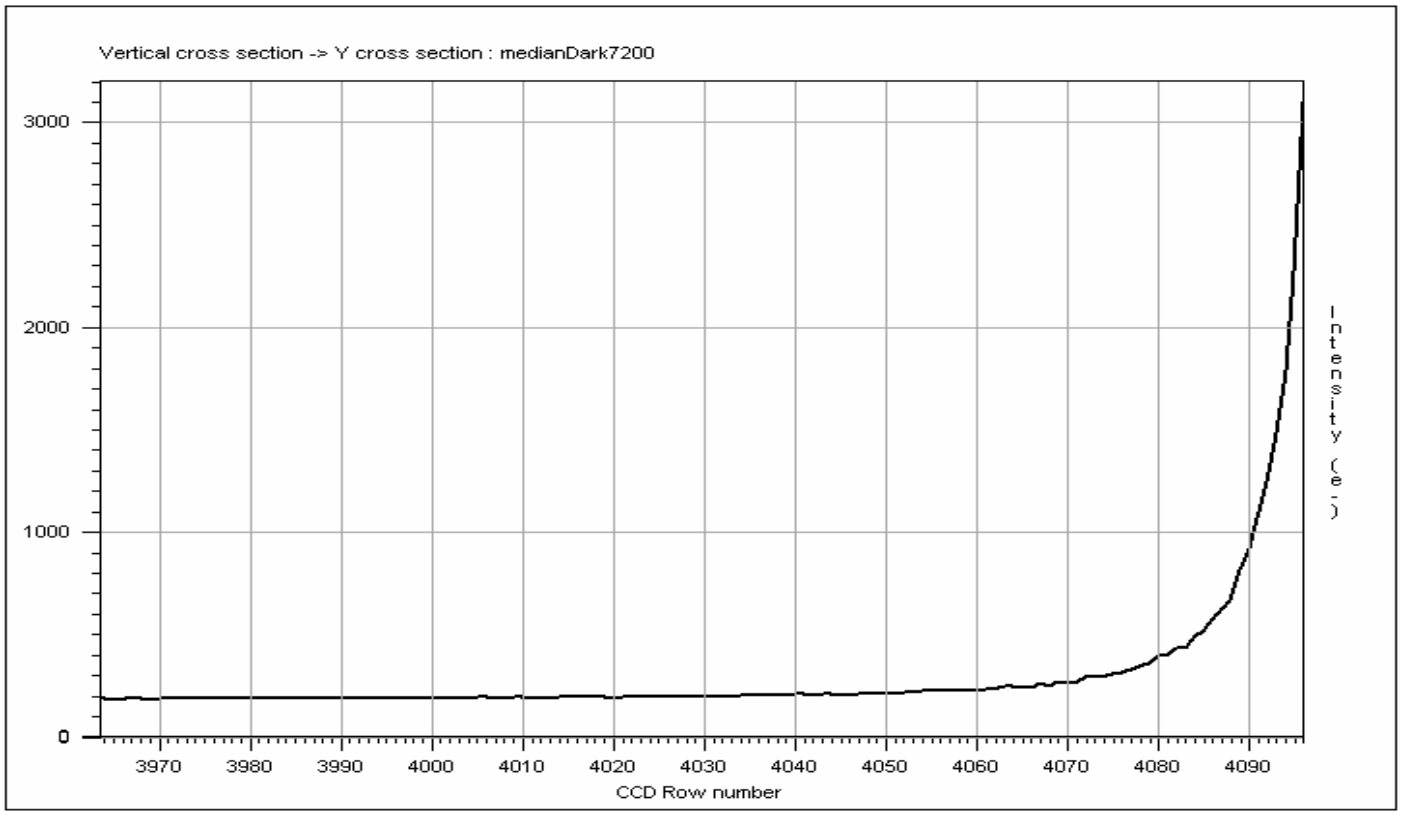


Figure 7.2-7, 7200s dark exposure, vertical cross section ending where the glowing is the strongest.

Figure 7.2-8, 900s, 0.58e-/ADU, top right of the CCD at X=1844,Y= 4096.

A filamentary dust particle of 1 mm has settled over the CCD surface during transportation to Paranal (see next figure). This filament can disappear from a day to another, or after break of vacuum, but it could also remain for a long time. The only way to remove it would be to dismount and clean the whole top head section.

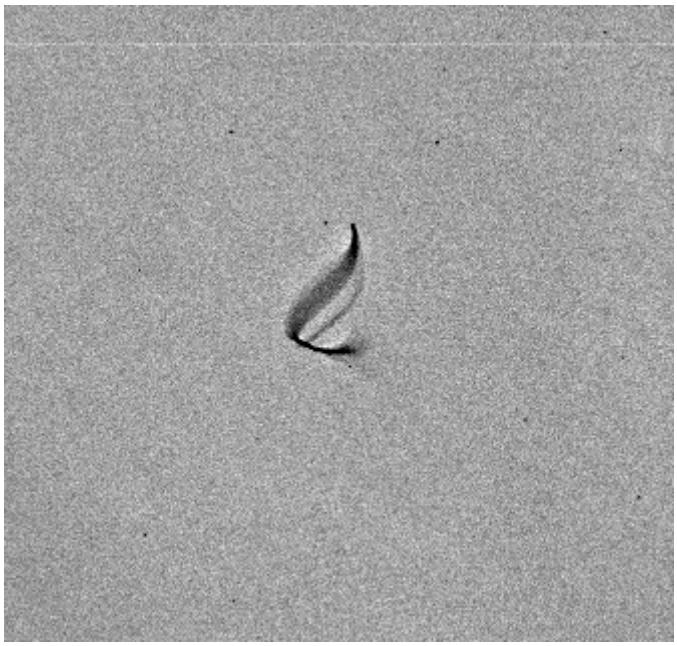


Figure 7.2-9, Dust particle, (flat field exposure), extending over a 47x67 pixel box at X=1922,Y= 905.

7.2.3 Dark current

Mean dark current is less than 1.0 ± 0.2 e-/pixel/hour @ -120 ºC. Ten 1800sec exposure frames were used.

7.2.4 Cosmic ray hit event

Cosmic hit event rate: 0.8 ± 0.4 events/min/cm²

7.2.5 Charge Transfer Efficiency

Vertical CTE to Port A/B : 0.9999988 (six 9s)
Horizontal CTE to Port A/B : 0.9999996 (six 9s)

The EPER method was used, at the ESO CCD testbench at –110C. Beware that a decrease in temperature has an immediate degrading effect on the horizontal CTE, see section related to CCD temperatures (5.1).

7.2.6 Linearity

Linearity for the Left output amplifier : +0.63/-0.47 %
Linearity for the Right output amplifier : +0.62/ -0.45 %

The linearity has been measured at the CCD Test bench Facility in Garching, with a gain of 2.2e- ADU (range was 130Ke-). At Paranal (figures 7.2-10 to 12), linearity measurements have been made (11th April 2002). Only readout modes 1, 3 and 5 have been measured because modes 1-2, 3-4 and 5-6 are identical. Several exposures leading to different light levels using the Giraffe spectrograph shutter have been used to compute the linearity. As a light source, the internal Giraffe flat screen and lamp where used.

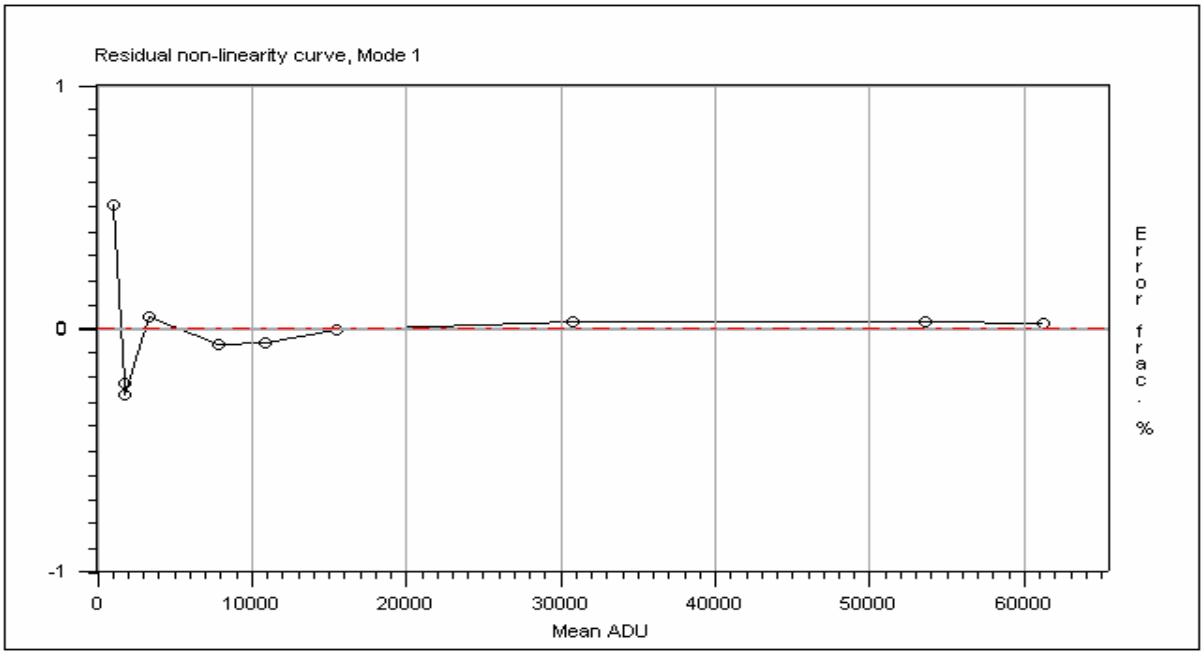


Figure 7.2-10, Mode 1 Non linearity

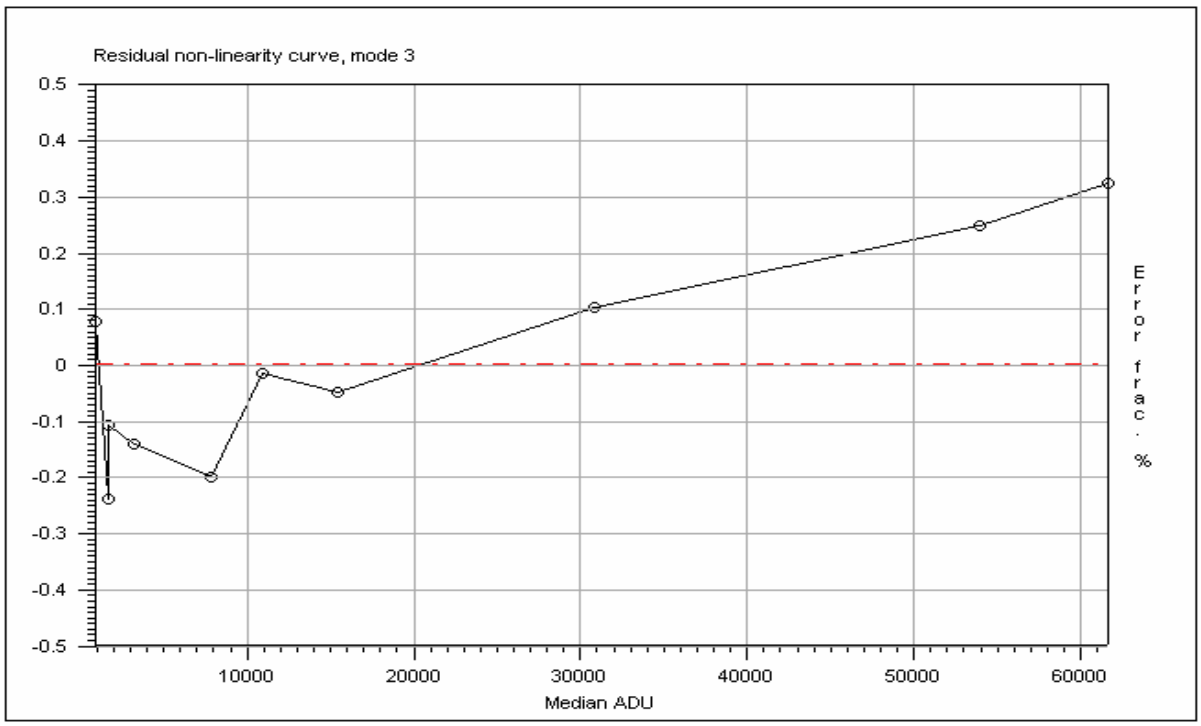


Figure 7.2-11, Mode 3 Non linearity

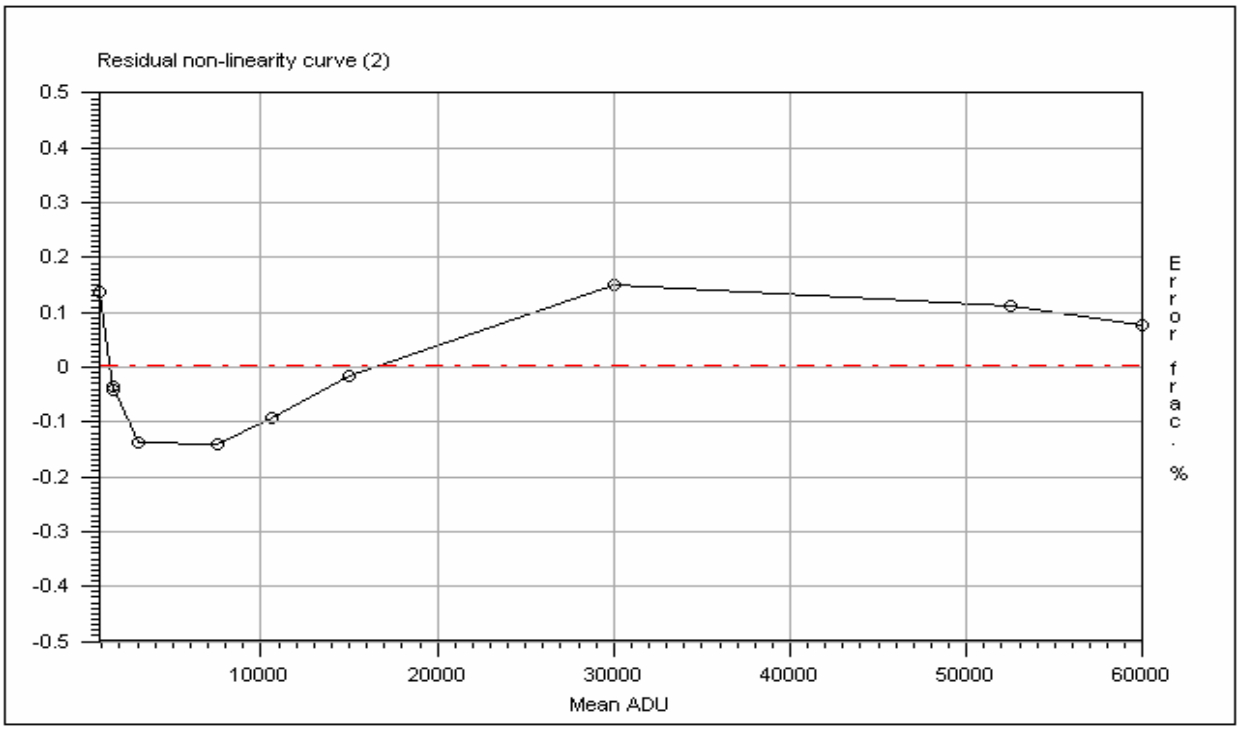


Figure 7.2-12, Mode 5 Non linearity

7.2.7 Dynamic range vs readout modes

The 16 bit ADC provides 65335 ADU of dynamic range. The later has to be multiplied by the conversion factor for a given readout mode to get the dynamic range expressed in electrons. This gives a dynamic range of **145Ke-** with a gain of **2.2e-/ADUs** (readout modes 1 to 4) and **43Ke-** with a gain of **0.65e-/ADUs** (readout modes 5 to 7).

7.2.8 Overexposure

No eclipse[4] or trailing effects due to over saturation have been observed. Counts are always going up to 65535 whatever the mode used. The overexposure has produced 150Ke-

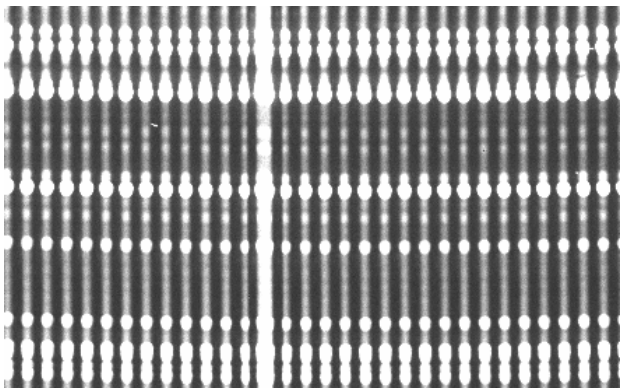


Figure 7.2-13, 120sec exposure spectra calibration (Thorium Lamp) over exposed.

[4] Eclipse effect means that at the center of an over-saturated star, all the values are clipped to zero instead of 65535. The effect looks like a star that has been eclipsed by a dark mask.

The next figures have been recorded in Garching, showing how the blooming extents according to photon per pixel. The CCD full well is 150Ke-. The changes within the central 9x9 pixels area are given with the next figures.

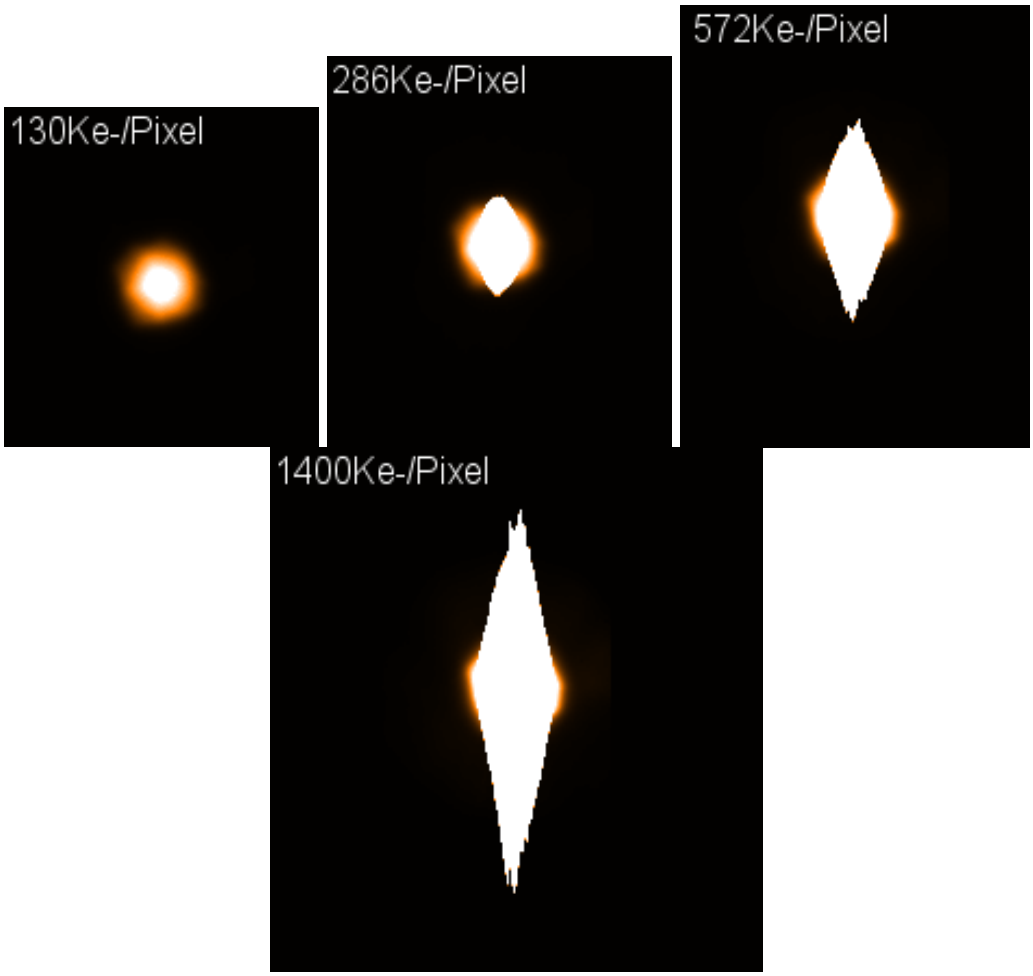


Figure 7.2-14, Different exposures showing the blooming extensions vs photon rate per pixel, spot size is 30x30 pixels.

7.2.9 Readout direction

Toward the right port for ALL modes

7.2.10 CCD flatness

The CCD flatness is reported into the next figure has been measured at Marconi Company. Peak to peak non-flatness is 20 microns, average is 10 microns.

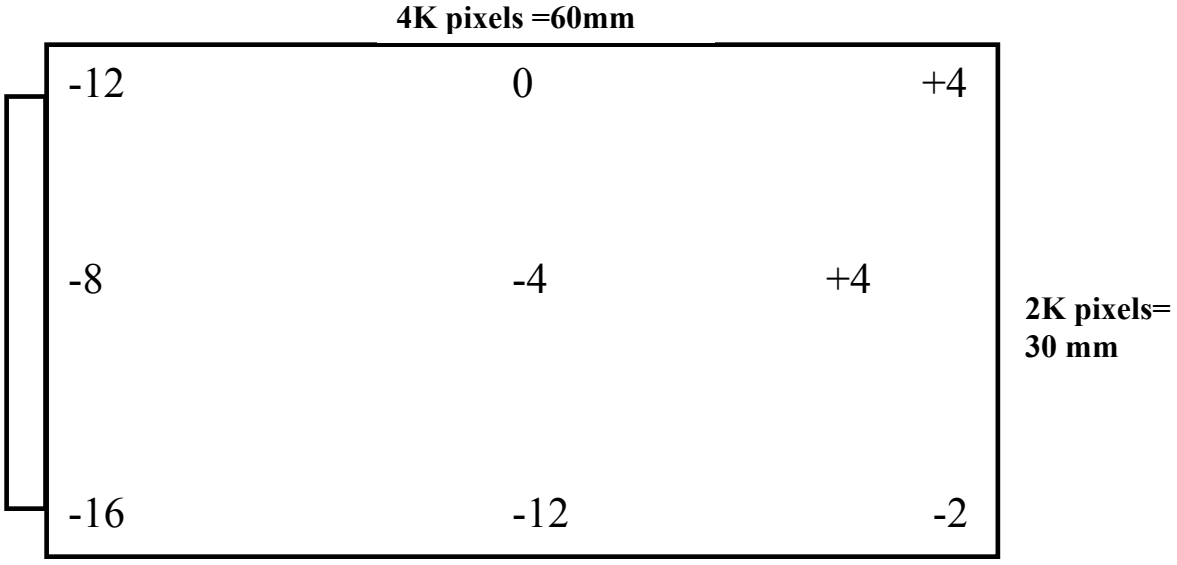


Figure 7.2-15, CCD Top view including the deviations in microns from a reference.

7.2.11 Quantum efficiency (QE) and photo-response non uniformity (PRNU)

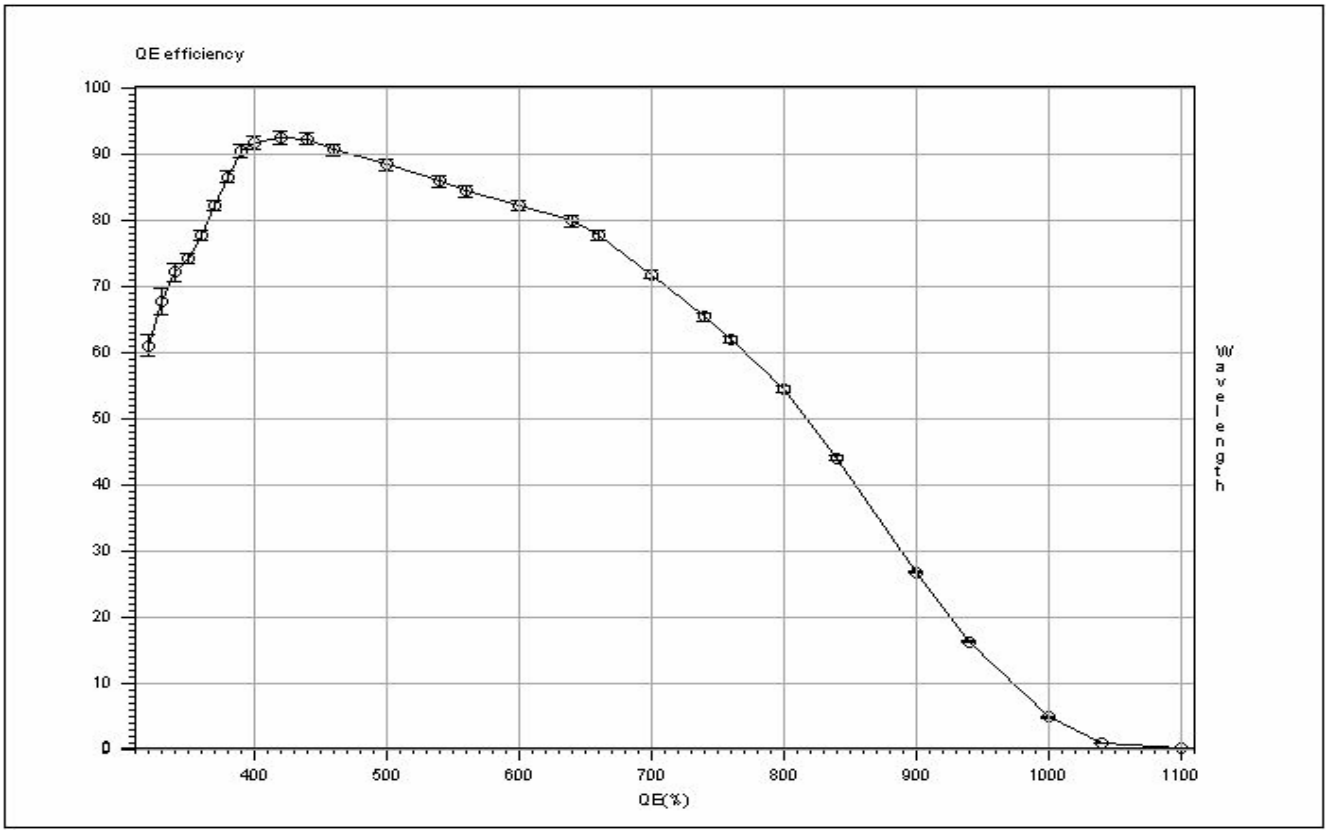


Figure 7.2-16, Quantum Efficiency curve

Quantum efficiency and PRNU table (F/3 incoming beam and 5nm bandwidth)

Wavelength	PRNU (%)	QE(%)	Error(%)
320	1.7	60.8	±1.7
330	1.5	67.5	±1.9
340	1.4	71.9	±1.4
350	1.4	74.0	±0.7
360	1.4	77.6	±0.7
370	1.3	82.0	±0.8
380	1.1	86.3	±0.8
390	1.0	90.3	±0.9
400	0.9	91.5	±0.9
420	0.8	92.2	±0.9
440	0.8	92.1	±0.9
460	0.7	90.4	±0.9
500	0.7	88.2	±0.8
540	0.7	85.7	±0.8
560	0.7	84.1	±0.8
600	0.7	81.9	±0.8
640	0.7	79.6	±0.7
660	0.7	77.5	±0.7
700	0.9	71.5	±0.6
740	1.0	65.2	±0.5
760	1.2	61.7	±0.5
800	1.6	54.3	±0.4
840	2.1	43.9	±0.3
900	2.5	26.6	±0.2
940	3.9	16.1	±0.12
1000	7.5	4.65	±0.03
1040	8.1	0.8	±0.005
1100	11.7	0.09	±0.0006

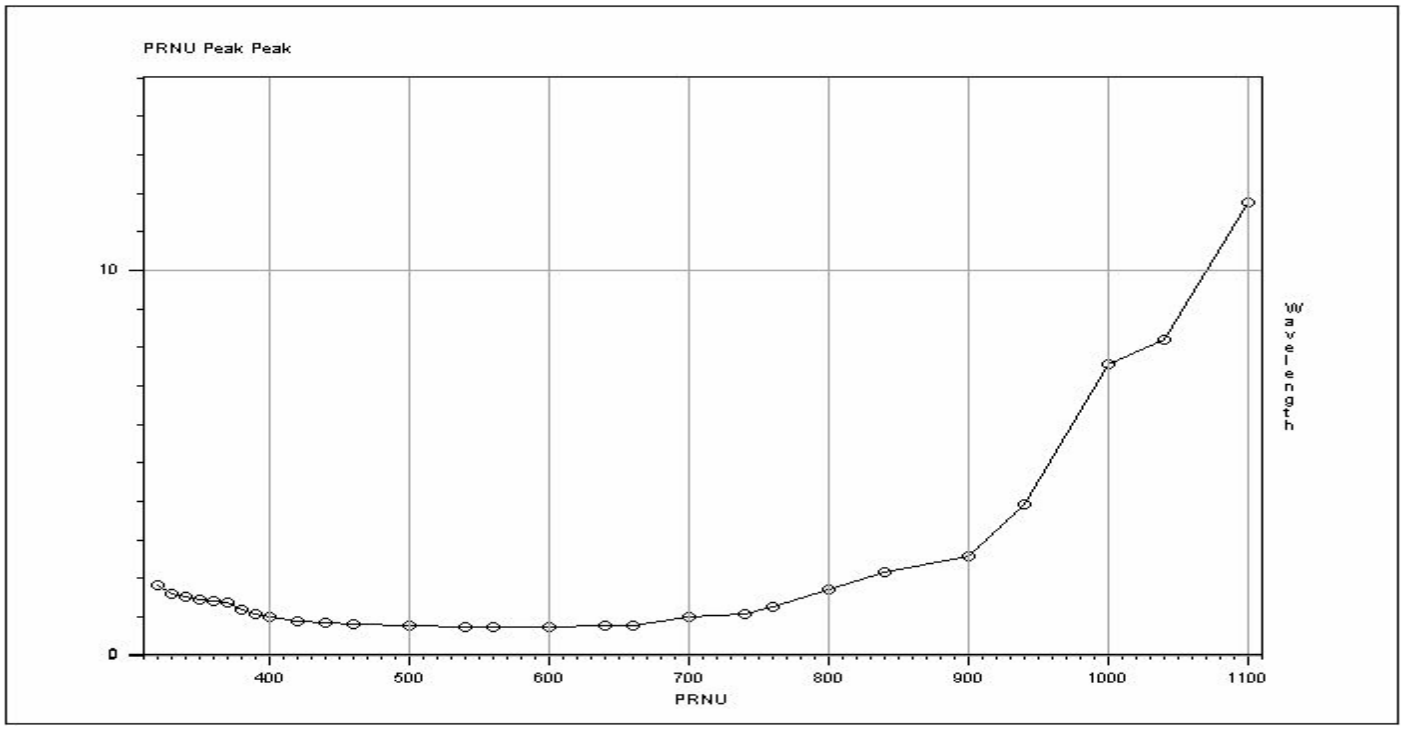


Figure 7.2-17, PRNU curve

The effective GIRAFFE bandwidth is 370 to 950 nm. This is limited by the Giraffe instrument optics transmission.

7.3 Opto-mechanical requirements for CCD's for GIRAFFE

The flatness tolerances are still based on a maximum allowable defocus blur of 10 μm with a target of 5 μm (note that the optics will deliver 80% of the energy within a circle of 15 - 20 μm)

	Requirements	**Measured results**
Item	detector (EEV 2K x 4K chip)	detector (Bruce)
Optical field size	Ø68 mm	Fulfilled
BFD [1]	$2^{+0.03}_{-0.03}$ mm	$1.98^{+0.01}_{-0.01}$ mm
De-centering [2]	< 0.5 mm	< 0.5 mm
P-V flatness	< 36 μm Goal : 18 μm [3]	X direction : 4 μm (64mm width) [4] Y direction : 5 μm (32mm width)

1. *The distance of the average CCD surface to the reference flange (mounting surface of field lens holder)*
2. *The distance between the optical center of the chip (not taking into account possible overscan pixels) and the mechanical axis of the dewar.*
3. *The distance of two planes, parallel to the reference flange, between which the sensitive surface of the chip or mosaic is contained. Applies to optical field size only.*
4. *Measured tilt along X and Y axis of the CCD.*

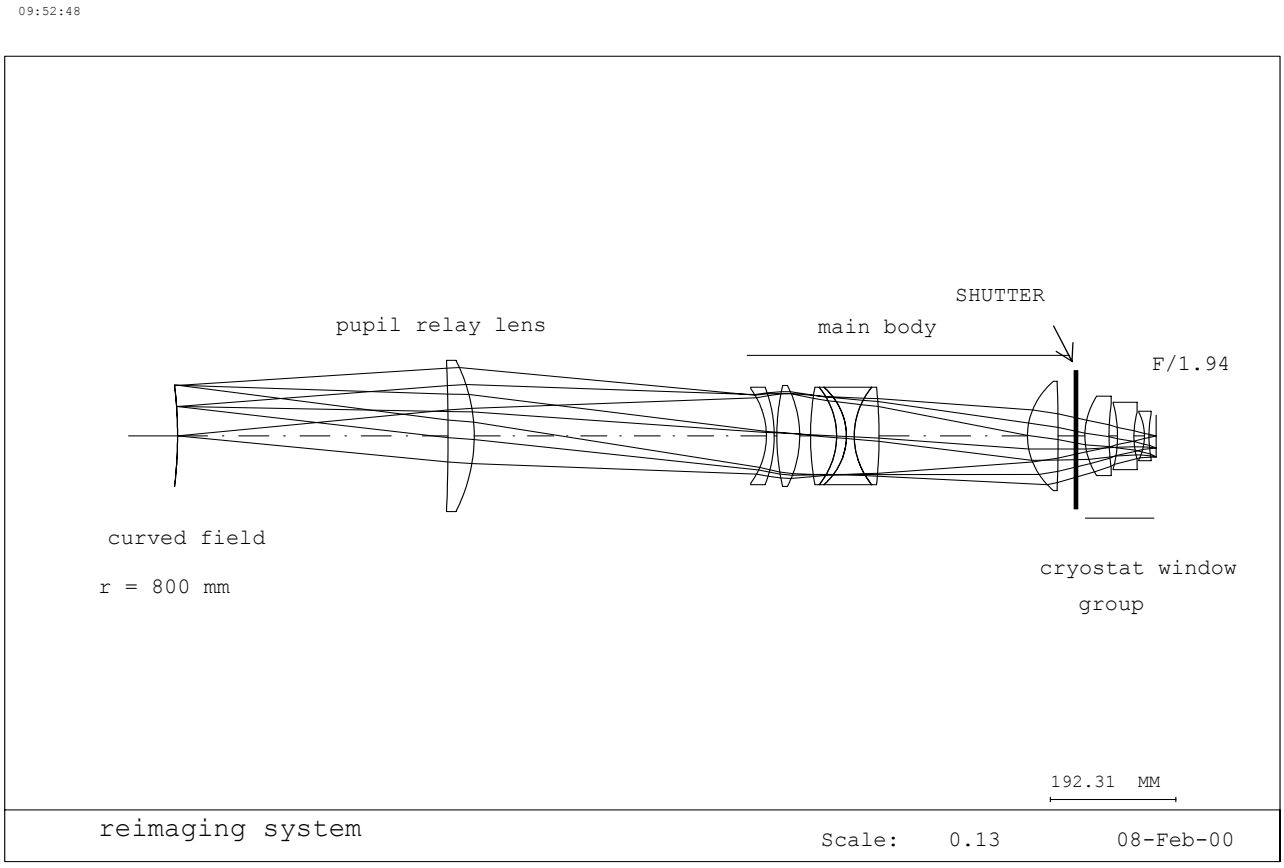


Figure 7.3-1, Optical path to the detector

8 Fiera housing, system design technical notes

These technical notes describe the basic design and performance of the FIERA Housing and Cooling system.

8.1 Fiera housing

The optical detector team has developed actively cooled housing for the controller and the power supply systems to meet the temperature specifications for the VLT.

8.2 Fiera cooling system

The FIERA active water-cooling system acts like a typical closed-loop liquid cooling system. In the system, cool water is supplied to the heat exchanger and (filtered) air is circulated between an electronic enclosure and a heat exchanger, which then transfers the heat to water flowing through the tubes. Our heat exchanger is placed inside the enclosure with cooled exit air blown directly through the FIERA boards and power supplies. This system permits closed-loop air-cooling and prevents entry of contaminated external on air.

System Design and size selection

Heat exchangers require some temperature difference between liquid and air entering the heat exchanger. In the VLT environment the incoming water temperature of the heat exchanger is regulated to be 8 degC below the ambient temperature. In order to dissipate the entire thermal energy produced, the thermal performance of the FIERA heat exchanger was specified as follows. To rate the thermal performance (TP) of our heat exchanger the following assumptions and equations were applied:

$$\mathrm{TP\,[Watts/^{\circ}C]} = \frac{Q}{T_{\text{air in}} - T_{\text{water in}}} = \frac{\text{thermal energy produced by the boards or power supplies}}{\text{air temperature into HX} \quad \text{- water temperature into HX}}$$

Figure 1 shows the FIERA heat exchanger mounted on the Rack unit. The heat exchanger is equipped with 4 slim-line low-noise fans to blow air through the complete area of the electronic boards. The fans are wired in parallel and operated with 24V DC voltages. The operating temperature range is from -10 degC to +70 degC. Additionally a temperature sensor (PT 100) is mounted on the rack on a cooling profile. This sensor monitors the air temperature inside the box and will give the reference value for the flow control unit.

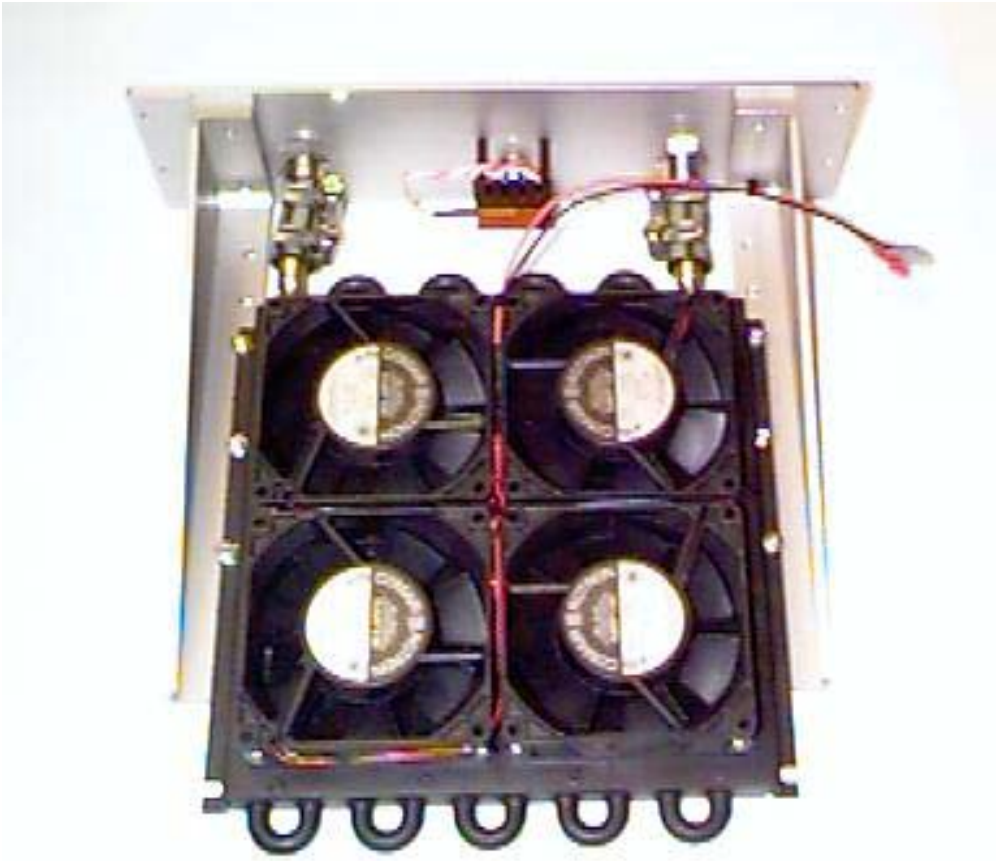


Figure 8.2-1, FIERA heat exchanger unit located at the bottom of detector head box and power supply

It will dissipate 200 Watts as a maximum value with a fully equipped FIERA detector head (11 slots) or power supply box. With an initial temperature difference of 8 degC the heat exchanger must have a minimum thermal performance of 200 watts / 8 degC = 25 Watts/degC. The result from the custom made heat exchanger is a little bit better and has TP of 27 Watts/degC. Thus 200 Watts /27Watts per degC = 7.4 degC. This means that the heat exchanger will dissipate 200 Watts and require 7.4 degrees C difference between the incoming water and incoming air. If the incoming water temperature is constant at 10 degC, the incoming air will stabilize at 17.4 degC.

9 System Maintenance

For any questions or maintenance problems, please send your input to ODT thru its generic email address odt@eso.org . Before any attempt to modify this system, please consult with the ODT.

9.1 Regular CCD performance checking

9.1.1 CCD Contamination

CCD contamination must be checked regularly by using the flat field screen and light at 450nm. The Giraffe instrument has all the embedded hardware to perform this kind of tests. The recorded flat field must be compared to a reference flat field by subtracting their bias and by dividing the two flat field. A 5x5 binning should be applied. The method employed is extensively described in the VLT-TRE-ESO-13121-2008 document. This should be done once a week.

9.1.2 Noise and conversion factor

By acquiring a set of biases and flat field, it is possible to measure regularly the noise and conversion factor. The same procedures that have been implemented for UVES shall be also used for Giraffe. It consists in acquiring images with BOB and to process them with MIDAS. This should be done once a week.

9.2 Electronic and detector head boxes

Maintenance of detector head and power supply boxes consist in checking once a year that the 4 fans described in figure 8.2-1 are still running and that the heat exchanger is not leaking.

9.3 SPARC Maintenance

The SPARC requires, that, after every VLT software update installed, the entire content of its hard disk is copied bit by bit to another disk. The latter will be regarded as a backup disk. The hard disk is a 9Gb SCSI hard disk, that is installed inside a case than can be easily pull out. The SPARC does not have any output display, or a video board. If one wants to get the SPARC state directly, because for instance the SPARC does not reply over the Paranal ATM network, a direct physical connection to the SPARC must be undertaken.

To be connected physically to the SPARC, the serial cable on TTYA can be tied to a PC running the Hyperterminal software under Windows (settings are 9800-N-8-1). All the debugging messages from the SPARC EEPROM/BIOS software are displayed. Access to Unix prompt using the "fcdrun" account can be also achieved by the TTYA cable. Moreover, for easier control, a crossed Ethernet RJ45 cable can be attached to the Ethernet board of the SPARC at IP=134.171.5.158, on the other side to the Ethernet board of the laptop PC. This allows a point to point connection, which supports Xterminals that can be run from a laptop using any emulator like Xwin32 or Linux. This permits to take the control of the SPARC locally without going thru the ATM LAN, only for maintenance and debugging purposes.

Be aware, that the hardware release of this SPARC is a temporary one (called as intermediate prototype), and, at some point, a final hardware release, including a PCI board, will update the current configuration.

9.4 Shutter

The SESO shutter is a fragile component and from time to time failures to close have been reported before COM1. Attention and future action might be planned to overcome these problems.

10 System pictures

This paragraph includes system pictures that have been recorded in the Garching integration hall.

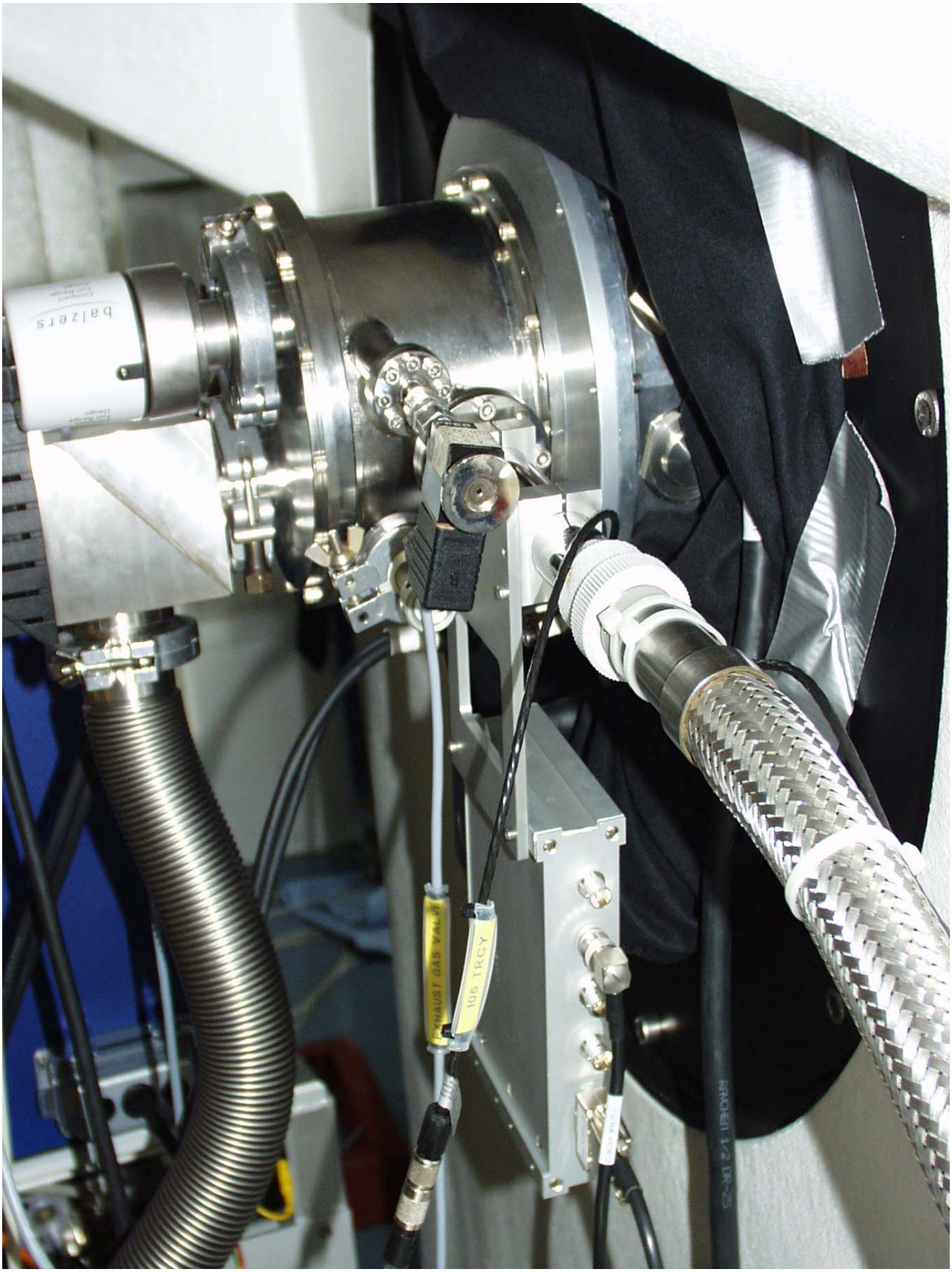


Figure 9.4-1, Preamp box and detector head

Figure 9.4-2, Power supply box, detector head box and PULPO+Shutter controller rack

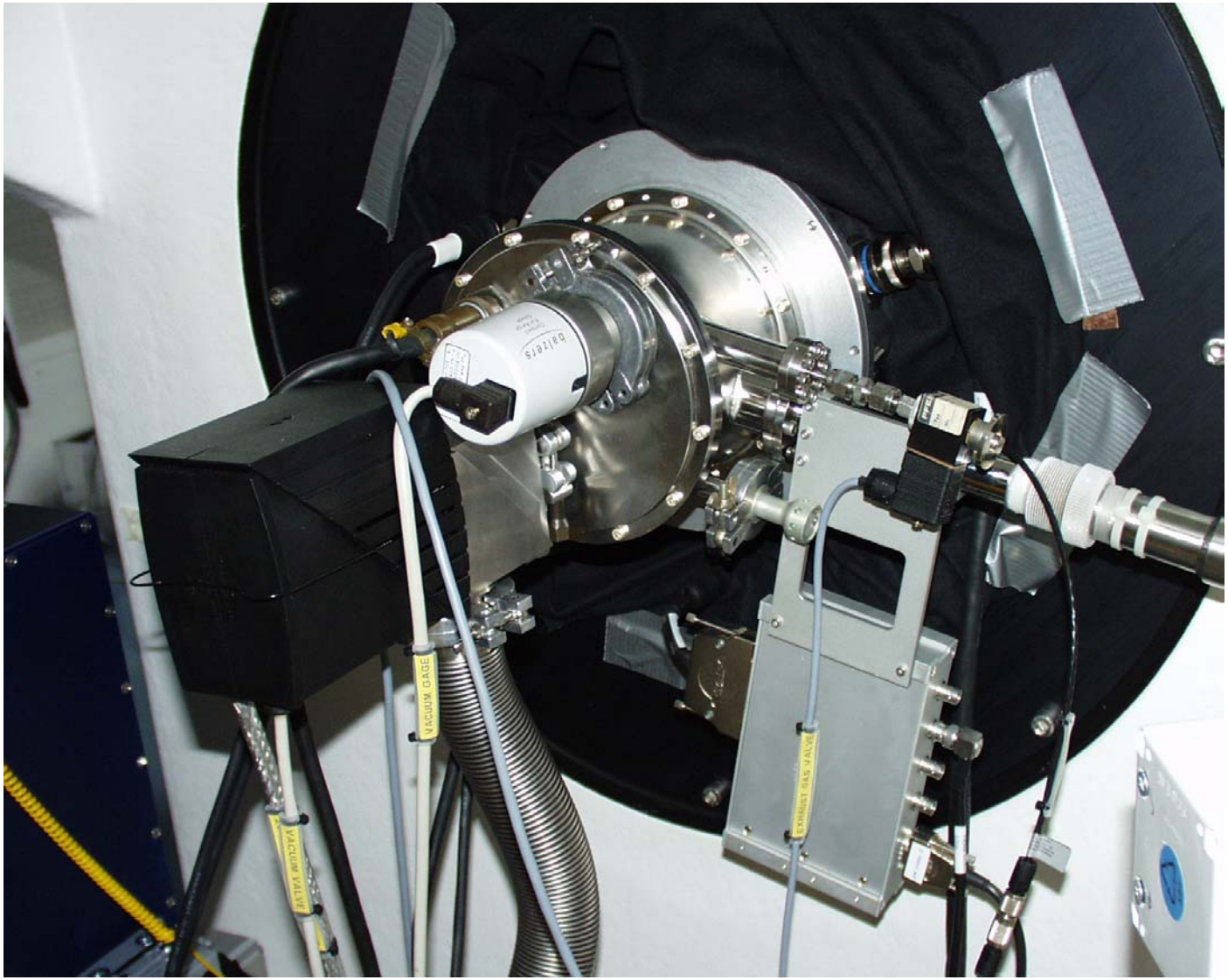


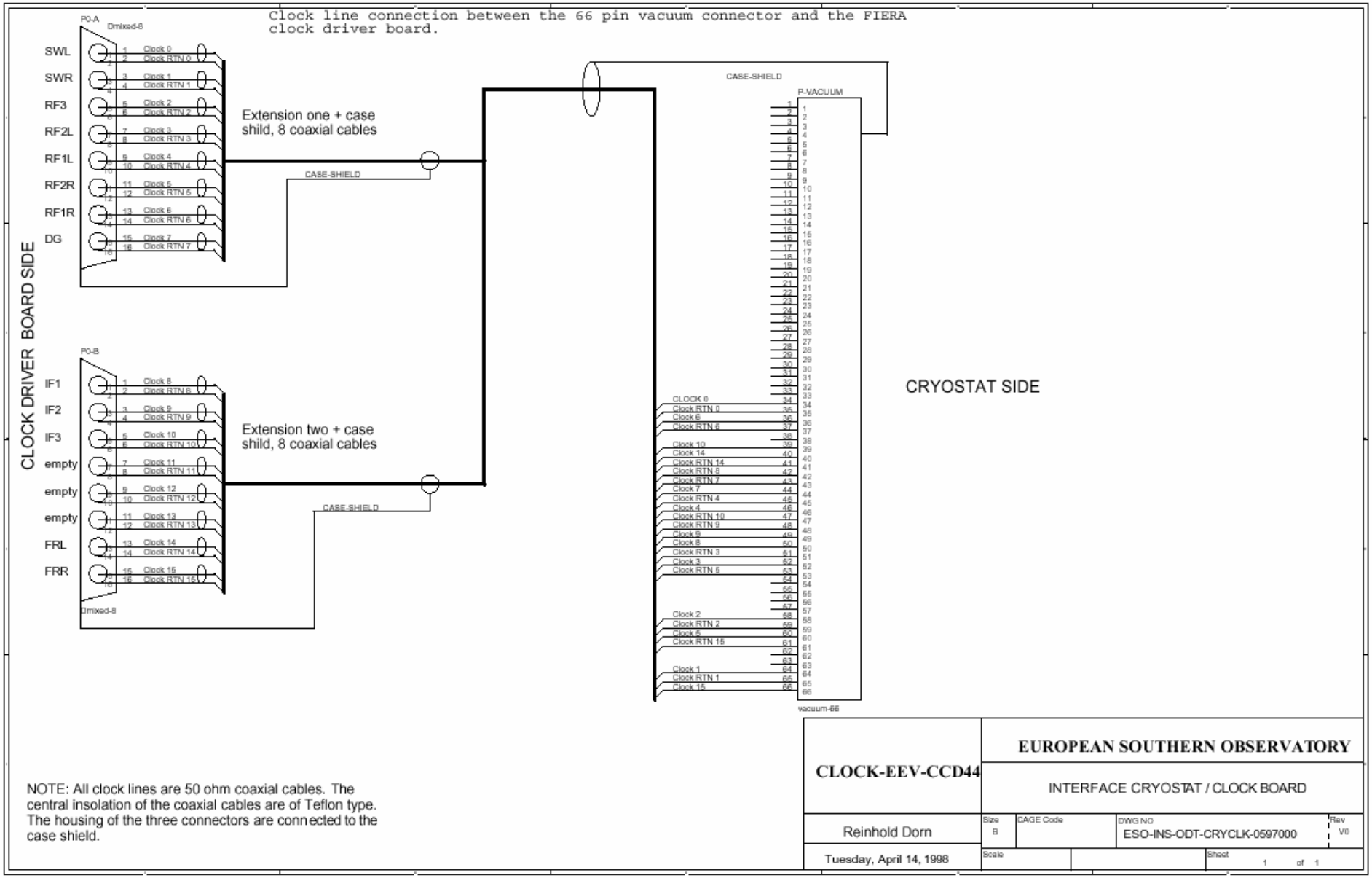
Figure 9.4-3, Detector head attached to the spectrograph, at Paranal, the input ln2 transfer line has been rotated by 180 degrees.

Figure 9.4-4, Detector head FIERA Box cable feed thru

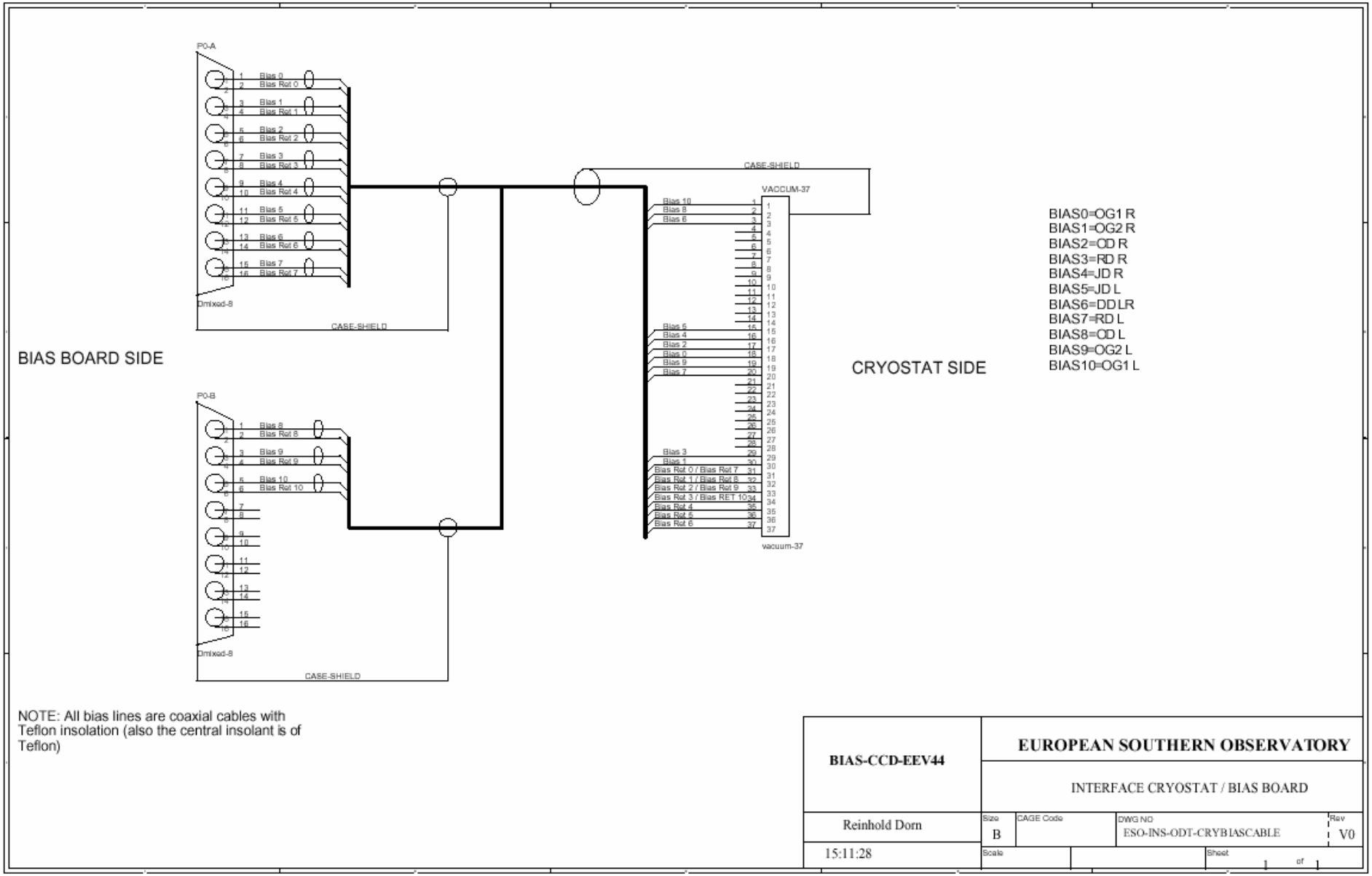
11 System cables

see drawings.

GIRAFFE CLOCK CABLE:



GIRAFFE BIAS CABLE:

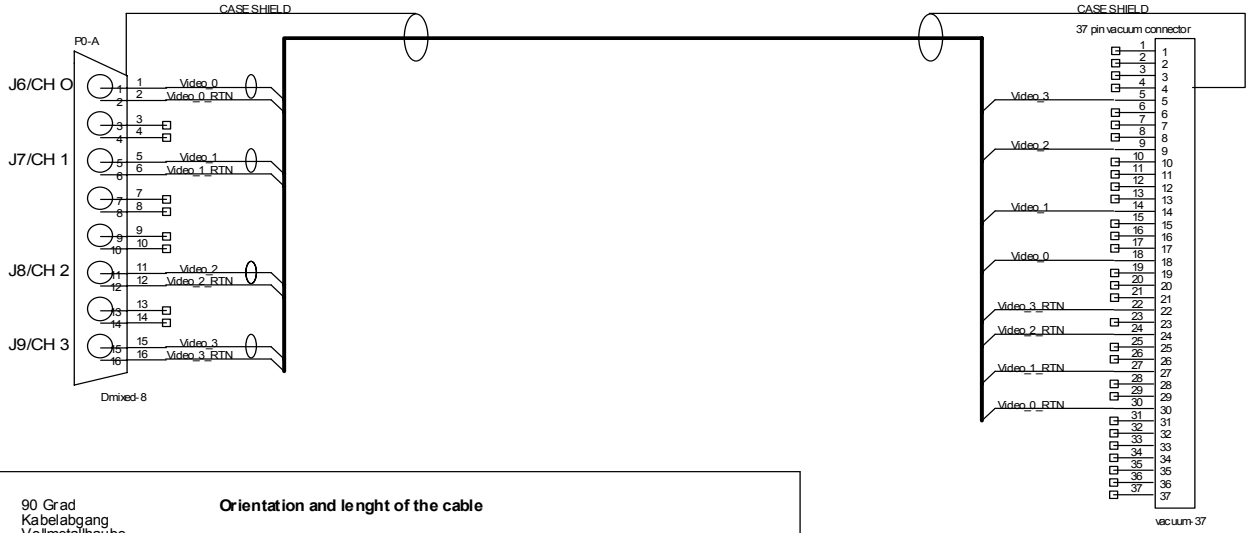


GIRAFFE CCD VIDEO CABLE

PREAMPLIFIER SIDE

Extension one + case shild, 8 coaxial cables

CRYOSTAT SIDE



This version of the cable take the upper row closer to the Cryostat. J6 to J9

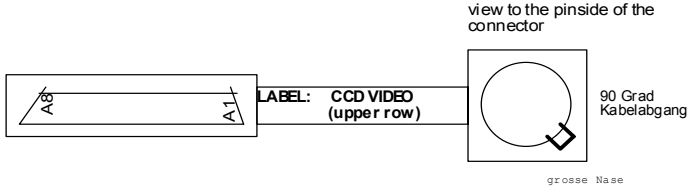
NOTE: The central wire of the coaxial cable should be connected to the video signal. The shield of the coaxial cable is to be connected to each video signals corresponding video return signal.

NOTE: Each video signal is fed to the preamplifier via a coaxial cable.Teflon insolated coaxial cables should be used, the central insolant should also be of Teflon.

90 Grad
Kabelabgang
Vollmetallhaube
FCT

Orientation and lenght of the cable

view to the pinside of the connector



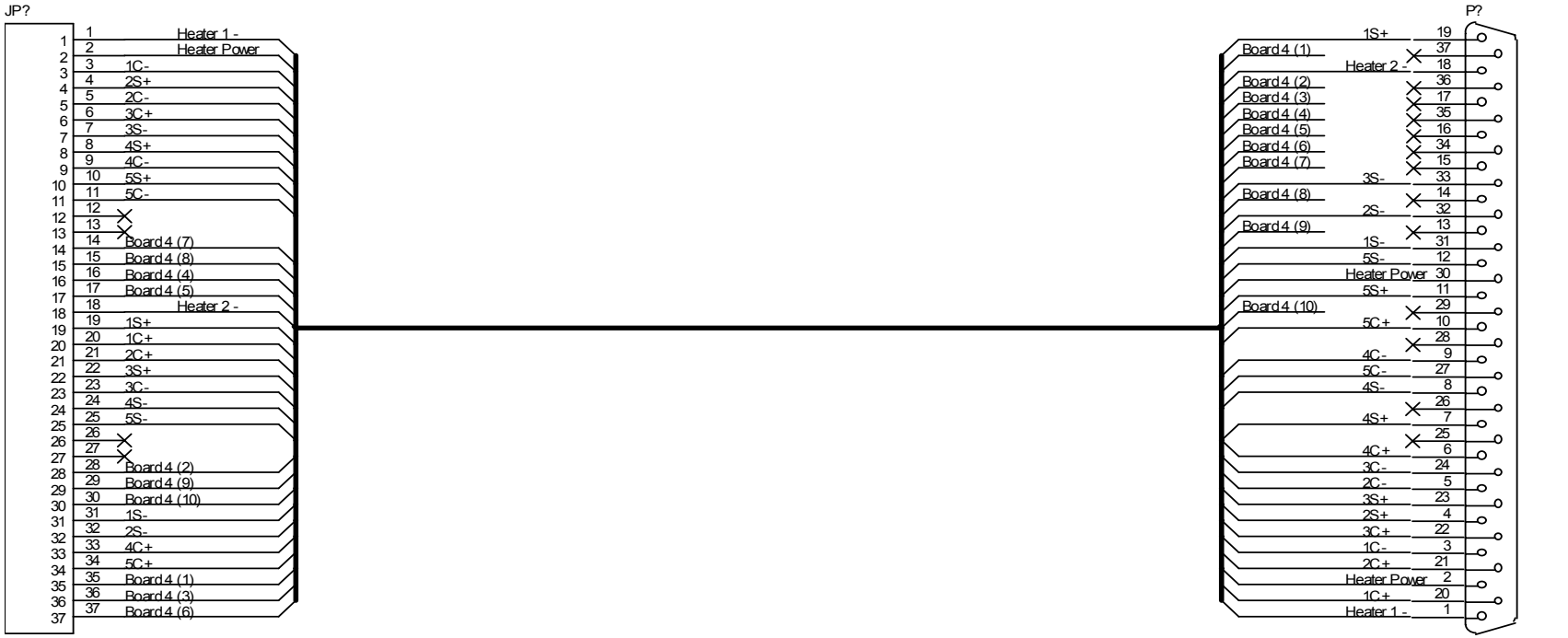
view to the pinside of the connector

The lenght of the cable between the two connectors is 4, 5 cm

D:\CCD_CABLES\VIDCAB_4LINES_UPPER.DSN
Monday, May 17, 1999

CCD VIDEO_upper_row	**EUROPEAN SOUTHERN OBSERVATORY**			
	INTERFACE CRYOSTAT / PREAMPLIFIER			
Reinhold Dorn	Size B	CAGE Code	DWG NO ESO-INS-ODT-CRYPAMP-	Rev V0
Monday, May 17, 1999	Scale		Sheet 1 of 1	

PULPO to cryostat CABLE



Do not populate pins 12,13,26,27
on vacuum connector

The wires for the connection of
Board4 (1-10) should be available at
the SUB-D connector,but NOT be
connected !!!

Title: Cryostat - Pulpo cable		
Size: A	Document Number: {Doc}	Rev: 1
Date: Friday, October 23, 1998	Sheet 1 of 1	

12 Acknowledgement

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This page is the last page of this document