DISCLAIMER

Custom CCD for adaptive optics applications

Mark Downing[a], Robin Arsenault[a], Dietrich Baade[a], Philippe Balard[e], Ray Bell[b], David Burt[b], Sandy Denney[b], Philippe Feautrier[c], Thierry Fusco[d], Jean-Luc Gach[e], José Javier Diaz Garcia[g], Christian Guillaume[f], Norbert Hubin[a], Paul Jorden[b], Markus Kasper[a], Manfred Meyer[a], Peter Pool[b], Javier Reyes[a], Michael Skegg[b], Eric Stadler[c], Wolfgang Suske[b], and Pat Wheeler[b].

[a]ESO, Karl-Schwarzschild-Strasse 2, 85748 Garching bei München, Germany;
[b]e2v technologies,106 Waterhouse Lane, Chelmsford, Essex, CM1 2QU, England;
[c]LAOG, Domaine Universitaire, 414 rue de la Piscine, BP 53 38041 Grenoble Cedex 9, France;
[d]ONERA, BP 72, 92322 Chatillon Cedex, France;
[e]LAM, Laboratoire d'Astrophysique de Marseille, 2 place Le Verrier, 13248 Marseille, France;
[f]OHP, Observatoire de Haute Provence, 04870 St.Michel l'Observatoire, France;
[g]IAC, Instituto de Astrofisica de Canarias, 38200 La Laguna, Islas Canarias, Spain.

ABSTRACT

ESO and JRA2 OPTICON have funded e2v technologies to develop a compact packaged Peltier cooled 24 µm square 240x240 pixels split frame transfer 8-output back-illuminated L3Vision CCD3, L3Vision CCD for Adaptive Optic Wave Front Sensor (AO WFS) applications. The device is designed to achieve sub-electron read noise at frame rates from 25 Hz to 1,500 Hz and dark current lower than 0.01 e-/pixel/frame. The development has many unique features. To obtain high frame rates, multi-output EMCCD gain registers and metal buttressing of row clock lines are used. The baseline device is built in standard silicon. In addition, a split wafer run has enabled two speculative variants to be built; deep depletion silicon devices to improve red response and devices with an electronic shutter to extend use to Rayleigh and Pulsed Laser Guide Star applications. These are all firsts for L3Vision CCDs. The designs of the CCD and Peltier package have passed their reviews and fabrication has begun. This paper will describe the progress to date, the requirements and the design of the CCD and compact Peltier package, technology trade-offs, schedule and proposed test plan. High readout speed, low noise and compactness (requirement to fit in confined spaces) provide special challenges to ESO's AO variant of its NGC, New General detector Controller to drive this CCD. This paper will describe progress made on the design of the controller to meet these special needs.

Keywords: Adaptive optics, AO systems, Electron Multiplying CCD, EMCCD, L3Vision CCD, readout noise, wavefront sensor.

1. INTRODUCTION

The success of the next generation of instruments (e.g. VLT SPHERE, MUSE, HAWK-I) for 8 to 10-m class telescopes will depend on the ability of Adaptive Optics (AO) systems to provide excellent image quality and stability. This will be achieved by increasing the sampling and correction of the wave front error in both spatial and time domains. For example, future Shack Hartmann systems will require 40x40 sub-apertures at sampling rates of 1-1.5 kHz as opposed to 14x14 sub-apertures at 500 Hz of current systems. Detectors of 240x240 pixels will be required to provide the spatial dynamics of 5-6 pixels per sub-aperture. Higher temporal-spatial sampling implies fewer photons per pixel therefore the

need for much lower read noise (<<1e-) and negligible dark current (<< 1e-/pixel/frame) to detect and centroid on a small number of photons. Existing detectors do not have this combination of image area size, read out speed, and low noise performance. As the WFS detector has been identified as the critical component of future AO systems there is an urgency to develop better detectors.

Numerous European astronomy institutions, including ESO, have teamed up in the OPTICON network[1], and obtained funds in the joint research activity JRA2[2], "Fast Detectors for Adaptive Optics", from the European Commission to support the massive R&D effort to develop a new detector. After extensive market research culminating in a Call For Tender, e2v was chosen to develop a custom-designed detector based on an extension of their L3Vision[4] EMCCD technology. Analysis[2,6] showed that the sub-electron read noise of L3Vision CCDs clearly outperformed classical CCDs even though L3Vision devices exhibits the excess noise factor of √2 typical of EMCCDs. The reason for this conclusion is clearly shown in the results (Fig. 1) of an analysis performed by Thierry Fusco[6] for the ESO instrument SPHERE for two different types of guide stars (GS), white-yellow and red, where a much higher Strehl Ratio is achieved for a faint guide star by an EMCCD than a classical CCD even though it was assumed that the classical CCD had a much higher quantum efficiency in the red.

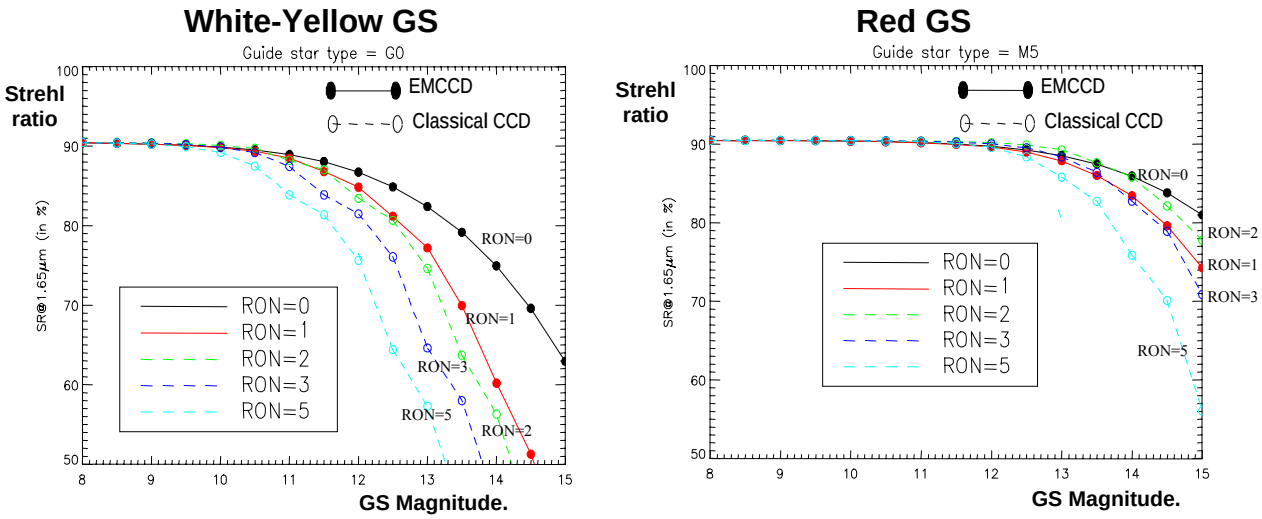

Fig. 1. Results of analysis performed by Thierry Fusco for ESO instrument SPHERE that compares an EMCCD of read out noise (RON) 0 and 1e- to a classical CCD of read noise 2, 3, and 5e- for two different types of guide stars. Left: Plots of Strehl Ratio versus GS magnitude for white-yellow guide star. Right: Plots of Strehl Ratio versus GS magnitude for red guide star.

2. REQUIREMENTS

The OPTICON JRA2 science working group set the top level requirements after carefully considering the needs of AO systems for future instruments and their science programs. The following detailed requirements were established:

1. big pixels, square 24 µm (goal), to ease the optical system design, but not too large to produce excessive dark current (DC) or CTE problems.
2. versatility of a 100% fill factor and 240x240 square grid array of pixels that can be used by any WFS system: SH, curvature, or pyramid, with or without gaps (guard bands) between sub-apertures.

3. format size of 240 pixels being a number that is divisible by the number of output nodes, 8, and binning factors and aperture sizes of 1, 2, 3, 5, 6 and meets the minimum pixel requirement of 40 sub-apertures x 6 pixels/subaperture.
4. low read noise of < 1 e-/pixel and goal of 0.1 e-/pixel.
5. range of operating frame rates from 25 frames/s (fps) for use when photon starved with faint Natural Guide Star (NGS) to highest sampling rate of 1,200 fps for use with bright NGS and Laser Guide Star (LGS).
6. easy to use; eight output nodes each operating at maximum pixel rate of 15 Mpixel/s, that provide a good compromise between the number of connections from the detector to the outside world and operational practicalities such as power dissipation, pixel rates, and clocking rates.
7. low image smearing (<5%) when transferring from the image to store area; an undesirable effect that can be corrected for by software.
8. cosmetically defect-free as every defect will either complicate the centroiding or make it impossible to centroid a sub-aperture.
9. good spatial characteristics, PSF < 0.9 pixel FWHM over 460 to 950 nm, to accurately determine where the photons are detected.
10. very low Dark Current (DC) of < 0.01 e-/pixel/frame at 1,200 fps and < 0.04 e-/pixel/frame at 25 fps to minimize the large errors introduced by the quantum nature of DC, as the electron is the smallest unit. A single electron of DC creates a large error when centroiding on a small number or single photon event. DC includes contributions from the clock induced charge (fixed amount per frame readout), the image area during exposure ($\propto$ exposure time), the store section and the serial register during readout ($\propto$ frame read out time).
11. Peltier cooled package for compact size, maintenance free, and minimal support equipment so that the final assembled camera system can fit in the small volumes usually reserved for AO systems.
12. detection signal limit of 5 ke-. In normal operation, the system will be photon starved as there are not too many bright NGS and LGS will be operated at as low a power as possible. Well depth and output amplifier dynamic range can be traded to improve other parameters such as higher gain of output amplifier and lower clock amplitudes to transfer charge.
13. linearity of < 2%. Analysis shows that this level of non-linearity does not introduce any significant errors. Non-linearity can be corrected by a look-up table.

3. DESIGN

The design (Fig. 2) is a 24 μm square 240x240 pixels split frame transfer 8-output back illuminated L3Vision CCD, designated as the CCD220. The shuttered variant is designated as the CCD219.

The image and store area are built with metal-buttressed parallel clock structures to enable line shifts of 10 Mlines/s for total transfer time from image to store of 12 μs and low smearing of under 1.5% at 1,200 fps. Two phase clocking was chosen for simplicity, lower power dissipation, and symmetry of drive. See Gach et al[5] for a discussion of the benefits to the CCD controller of having a symmetric drive.

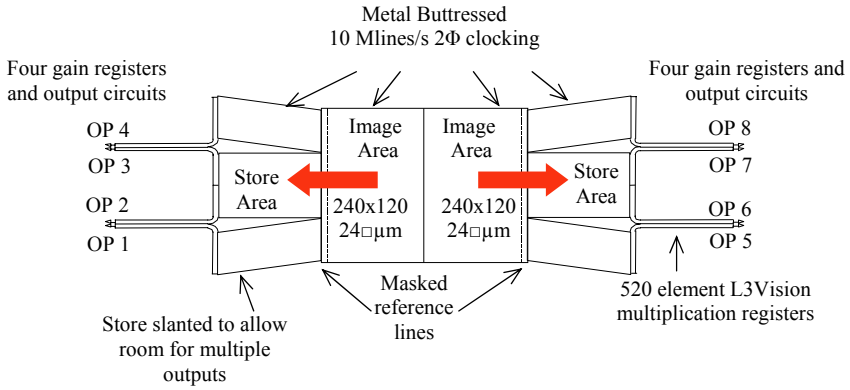

Fig. 2. Schematic of CCD220.

The store area is slanted out to make room for the standard serial registers (three phase clocking) to curve around (Fig. 3) and provide space for the output circuitry. Each output will have a 520 element 16 µm standard L3Vision gain register whose gain is controlled by the voltage of the multiplication phase. The output amplifier will be a 2-stage source follower (

Fig. 4 for specifications) and of similar design to that employed on recent L3V CCDs (CCD97[12]). The gain register will be optimized for a gain of 500-600, a value typically expected for AO applications. With an expected output amplifier read out noise (RON) of 50e, this will provide an overall effective read noise of under 0.1 e- (50 e- RON/500 of gain register). The serial registers, gain registers, and output amplifiers are designed to operate up to 15 Mpixel/s to achieve a full goal frame rate of over 1,500 fps.

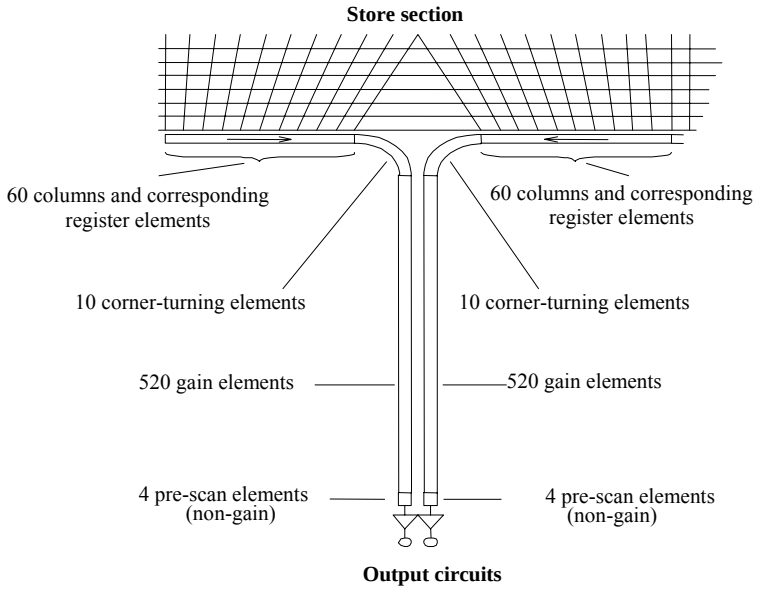

Fig. 3. Details of serial and gain register.

The baseline device will be built in standard silicon and is low risk with guaranteed delivery of devices that meet minimum requirements. This meets the risk profile of both JRA2, who must produce a design report to the EU by 2008, and ESO, who require working detectors for their next generation of instruments. A split wafer run will enable two speculative variants to be built. The first is to build devices in 40 µm deep depletion silicon (1500 Ohm.cm) which will

offer much better red response (Fig. 5). High red response is important for applications that rely on natural GS such as VLT SPHERE. The second is to build devices with an electronic shutter to extend the use of the detector to applications such as Rayleigh and pulsed Laser Guide Stars (LGS) which require very short shutter times of 2-3 μs. These short shutter times are not possible by mechanical means. Pulsed LGS systems offer the advantage to freeze the laser pulse to a small spot in the sodium layer and thus overcome the problem of spot elongation.

Feature	**CCD220**
Overall responsivity	1.0 μV/electron
Node capacitance	100 fF
RON (rms with CDS ~ 15 MHz)	50 electrons
Reset rms noise (dominates without CDS)	125 electrons
Saturation (3V swing at node)	1.9 M electrons
Output impedance	350 Ohms
Maximum frequency (settling to 1%, load ≤ 10pf)	15 MHz
Maximum frequency (settling to 5%, load ≤ 10pf)	25 MHz
Power dissipation	50 mW

Fig. 4: Nominal specifications of the output amplifier.

No dump gate was included in the design as it was doubtful whether its response time to dump charge would be any faster than simply clocking the serial register, and if included would add excessive capacitance to neighbouring registers and add pins to the package resulting in a larger package size and more heat load. Additionally, for deep depletion devices a much wider dump gate would be required to avoid parasitic effects resulting in an even slower dump time. To reduce pin count further, summing wells were not included as it was thought to be acceptable that with low read noise of 0.1e- binning in the serial direction could just as easily be performed off chip.

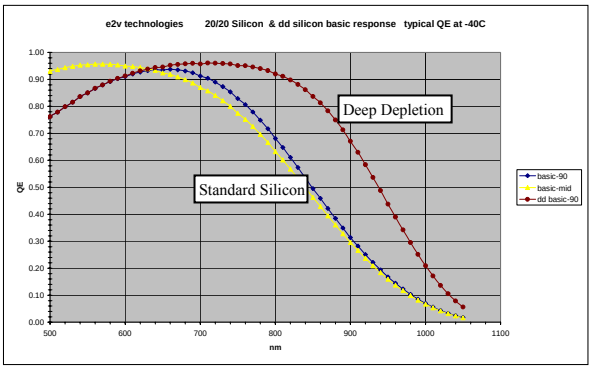

Fig. 5. Comparison of QE for a standard silicon device (basic-90/basic-mid) to that of a deep depletion device (dd basic-90). These curves are only typical and the curves of the final devices may differ.

4. CCD219 SHUTTER DESIGN

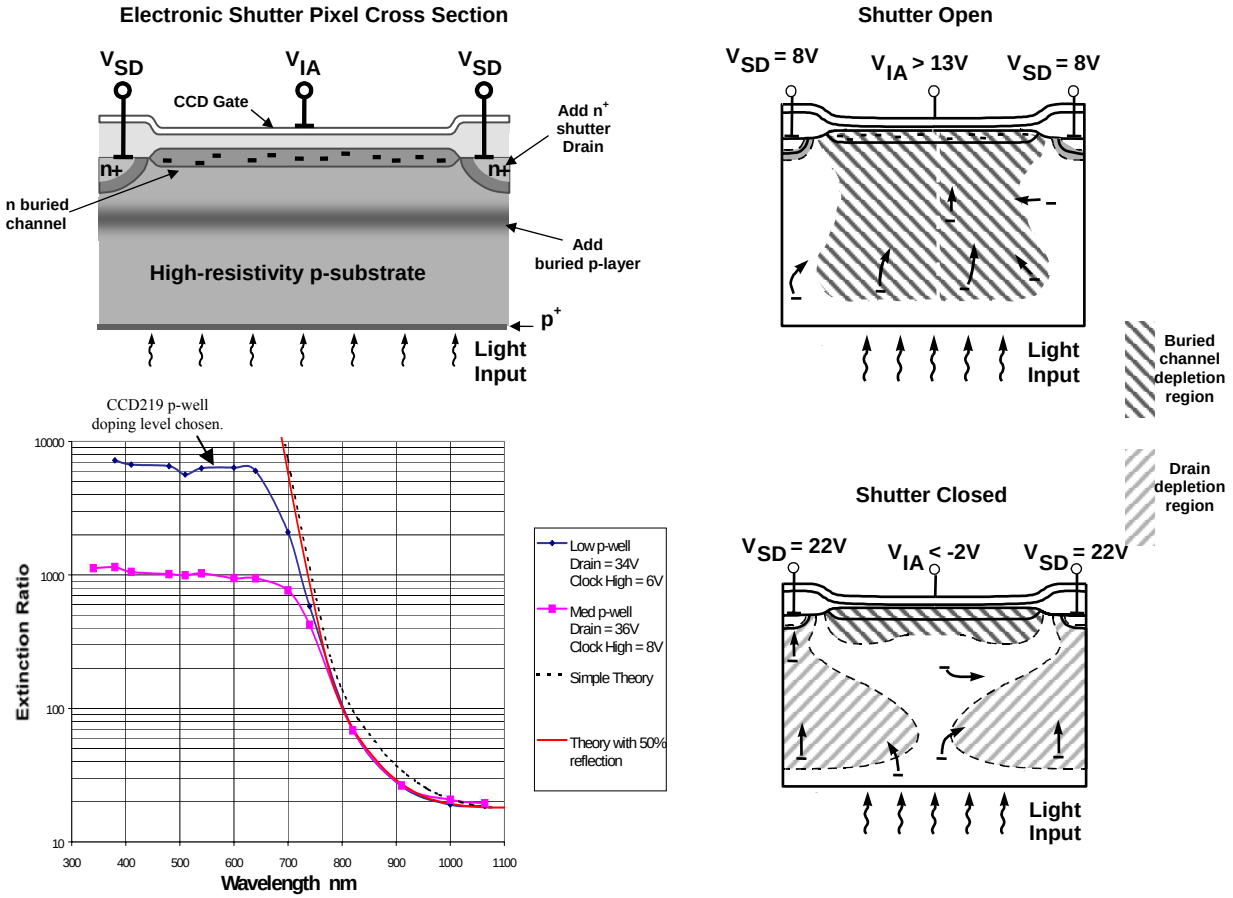

Fig. 6. Principle of the Integral Shutter of CCD219 (see text for explanation). Top left: Cross-section of pixel showing added p-layer implant and n^+ doping to form the shutter drain. Top right: Clock voltages for shutter open. Bottom right: Clock voltages for shutter closed. Bottom left: Expected extinction ratio versus wavelength.

The principle of the integral shutter is shown in

Fig. 6. The device is manufactured in high resistivity silicon (top left

Fig. 6) to which a more heavily doped p-layer (a boron implant followed by a long high-temperature drive-in) is added below the n-type buried channel. An n+ doping is added in the channel stop region to form the shutter drain, SD, to which is overlaid a biased gate, SG, for field-relief purposes (not shown in

Fig. 6). If the shutter drain voltage, V_{SD} is taken "low" (~ 8V) and the image area clock voltage, V_{IA}, is taken to a sufficiently "high" level (~13V), then the depletion region from the pixel punches through the p-layer implant and charge generated in the underlying substrate is collected. If the image area clock voltage, V_{IA}, is taken to a somewhat lower level (~ -2V) and V_{SD} is taken "high" (~22V), then only the drain depletion region punches through the p-layer and collects charge generated in the underlying substrate. These two states are effectively shutter "open" (top right

Fig. 6) and "closed" (bottom right

Fig. 6), respectively. The voltage on the shutter gate is not critical, other than it helps avoiding the drain breakdown voltage being too low for the shutter-closed condition. The CCD219 is essentially the same as the CCD220 but with the

incorporation of the shutter gate and drain structures. The individual column drains join to a bus that runs across the centre of the image section (i.e. between the two halves).

The manufacturing processing (namely the doping level of the p-layer implant) was chosen to obtain the best compromise between the extinction ratio (ratio of collected signal between shutter "open" and "close" states) and PSF. The expected extinction ratio for the chosen doping level of the p-layer is shown in the bottom left graph of

Fig. 6. The shutter switching time is dependent on the RC time constant of the shutter drain which is estimated to be ~ 1μs (C ~ 2 nF and series R~500 ohms). Shutter switching times of a few μs are expected.

5. PSF

Fusco et al[10] have shown that for upcoming AO instruments (e.g. VLT SPHERE, MUSE, HAWK-I) good spatial characteristics of PSF < 0.9 pixel FWHM over 460 to 950 nm is required for a 24 μm square pixel detector. Model predictions of the performance of the CCD220 by e2v and measurements carried out by Fusco et al[10] on a similar L3Vision device (CCD60) show that the baseline standard silicon CCD220 should meet this requirement under favourable operating conditions. On the other hand the speculative variants, the deep depletion CCD220 and the CCD219 shuttered device, will have worse PSF due to the extra thickness (40 μm versus 13 μm) of the devices and the inclusion of the necessary buried p-layer. The extra thickness of the device will result in a greater undepleted region at the back of the CCD where charge must laterally diffuse. The buried p-layer implant acts as a barrier to the electric fields of the image area clocks thus reducing their penetration depths and increasing the width of the undepleted region at the back of the CCD. The buried p-layer is necessary for the correct operation of the L3Vision gain register built on high resistivity silicon and in the case of the CCD219 one of the processes essential to the operation of the shutter (see discussion of CCD219 in previous section).

The p-layer implant of the deep depletion and shuttered devices were dosed differently to individually optimise their performance. e2v had experience of using four different dose levels, the higher three of which had been used on a previous integral shutter development[8]. To obtain a better PSF, the lowest dose level was chosen for the deep depleted CCD220. A slightly higher dose level was chosen for the CCD219 shuttered device to ensure that the image clock high level during shutter closed operation does not "punch through" the p-layer implant, but is still high enough to transfer charge.

PSF modelling was performed in two steps. First, simulations determined the median depletion depth for a given p-layer implant level. The results being adjusted for the two-dimensional geometry of the pixel, i.e. the depletion is different under the channel stops compared to the 2-phase clock regions. The same model has been used by e2v previously to calculate the depletion depths of the CCD55-20 for the ESTEC program[8]. The results for this program were in good agreement with the clock voltages required and the depletion depths inferred by the measurements. In the second step, the PSF was estimated from this simulated depletion depth by the following two methods:

Approximation Method (Holland et al[7]): The PSF for signal generated near the back surface can be approximated to the undepleted silicon thickness, such that $\sigma ff = Lff$, where σff is the rms standard deviation of the PSF of the undepleted or field-free region and Lff is the field-free thickness. For the two curves in

1. Fig. 7, it is assumed that the silicon has been back-thinned to 40μm and that 2 σff is equivalent to the FWHM of the PSF distribution.

e2v Model: The depletion depths were fed into the e2v model for PSF. This model has not been verified with measurement for high resistivity material so it is interesting to see how closely its predictions match those of the approximation method. The kink in the curves of

2. Fig. 7 indicate the clock voltages at which the depletion begins to extend beyond the p-layer implant, sometimes referred to as "punch-through".

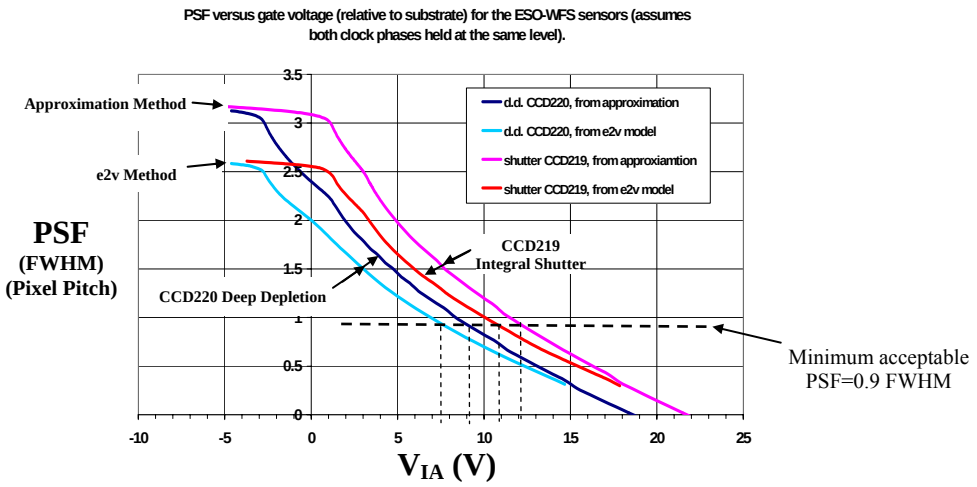

Fig. 7. Simulation of PSF versus image area clock voltage, V_{IA}, relative to the substrate for the CCD220 deep depleted and CCD219 shuttered devices at worse case wavelength of 460 nm. PSF was predicted by two methods; approximation to the undepleted thickness and e2v model. The dashed line shows the minimum acceptable PSF of 0.9 pixels.

Note that the modelling has the following approximations and uncertainties. Predicting the depth of depletion is made difficult by the fact that the doping concentration tends to vary between wafers and with depth. The basic simulations assume an ideal doping profile based on the nominal 1500 Ohm-cm resistivity. Out-diffusion during processing also affects the location of the epitaxial silicon-substrate boundary, thereby complicating control of the final silicon thickness. In addition, the defined epitaxial thickness is subject to a ±10% tolerance. The lowest p-layer dose for the CCD220 is approximately five-sixths of that modelled for the CCD219 dose. The difference in required voltages seen in the graph indicates just how much difference any variation in p-layer dose will make. At longer wavelengths, a proportion of the light will be reflected from the front surface and much of this may be scattered by the electrode structure. It is not known whether this scattering will be affected by the metal buttressed gates. The specular reflection and the scattered component are not accounted for in the PSF models.

The results of the estimation are given in

Fig. 7. To obtain a PSF of 0.9 pixel FWHM, the CCD220 deep depletion device will require an image area clock voltage with respect to substrate of VIA > 10V. The shuttered device will need a VIA > 13V. To operate at these voltages will require the image area to be operated non-inverted during the time charge is collected and this may result in two orders of magnitude higher dark current (see discussion of dark current in the next section). Note that once running non-inverted, the dark signal does not degrade further by using high clock levels such as 10V and 13V.

High clock levels of 10V and 13V will cause degradation in the full well capacity of the image area as charge will start to interact with the surface at a much lower level. However, as the application only requires a well capacity of 5000e, this is not anticipated to be a problem.

6. DARK CURRENT AND CLOCK-INDUCED-CHARGE

The baseline standard silicon CCD220 will be operated in inverted mode. At an operating temperature of -45 °C which has been predicted by thermal modelling, the standard silicon device is predicted to surpass the minimum and almost meet the goal requirements of dark current. See section 8 for further details of thermal and dark current modelling.

The discussions of the previous section have shown that to achieve the required PSF it will be necessary for the deep depletion CCD220 and the CCD219 shuttered device to be operated during integration of charge with the image area

clocks at very high levels (+10V and +13V respectively) and hence out of pinning (note that surface inversion occurs at V_{IA} ~ -9V). This non-inverted mode would normally lead to a dark current increase of approximately two orders of magnitude higher than the inverted mode level due to the lack of suppression of the surface dark current. However, it may be possible to still achieve inversion dark current levels if the clocks are taken "low" to achieve pinning at least once per frame period. At the low temperature of operation and fast integration times of the CCD220, the trap-release time constants are long enough such that the holes will not have time to travel away from the surface through the column channel stops to substrate before the frame transfer pulses commence again. The dark current therefore stays at the pinned value, a technique known as "intrinsic dither mode". To demonstrate this "intrinsic dither mode", measurements were performed at e2v on a CCD47-20. The results (

Fig. 8) show that with "intrinsic dithering" the dark signal level approaches the inverted mode of operation as the temperature falls and the dithering rate increases. These results are in good agreement with Burke and Gajar[11] who have extensively analysed this phenomenon.

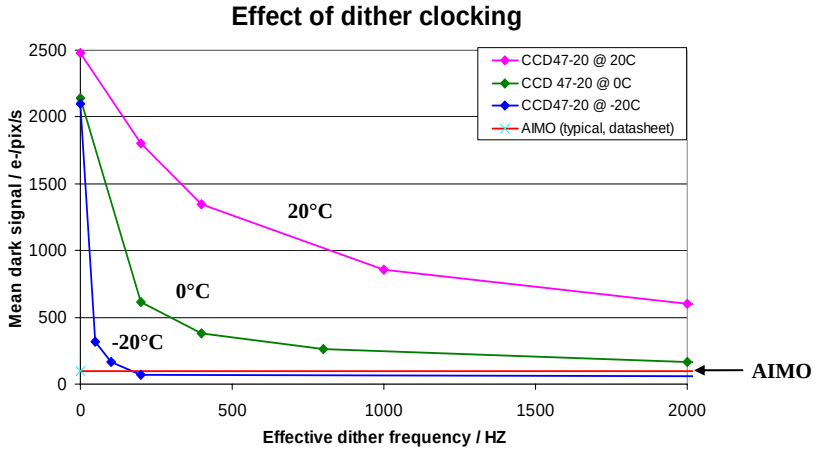

Fig. 8. Results of measurement performed at e2v on a CCD47-20 at various temperatures to demonstrate "intrinsic dither mode". The curves have been scaled differently for convenient plotting. The main item to note is that at the lowest temperature (-20°C) the dark current reduces at high readout rates. This process is expected to apply to the CCD220 at operating temperature of -40°C.

Clock-induced charge (CIC) is generated during frame transfer and increases with increasing clock amplitude. It is a consequence of holes released from surface traps and being subjected to impact-ionisation as they travel through the high fields between electrodes. It is clear that having clock low 9V below substrate to pin the surface but clock high at +15V to increase the depth of depletion will give rise to very large levels of CIC. However, using three clock levels as necessary for the CCD219 shuttered device will aid the compromise between CIC and PSF. If the same clock "high" and "low" levels as used for the baseline sensors are employed for frame transfer, the deep depleted CCD220 CIC should be the same. This clock amplitude should be chosen to be just adequate to transfer charge over the 2-phase barrier. The "extra high" image area level should only be used during integration in order to improve PSF, and will not therefore give extra CIC.

Fig. 9 provides an example of this clocking scheme.

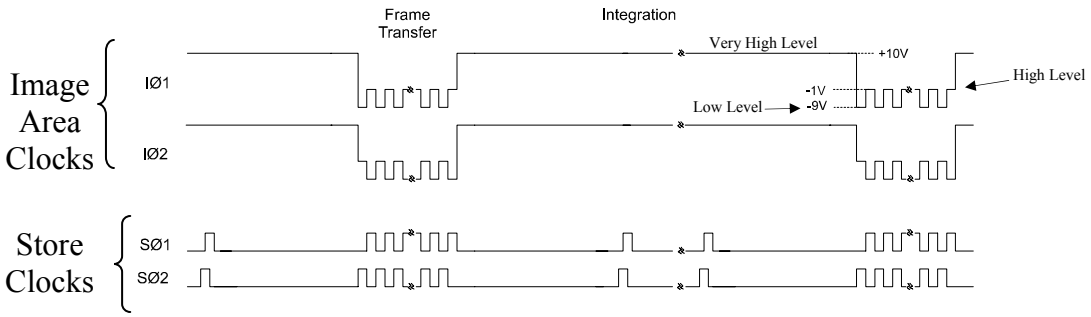

Fig. 9. Example clocking scheme for the deep depleted CCD220 using tri-state image area clocks. This mode should minimize the dark signal and CIC while maximizing the PSF performance.

7. POWER DISSIPATION

The power dissipated, W_{total}, in clocking the capacitive load of a CCD clock line may be estimated by,

$$W_{total} = CV^2 f$$

where C is the clock capacitance in Farad per phase, V is the clock amplitude in volts and f is the mean clock frequency in Hz. The mean clock frequency is the number of clock pulses per second and takes into account periods of clocking inactivity. The power dissipated on-chip , $W_{on\text{-}chip}$, is given by:

$$W_{on-chip} \approx W_{total} \Big/ \sqrt{\left(1 + \left(\Delta t / 2\tau\right)^2\right)}$$

where the rise and fall times of the clock edges (assumed to be trapezoidal in shape) are each Δt and τ is the RC time constant of the clock line. If $\Delta t \leq 2\tau$, then almost all of the power is dissipated on-chip. For much slower edges, the fraction is approximately $2\tau/\Delta t$. In all cases, the off-chip fraction, ($W_{total} - W_{on\text{-}chip}$), is dissipated in the output impedance of the buffer and any external series resistance. In the case of a sinusoidal drive, as is suggested for the high voltage clock of the multiplication register, the on-chip power is $\pi^2 \tau f W_{total}/2$. If this sinusoidal drive is generated by a resonant drive, it has been found that the power actually dissipated in the external circuitry can be reduced by a factor of about 4 (i.e. to ~ $W_{total}/4$).

Section	ΔV	***Load C***	τ **(ns)**	Δt **(ns)**	**Mean** ***f***	W_{total}	$W_{on\text{-}chip}$
Image	10 V	3.48 nF	~2	20	183 kHz	64 mW	13 mW
Store	10 V	3.16 nF	~2	20	366 kHz	116 mW	23 mW
Serial Register	10 V	552 pF	~1.2	5	13.2 MHz	730 mW	316 mW
Multiplication High Voltage	45 V	220 pF	~0.3	Sine	13.6 MHz	6.1 W	122 mW
Amplifiers	-	-	-	-	-		400 mW (8 x 50 mW)
Total	-	-	-	-	-	-	**874 mW**

Fig. 10. Estimated total and on-chip power dissipation of CCD220 at 1,500 fps.

The table in Fig. 10 provides a section-by-section worst-case estimate of the on-chip power dissipation for the CCD220 operated at a frame rate of 1,500 fps. Note that nearly 50% of the on-chip power is dissipated in the output amplifiers. The image and store sections contribute only 5% of the total on-chip power dissipation.

8. PACKAGE

The CCDs will be encapsulated in a 64 pin package with a custom-designed integral thermo-electric cooler similar to that shown in

Fig. 11. The Peltier cooler, ceramic chip carrier and CCD will be glued by a thermally conductive epoxy adhesive (50 µm of ABLEBOND). The package will be sealed and back-filled with 0.9 bar of Krypton gas to minimize heat transfer to the outside.

The CCD220 die will have four fiducial crosses in the region of the bond pads, two on either side of the device image area, in the region of the bond pads. These will be clearly visible through the package window for alignment purposes such as when attaching lenslet arrays. An AD590 temperature sensor will be glued to the ceramic chip carrier to provide a sensor for temperature regulation. The sapphire entrance window will be of a high optical quality (double path wavefront error of < 50 nm rms), good surface quality (defects meet 5/2x0,05 DIN3140), and AR coated with transmission > 98% over range 400-950nm.

Philippe Feautrier has performed extensive thermal modeling[9] of the CCD, Peltier cooler, package, proposed clamping arrangement, and water-cooled heat exchanger. The results show that for 10 °C water temperature in the heat exchanger, the Peltier can cool the CCD to below -45 °C. Some results of Feautrier's simulation of CCD temperature for different Peltier currents can be found in the left plot of

Fig. 12. This will enable the dark current specification (0.01 e/pix/frame) of the standard silicon device to be easily achieved when the image area is operated in the fully inverted mode and comes very close to meeting the goal requirement (0.001 e/pix/frame). Refer to right plot in

Fig. 12 for modelling results provided by e2v of dark current versus temperature.

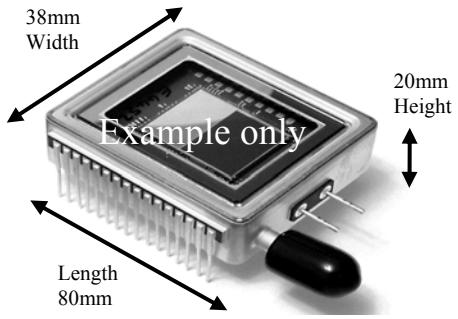

Fig. 11. Photograph of CCD65 Peltier cooling package. The AO CCD220 detector will use a similar Peltier package. Dimensions shown are the requirements on the maximum package size.

The high speed operation of the package was optimised by reducing parasitic inductance of the connections between the CCD and the pins of the package by increasing track widths as much as practical and providing ground planes above and below tracks on the ceramic insert (to which the CCD is glued) and package ceramic feed-through. In addition, the camera electronics will use a special pressed contact arrangement to make electrical contact at the ceramic feed-through rather than at the end of the package pin if a traditional ZIF socket was used. Simulation performed by Christian Guillaume[13] showed that any parasitic inductance will form an LC circuit with the clock phase capacitances (especially

the high capacitances of the image and store clocks) and if care is not exercised could generate destructive ringing voltages or when damping serial resistances are inserted reduce the maximum attainable clocking speed.

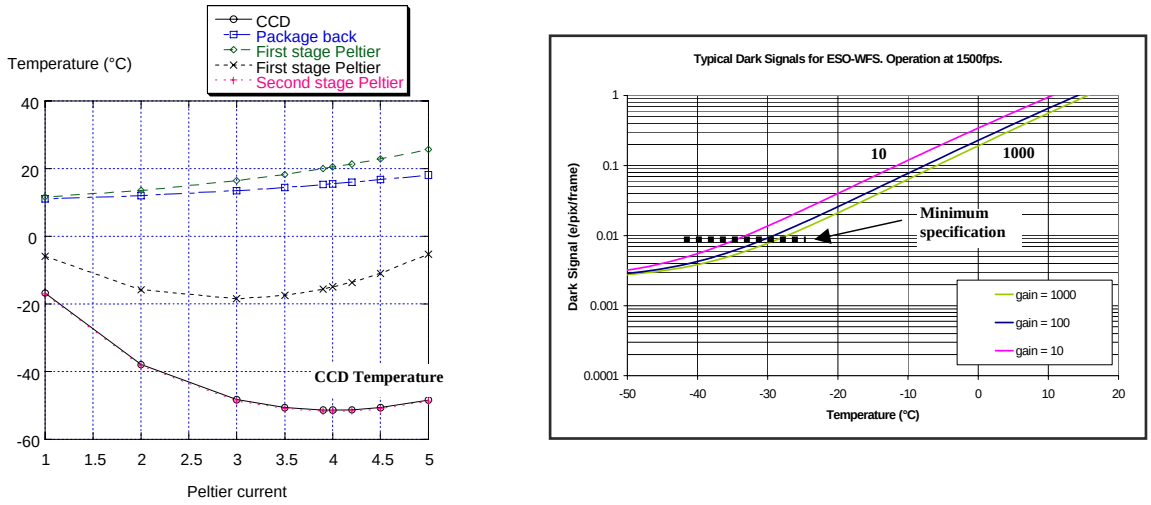

Fig. 12. Results of thermal and dark current modelling. Left: Predicted temperature of the CCD versus Peltier current modelled by Philippe Feautrier[9]. Right: Dark current versus temperature modelled by e2v for the baseline standard silicon CCD220 when the image area is operated fully inverted.

9. SCHEDULE

The major milestones (

Fig. 13) of critical design review, CDR (Sept 2005), package review (Jan 2006), and Test Camera design review (Mar 2006) have been successfully passed. The CCDs have been manufactured and probe testing has begun. Everything is on schedule for final delivery of devices in Q2 2007. The Test Camera is being developed by Gach et al[5] on behalf of ESO and will be loaned to e2v for testing. A copy of the Test Camera will be used by the IAC (JJDG) to do acceptance test. ESO are developing the New General detector Controller[14, 15, 16] (NGC) to support the CCD220 for deployment on the VLT.

The test plan is for e2v to do parametric and functional tests and measure standard parameters such as noise, gain, cosmetics, dark current, smearing, and CTE and for IAC (Canary Islands) and ESO to do full acceptance tests plus make the more demanding measurements of crosstalk, PRNU, fringing, and PSF.

Milestone	Date
Kick-off meeting	March 2005
CCD220/219 Design Review	September 2005
Package Design Review	January 2006
Test Camera Design Review	March 2006
Mechanical samples delivery	July 2006
ESO supplied Test Camera Delivery	October 2006
Devices delivery	Q2 2007

Fig. 13. Major milestones of the CCD220 development.

10. CONCLUSION

Several European institutions under the umbrella of OPTICON have formed a very good working relationship with e2v to develop a new 240x240 pixel wavefront sensor detector, CCD220, with subelectron read noise at 1,200 fps that will enable future AO systems to provide the image quality and stability to guarantee the success of the next generation of instruments on 8 to 10-m class telescope. Baseline development is low risk by extending existing e2v L3Vision technology to multiple outputs and metal buttressing parallel clock structures. In addition higher risk (more speculative) but higher performance devices in deep depletion silicon and with an electronic shutter will be developed in parallel.

The challenge to obtain good PSF, low dark current and CICs at the same time for the deep depletion and shuttered variants was described together with operating and clocking techniques that should allow all specifications to be simultaneously met.

For compactness and low maintenance the CCD is mounted in an optimised Peltier cooled package. Modelling has shown that by using an optimised custom Peltier, operating temperature lower than -45 °C will be achieved and this will enable dark current specifications to be surpassed.

Development has passed major milestones and is on-schedule for delivery of devices by Q2 2007.

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