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2009 INTERNATIONAL IMAGE SENSOR WORKSHOP

June 26-28, 2009 Bergen, Norway

Mark Downing, O. Iwert.
ODT/ Instrumentation division ESO


Agenda:

- **None**
- **Just report on some of the interesting developments in detectors**

Major Objective

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- Find out about the latest trends in CMOS imagers.
- Get answers to the question: **Are we crazy**?
  - Can a 1680x1680 24 pixels CMOS imager be developed with **< 3e RON at 700fps**.
- Assess "state of the art" performance w.r.t.
  - RON, dark current, image lag, read speed, RTS noise.
- Make new contacts and discover new potential suppliers.

A large number of companies are now doing Backside Illuminated CMOS

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Improved colour separation for a backside illuminated image sensor with 1.4 µm pixel pitch

Jens Prima(*,1), *Francois Roy*(1), *Hugues Leininger*(1), *Christophe Cowache*(1), *Jerome Vaillant*(1), *Luc Pinzelli*(1), *Daniel Benoit*(1), *Norbert Moussy*(2), *Benoit Giffard*(2)

(1) FTM Imaging, STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles, France

A Manufacturable Back-Side Illumination Technology using Bulk-Si Substrate for Advanced CMOS Image Sensor

S.G. Wuu[1], C.C. Wang, D.N. Yaung[1], Y.L. Tu[1], J.C. Liu[1], T.H. Hsu[1], F.J. Shiu[1], C.Y. Yu[1], G.Y. Shiau[1], R.J. Lin, C.S.Tsai[1], L. Tran[1], SSChen[1], CCWang[1], SYHuang[1], H. Rhodes[2], D. Tai[2], Y. Qian[2], D. Mao[2], S. Manabe[2], A. Shah[2], R. Yang[2], J.C. Hsieh[3], Calvin Chang[3], C.W. Lu[3], Shawn Tseng[3]

[1]Taiwan Semiconductor Manufacturing Company, Hsin-Chu, Taiwan, R.O.C.
[2]OmniVision Technologies, Inc., 4275 Burton Drive, Santa Clara, CA 95054

A 1.4 µm Pixel Backside Illuminated CMOS Image Sensor with 300 mm Wafer Based on 65 nm Logic Technology

Y.Kohyama, H.Yamashita, S.Uya, T.Yoshida, N.Sakurai, I.Inoue, T.Yamaguchi, K.Nagata, *H.Harakawa, *A.Murakoshi, *T.Harada, *M.Takahashi, *M.Morita, *K.Tanida, *M.Dohi, *K.Takahashi, *K.Iwade, *T.Matsumura, *H.Sugiyama, H.Goto and K.Tomioka

Imaging Device Marketing & Engineering Dept., System LSI Division, Toshiba Corporation Semiconductor Company

Monolithic and Fully-Hybrid Backside Illuminated CMOS Imagers for Smart Sensing

Padmakumar R. Rao, Kyriaki Minoglou, Koen De Munck, Deniz Sabuncuoglu Tezcan, Chris Van Hoof and Piet De Moor

IMEC, Kapeldreef 75, B-3001 Leuven, Belgium
Email: ramach@imec.be, Ph : +32 16 281245

The Mass Production of BSI CMOS Image Sensors

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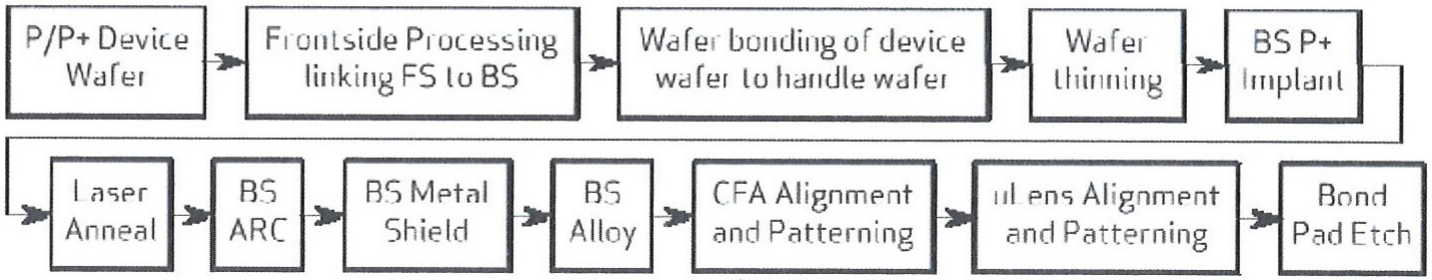
OmniVision

BSI Process



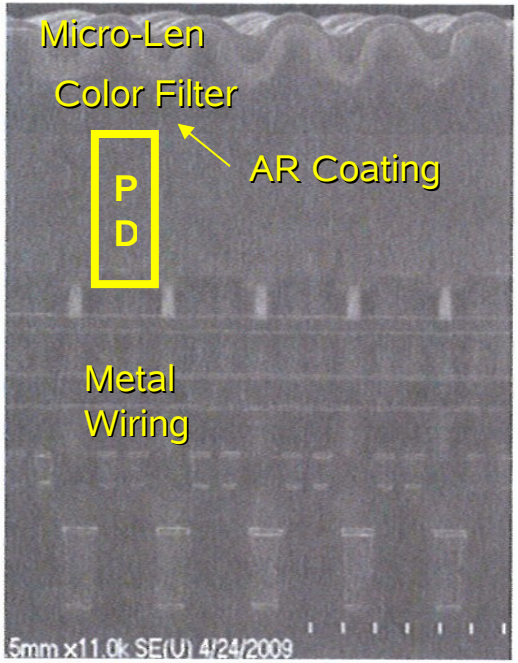


Figure 1. 1.4µm pixel cross-sectior

- Collaborate closely with TSMC
- Thin -> P+ implant then laser anneal
- See Olaf's talk

OmniVision

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Table 1. 1.4µm and 1.75µm pixel performance

Parameter	1.4 µm	1.75 µm
FWC	4500 e	6500e
Peak QE - R	43.8%	53.0%
Peak QE - Gb	53.5%	60.1%
Peak QE - Gr	53.6%	60.2%
Peak QE - B	51.6%	60.4%
R/B	5.70%	4.8%
G/B	14.40%	11.4%
R/G	11.20%	9.2%

Parameter	1.4 µm	1.75 µm
B/G	31.80%	24.0%
G/R	35.20%	28.9%
B/R	7.30%	5.4%
Sensitivity (530nm)	671 mV/Lux-sec	1500 mV/lux-sec
Read Noise (pixel/periph)	1.9/1.3 e	2.1e/1.3e
PRNU	0.75%	0.8%
Lux for 10:1 SNR	110 Lux	60 Lux
Dark Current (50 C)	27 e/sec	22 e-/s

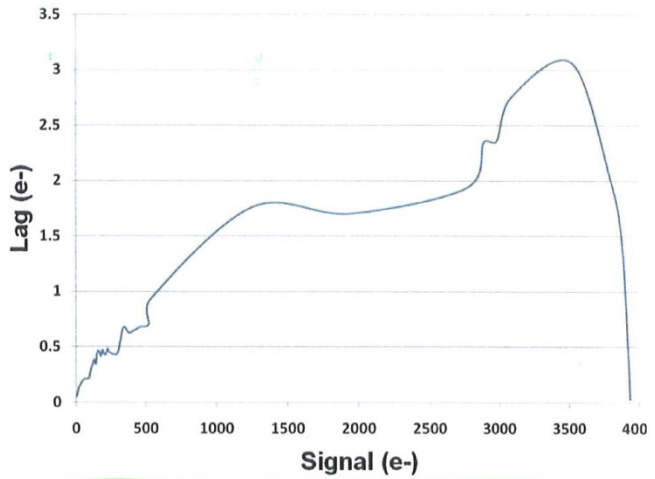

Figure 6. Lag(e) vs signal level (e) for 1.4µm pixel

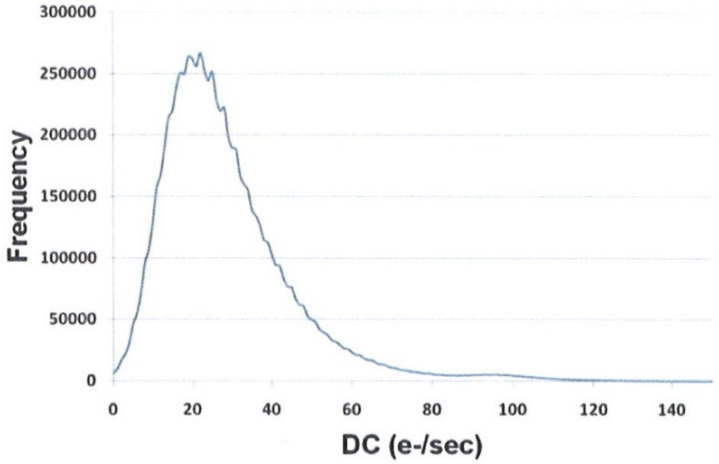

Figure 8. Dark current histogram for 1.4µm pixel at 50°C

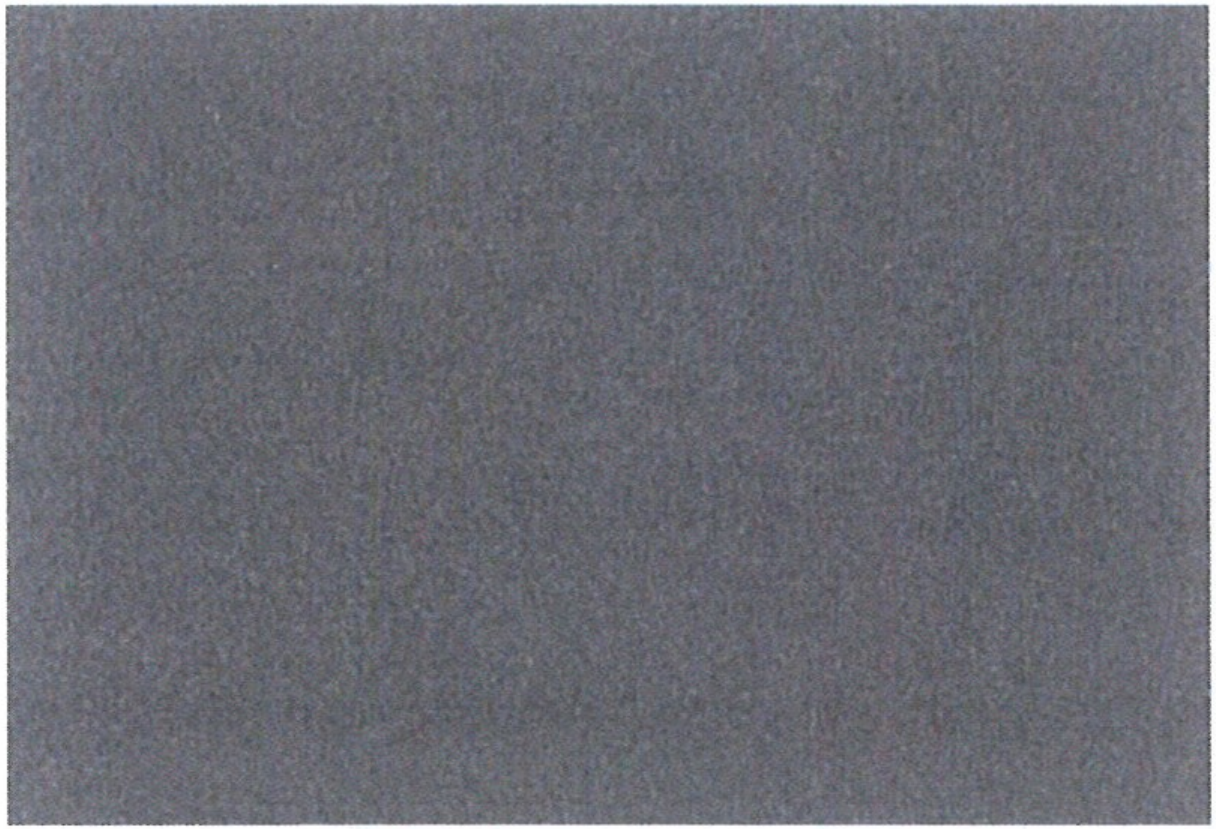

Figure 7. RAW dark image

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High Speed Imagers

Limitations to the frame rate of high speed image sensors

G. Meynants, G. Lepage, J. Bogaerts, G. Vanhorebeek, X. Wang

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The introduction of CMOS image sensor technology has accelerated the development of high frame rate image sensors, which are used in broadcast, sports and research applications, and in motion and impact analysis. The CIS architecture allows exchanging resolution for frame rate. Small

image sensors require higher frame rates that require further optimization. Typically larger pixel sizes are used for reasons of light sensitivity, which allows implementing several tricks to increase frame rate. Most of them consist in either reducing the capacitance of a column, introducing more parallelism or implementing buffering or repeaters.

Progress in 1.25-inch Digital-Output CMOS Image Sensor Developments for UDTV Application

I. Takayanagi, S. Osawa, T. Bales, K. Kawamura, N. Yoshimura, K. Kimura, H. Sugihara, E. Pages, A. Andersson, S. Matsuo, T. Oyama, M. Haque, H. Honda, T. Kawaguchi, M. Shoda, B. Almond[1], P. Pahr[2], S. Desumvila[1], D. Wilcox[1], Y. Mo[3], J. Gleason[3], T. Chow[3], J. Nakamura. Aptina Japan, LLC.; [1] Aptina UK, Ltd.; [2] Aptina Norway, AS.; [3]Aptina LLC, USA

A 2.5 inch, 33Mpixel, 60 fps CMOS Image Sensor for UHDTV Application

Steven Huang, Takayuki Yamashita[1], Yibing Wang, Kai Ling Ong, Kohji Mitani[1], Ryohei Funatsu[1], Hiroshi Shimamoto[1], Lin Ping Ang, Loc Truong, Barmak Mansoorian. Forza Silicon Corporation, USA; [1]NHK Science and Technical Laboratories

A High Speed Pipelined Snapshot CMOS image sensor with 6.4 Gpixel/s data rate

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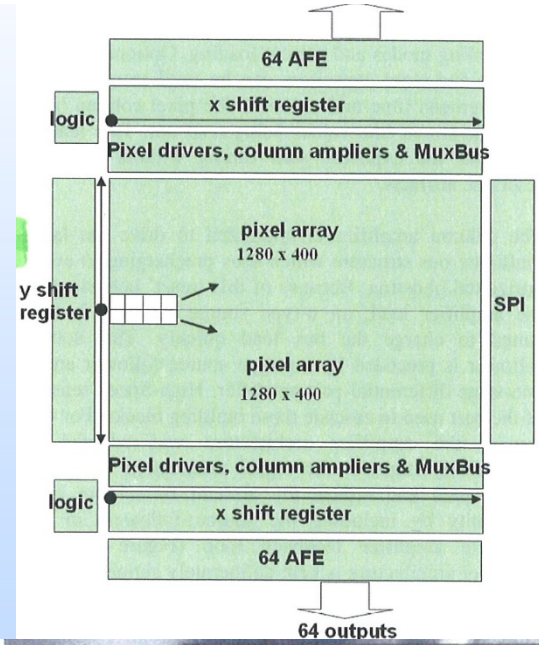
Parameter	Value	Remark
Pixel size	20 x 20 μm^2	
Pixel array	1280 x 800	
Pixel type	6T	Pipelined, snapshot shutter
Interface	Analog Out	1.3 V swing
Frame Rate	6242 fps	For full frame readout
Data Rate	65 MSamples /s	128 outputs
Main power supply	3.3 V	
Power consumption	2.5 W	
Fill Factor	58 %	
Full well	38 ke^-	
Read noise	28 e^-	In the dark
Responsivity	13100 V/s/(W/m^2)	@ 550 nm
Conversion gain	32 uV/e-	@ the sensor output
DR	62.6 dB	Intra-scene
MTF	> 60%	@ Nyquist frequency
FPN	2.9 %	rms of full output swing
RNU	3.1 %	rms of signal level
Dark Signal	85 mV/s	@ room temperature
Chip size	29 x 25.5 mm^2	
Maximum output load	10 pF	
Package	314 pins PGA	With built-in Peltier cooler



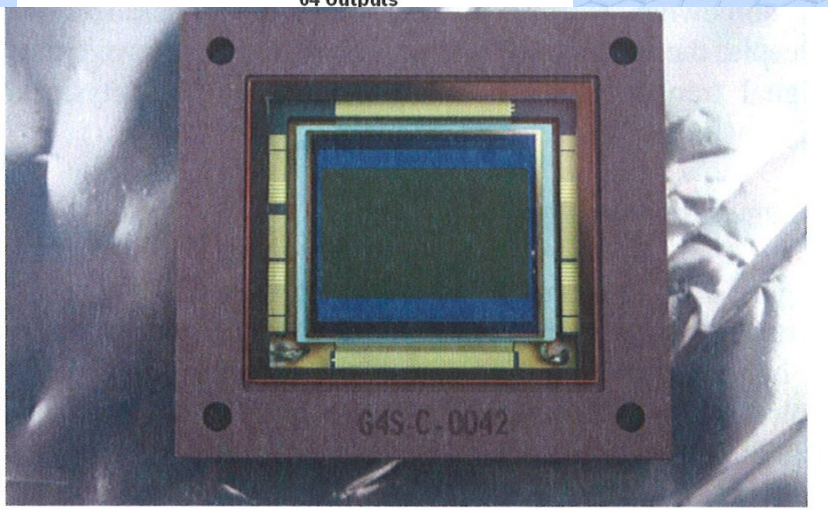


Figure 4: 314 pins PGA package with built-in peltier

Numerous novel techniques to improve RON.

- Common comment is that it is only a matter of time before sub-electron RON will be possible

Random Telegraph Signal Noise

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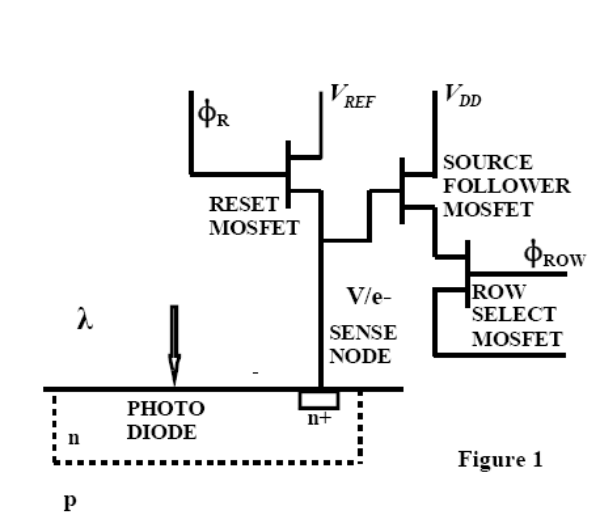


Figure 1

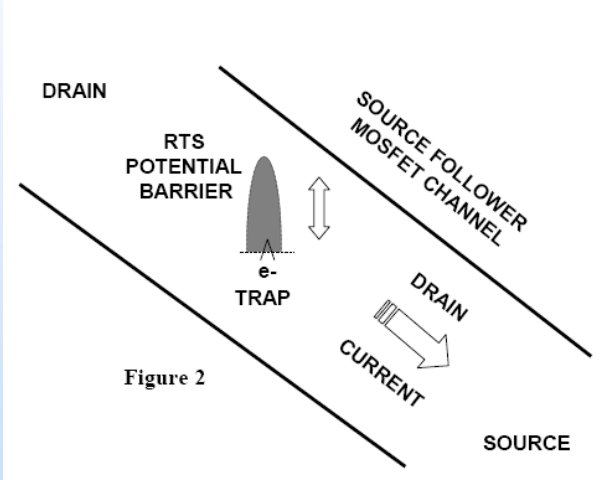


Figure 2

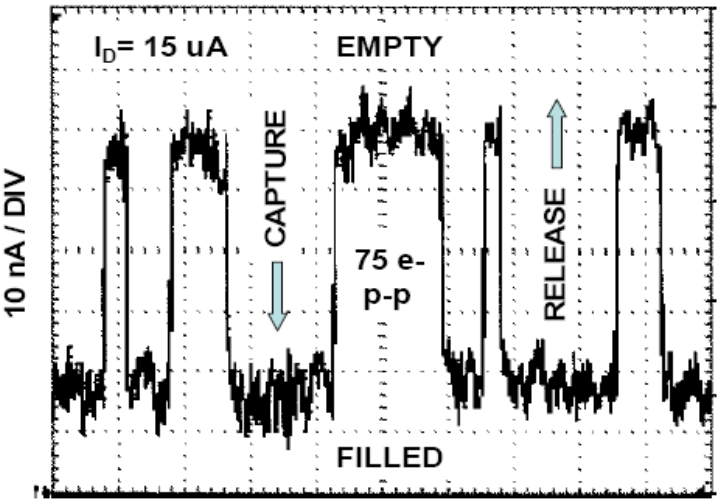
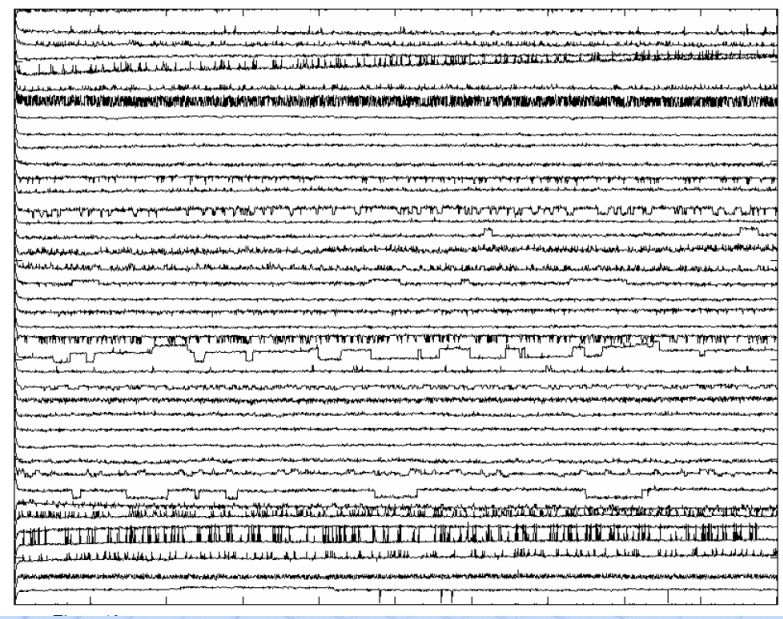


Figure 3



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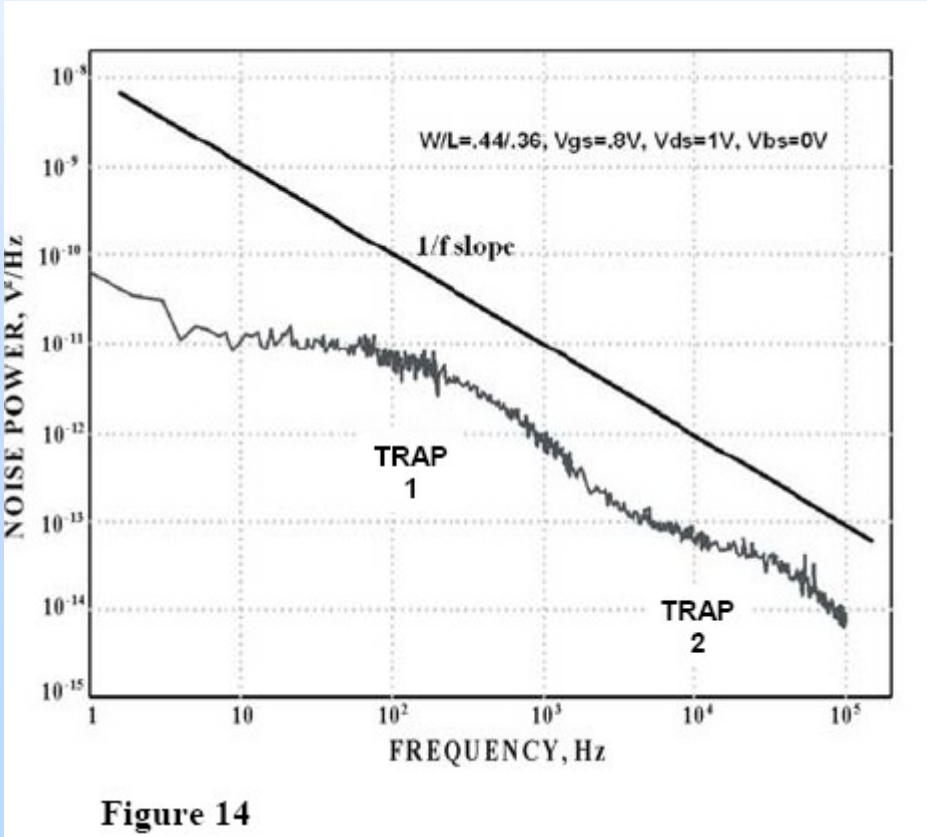

Figure 14

Random Telegraph Signal Noise

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Characterization of In-Pixel Buried-Channel Source Follower with Optimized Row Selector in CMOS Image Sensors

Yue Chen, Xinyang Wang, Adri J. Mierop and Albert J.P. Theuwissen
Electronic Instrumentation Lab., Delft University of Technology,

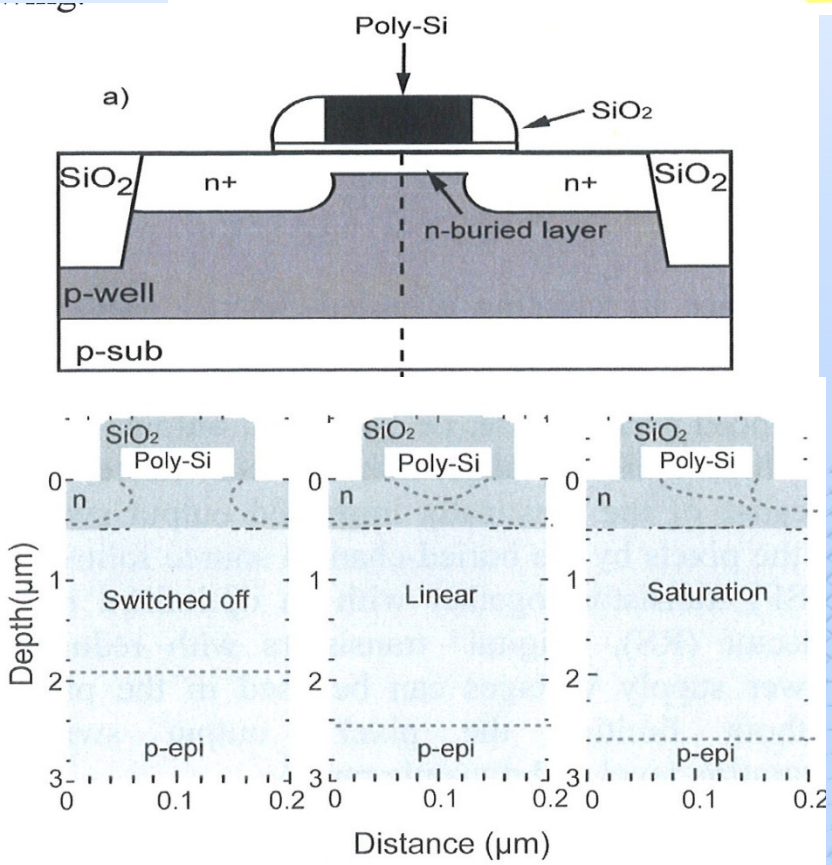


Figure 2. Expected operation modes of a buried-channel nMOS transistor

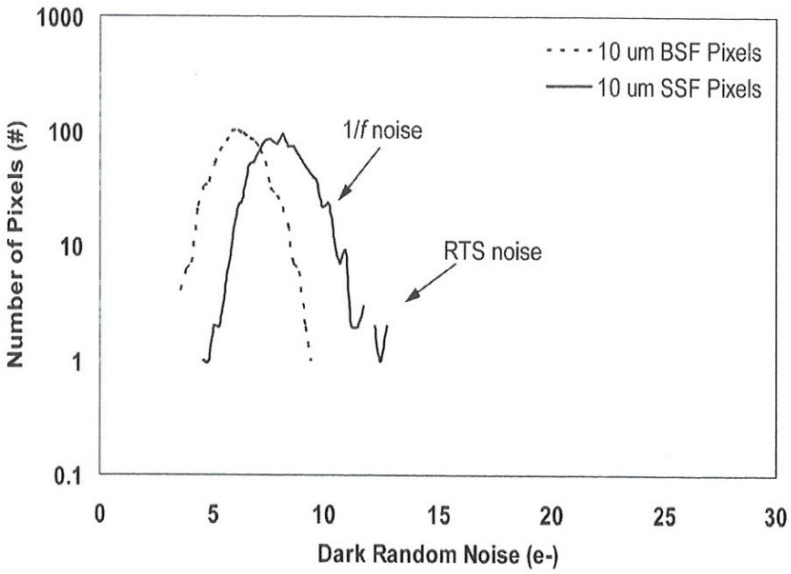
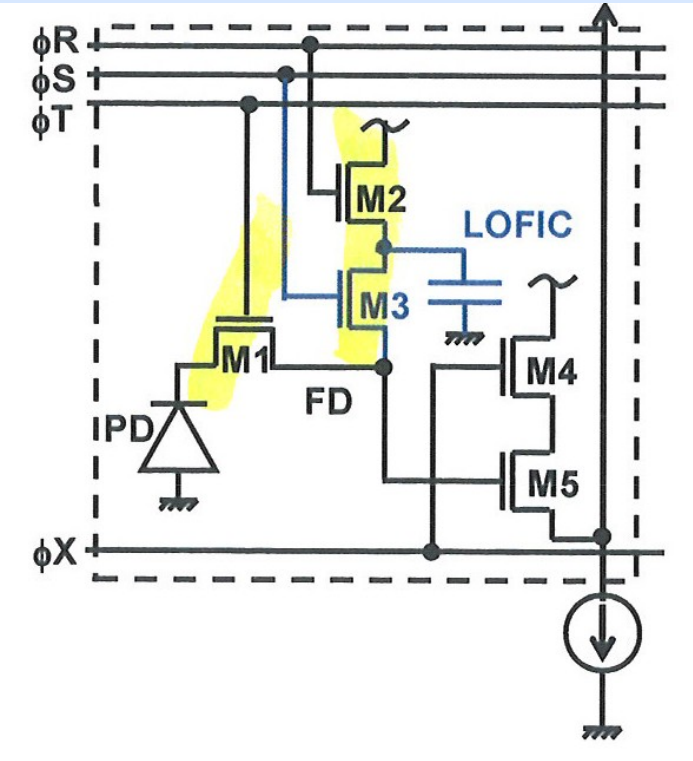


Figure 6. Histograms of the dark random noise for BSF and SSF pixels

A 200-μV/e$^-$ CMOS Image Sensor With 100-ke$^-$ Full Well Capacity

Satoru Adachi, *Member, IEEE*, Woonghee Lee, Nana Akahane, Hiromichi Oshikubo, Koichi Mizobuchi, *Member, IEEE*, and Shigetoshi Sugawa, *Member, IEEE*



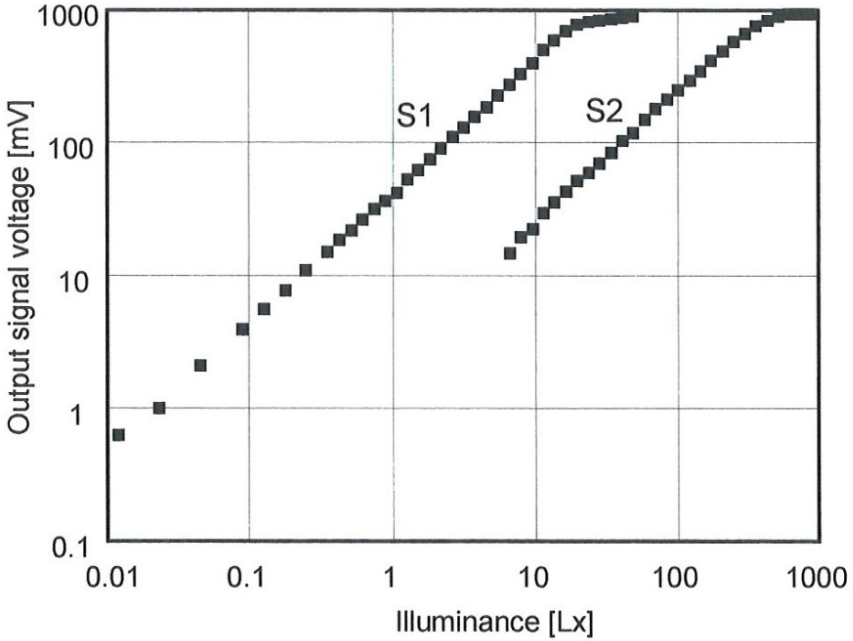


Fig.6 Photo-electric conversion characteristics

A 200-μV/e$^-$ CMOS Image Sensor With 100-ke$^-$ Full Well Capacity

Satoru Adachi, *Member, IEEE*, Woonghee Lee, Nana Akahane, Hiromichi Oshikubo, Koichi Mizobuchi, *Member, IEEE*, and Shigetoshi Sugawa, *Member, IEEE*

Effective number of pixels	800 × 600	
Pixel pitch	4.5 μm	
Process technology	0.18μm 2P3M CMOS	0.18μ
Operation voltage	5 V	
Frame rate	60 fps	
Differential amplifier gain	x1, 2, 4, 8	
Temporal noise (Gain=x2)	0.19 mVrms (2.3 e-rms)	0
Saturation of S1 (Gain=x2)	770 mV	
Saturation of S2(Gain=x1)	750 mV	
Full well capacity	154 Ke-	
Dynamic range	96.5 dB	

Synchronous and Asynchronous Detection of Ultra-Low Light Levels

Christian Lotto[1,3], Peter Seitz[2,3]. [1]CSEM SA, Photonics Division, Switzerland; [2]CSEM SA, Nanomedicine Division, Switzerland; [3]EPFL STI IMT-NE, Federal Inst. of Technology, Switzerland

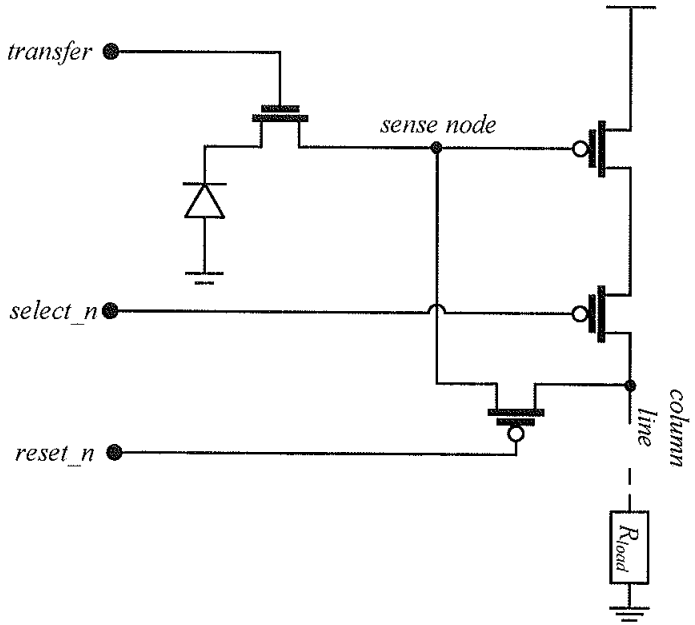


Fig. 4: Amplifying 4-Transistor-Pixel for Ultra-Low-Noise CMOS Image Sensor

We propose a novel synchronous CMOS image sensor pixel with an in-pixel voltage amplifier (see figure 4) [4]. Due to amplification, the impact of electronic noise from downstream circuits is effectively reduced to a high degree. The remaining readout noise is dominated by the pixel amplifier's performance.

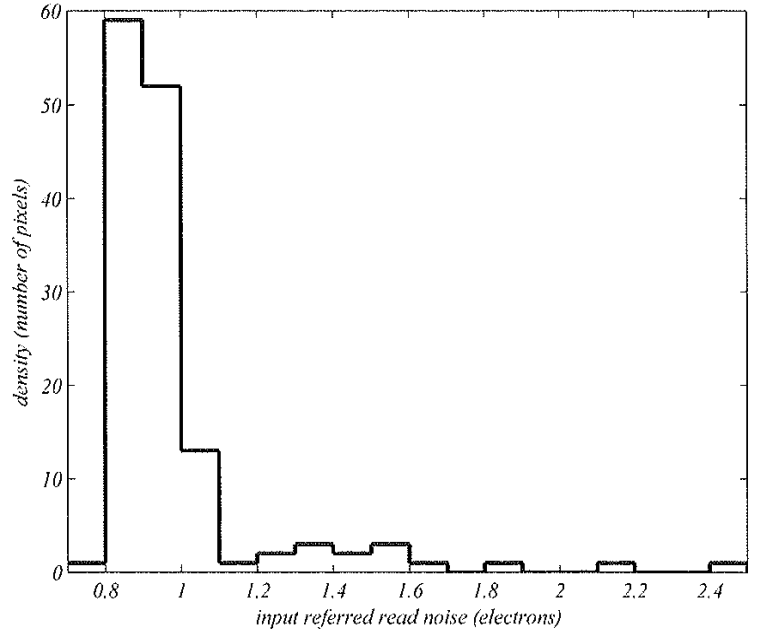


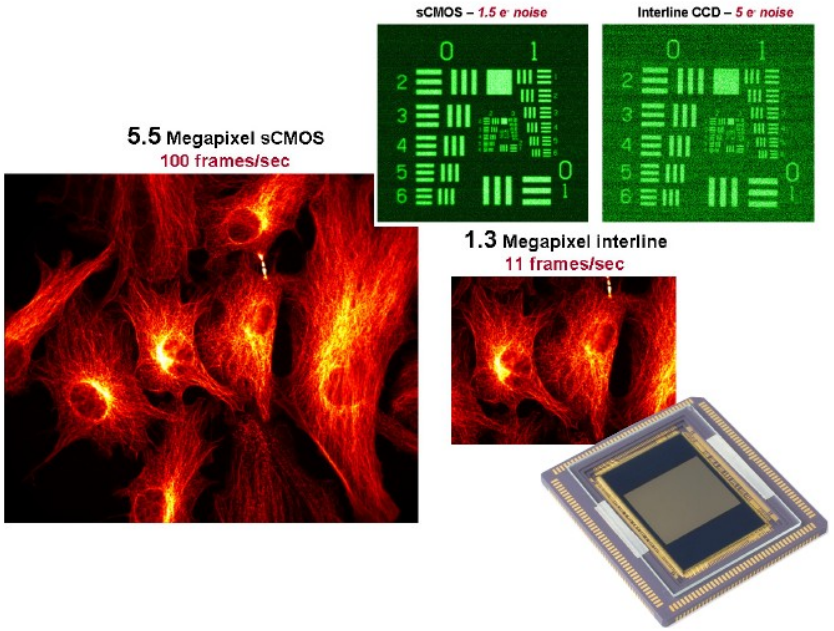
Fig. 7: Readout noise distribution for 140 pixels.

ANDOR™ TECHNOLOGY Fairchild imaging pco. imaging

sCMOS

Scientific CMOS Technology

A High-Performance Imaging Breakthrough



White Paper : Dr. Colin Coates, Andor Technology
Dr. Boyd Fowler, Fairchild Imaging
Dr. Gerhard Holst, PCO AG

Wide Dynamic Range Low Light Level CMOS Image Sensor

Boyd Fowler, Chiao Liu, Steve Mims, Janusz Balicki, Wang Li, Hung Do, and Paul Vu

Fairchild Imaging, Inc., 1801 McCarthy Blvd., Milpitas, California, USA

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Fairchild imaging

TABLE I
SENSOR PROPERTIES (PIXEL 7)

Parameters	High gain channel	Low gain channel
Conversion gain (DN/e-)	2.1	0.065
Read noise (e- RMS)	0.80 (median)	7.2 (median)
	1.15 (mean)	7.0 (mean)
	1.10 (std)	1.5 (std)
Dark Current (e-/pixel/sec) @ 20C	9	9
Full well capacity (e-)	1.4K	42K
Linearity (% RMS)	1.3	0.15
Dynamic range	1750 (median)	5800 (median)
Max pixel clock (MHz)	287	287
Gain FPN (DN/e-RMS)	0.084	3.9e-5
DSNU (e-/pixel/sec RMS) @ 20C	3.5	3.5
Offset FPN (e- RMS)	13	210

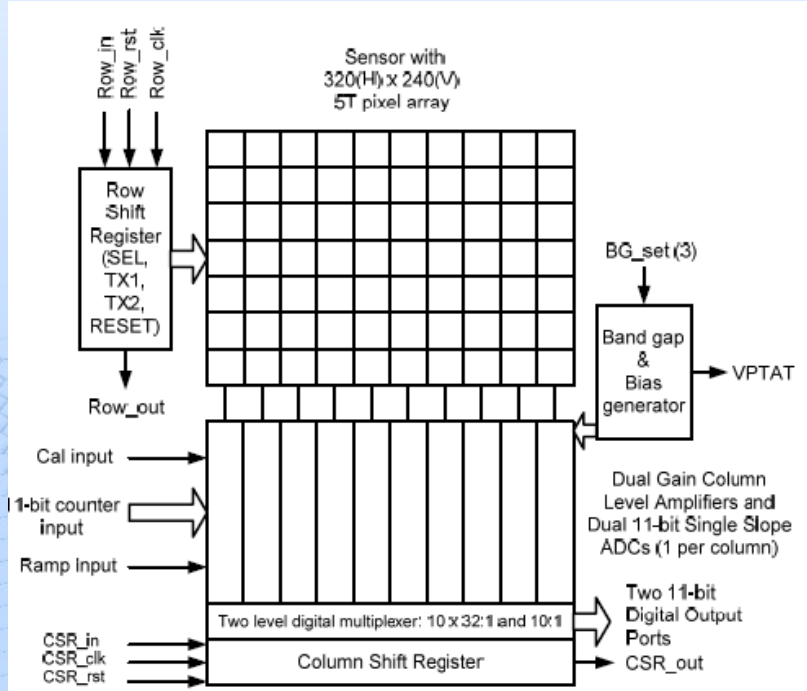

Figure 1. Sensor Block Diagram

The sensor has a 22-bit digital output port operating at up to 287 MHz. The digital data at the column is transferred to the output pins using a two level 320:1 digital multiplexer. Note that each pixel is simultaneously readout twice, once through a high gain amplifier and once through a low gain amplifier. Both the high gain amplifier and the low gain amplifier outputs are digitized to 11 bits. The maximum frame rate of

sCMOS

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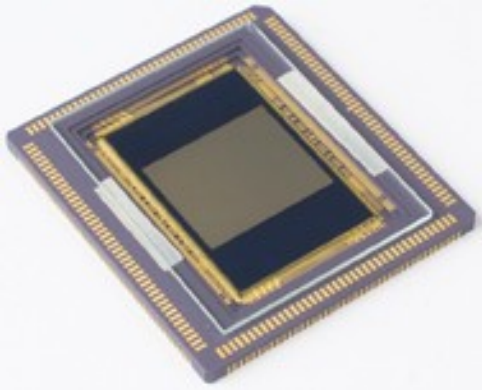
Performance highlights of the first sCMOS technology sensor include:

Sensor format	5.5 megapixels 2560 (h) x 2160 (v)
Read noise	< 2 e^- rms @ 30 frames/s; < 3 e^- rms @ 100 frames/s
Maximum frame rate	100 frames/s
Pixel size	6.5 µm
Dynamic range	16,000:1 @ 30 frames/sec
QE_{max}	60%
Read out modes (User selectable)	Rolling and Global Shutter



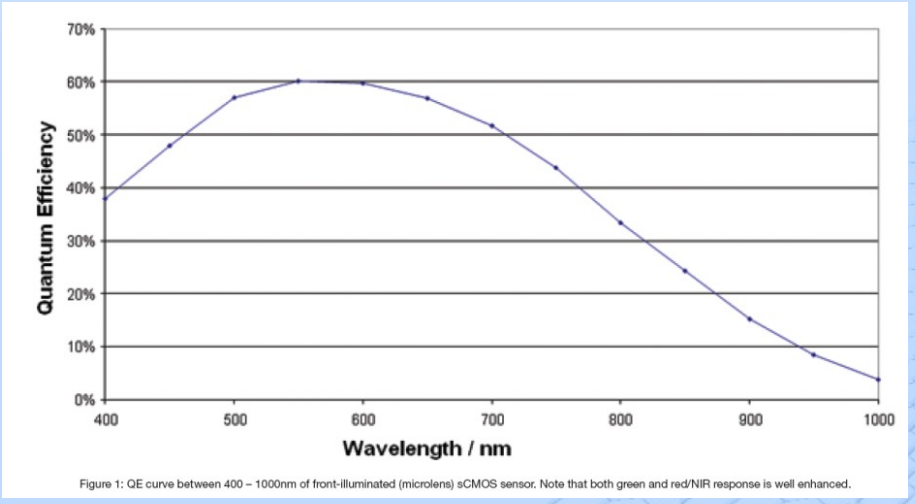


Figure 1: QE curve between 400 – 1000nm of front-illuminated (microlens) sCMOS sensor. Note that both green and red/NIR response is well enhanced.

Array Size (H x V)	Rolling Shutter mode (frames per second)
2560 x 2160 (full frame)	105
2048 x 2048 (4 megapixel)	110
1300 x 1024 (1.3 megapixel)	220
512 x 512	440
256 x 256	880
128 x 128	1760

- Looking at possibility to get loan and purchase a camera from Andor

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CCD Advances

High Speed Impactron CCD Line Sensor with Color Sensing Capability

Izumi Kobayashi [1], Jaroslav Hynecek [2]

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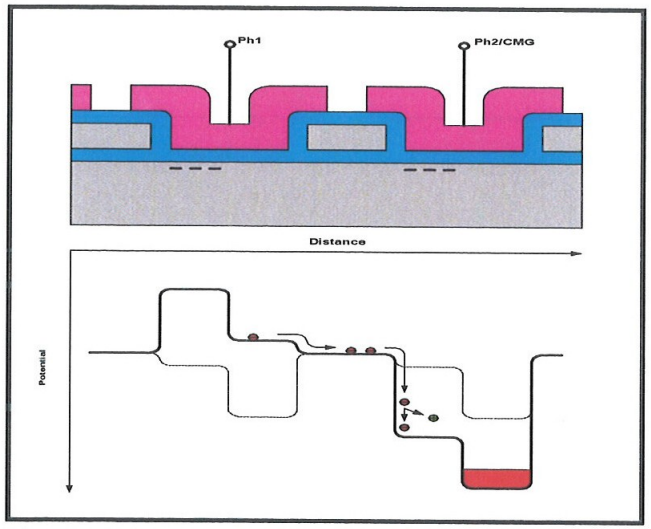

Fig.1. Charge multiplication concept.

Table T1: Summary of the device performance parameters:

ITEM	TARGET	ACTUAL
Pixel Size	10x10um	←
Active Pixel Number	3600x2 pixel	←
OB Pixel Number	20 pixel	←
Dummy Number	6 pixel	←
Output Terminal	4-ch	←
PD Cell Well Capacity	50ke- ~ 80ke-	**74ke-**
Serial/CMG Well Capacity	50ke- ~ 80ke-	**74ke-**
FD Well Capacity	80ke- ~ 110ke-	**98ke-**
Line Rate	10kHz ~ 15kHz	**13kHz**
Serial Transfer Frequency	46MHz ~ 80MHz	**60MHz**
CMG Register Frequency	23MHz ~ 40MHz	**30MHz**
CMG Gain	500x ~ 1000x	←
Amp. Conversion gain	12uV/e ~ 14uV/e	**13.2uV/e**
Amp. Noise floor	1e	**<1e**

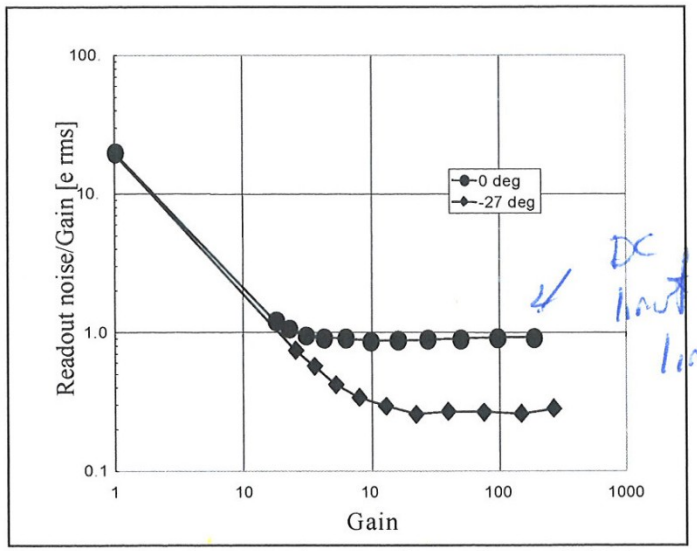

Fig.5. Readout noise as function of Gain

- Meet Jerry; the concept man behind EMCCD and Texas Instrument Impactron technology.
- No over-illumination problem as pixels have anti-blooming and only modest gains of 10-20 are required.

Low Noise High Speed Amplifier

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A 2/3-inch Low Noise HDTV FT CCD-Imager for 1080i180, 1080p90 and 720p120 Scanning at Constant Image Diagonal

Peter Centen[1], Holger Stoldt[2], Jan Visser[3], Jan T. Bosiers[2]

reaches a pixel rate of 223Mpixel/sec. The on-chip amplifier has a bandwidth >241MHz. At 112MHz it has a Noise Electron Density of NED=0.59 e2/MHz and after CDS, 8 electrons in 30MHz bandwidth.

The classical parameters for noise optimization of the on-chip amplifier are the Width, the Length and the Bias current of the source follower in the detection node [10,11]. Noise optimization stops at the statement to make the channel length as small as possible. An additional degree of freedom for further optimization is found when the oxide thicknesses of the MOS transistors in the on-chip

In **Figure 5** the state-of-the-art amplifier noise performance is given using reference to the reset frequency [8]. Noise levels in the range of 4.6 to 2 electrons are reported [2,13,14] but only for CMOS imagers and only at a high gain setting of the column amplifiers, reducing saturation level at the same time, or with 4 channel readout [14]. In the past sub-electron noise levels where reported for CCDs but always for bandwidths less than 1MHz.

Type	Ref	Reset Frequency	Ampl. Type	Conversion gain	Noise after CDS/ √Resetfrequency
FF-CCD	ED1997 Burke	100 kHz	Source Follower	20 µV/e	6.3 e/√MHz
CMOS	AIS2003 Krymski	50 kHz	Source Follower +Gain	60 µV/e	6.3 e/√MHz
FF-CCD	AIS2005 Draijer	25 MHz	Source Follower	40 µV/e	2.8 e/√MHz
CMOS	ISSCC2005 Kozlowski	104 kHz	Source Follower +Gain	?µV/e	46 e/√MHz
CMOS	ISSCC2006 Yoshihara	156 kHz	Source Follower +Gain	40 µV/e	17.7 e/√MHz
CMOS	ISSCC2007 Takahashi	156 kHz	Source Follower +Gain	75 µV/e	11.6 e/√MHz
CMOS	ISSCC2007 Cho	625 kHz	Source Follower +Gain	101 µV/e	10.4 e/√MHz
FT-CCD	This paper	111MHz	Source Follower	18 µV/e	1.3 e/√MHz

Figure 5: *State-of-the-art amplifier noise performance*

Other Applications

IR Detector

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A Monolithic Ge-on-Si CMOS Imager for Short Wave Infrared

B. Ackland, C. Rafferty, C. King, I. Aberg, J. O'Neill, T. Sriram, A. Lattes, C. Godek and S. Pappas.

NoblePeak Vision

500 Edgewater Dr., Ste 570, Wakefield MA 01880. USA.
Ph: +1(781) 224-9740 email: bdackland@noblepeak.com

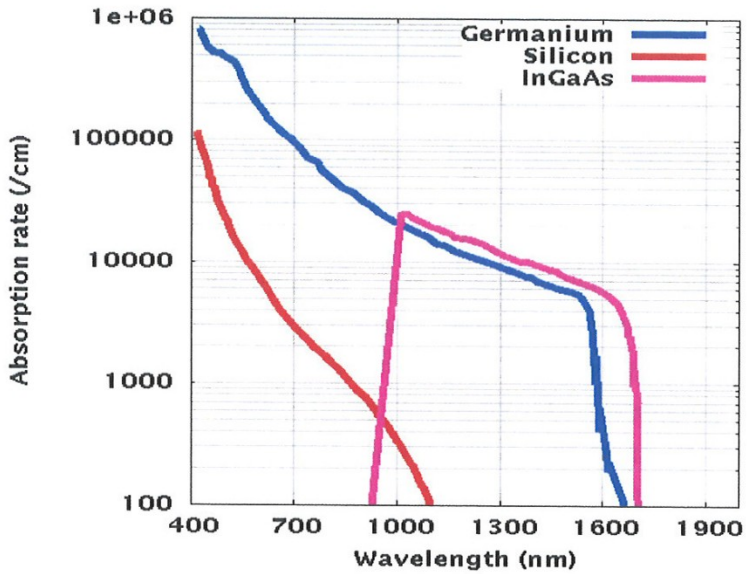

Figure 1 – Absorption in Si, Ge and InGaAs

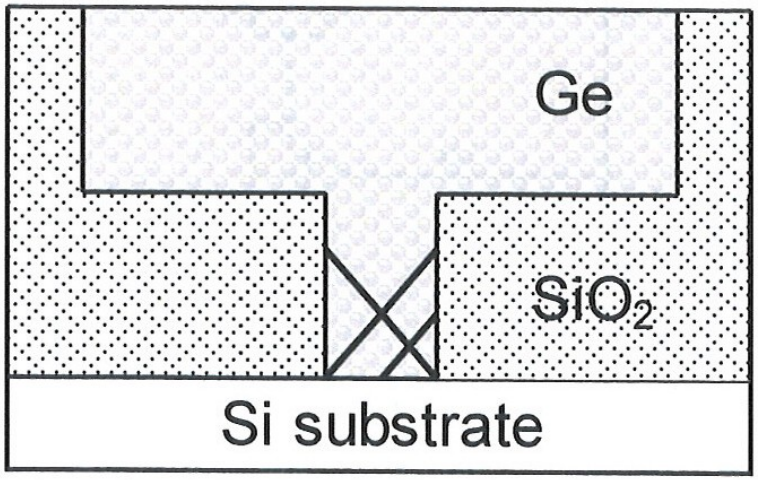

Figure 2 – Germanium selective growth

IR Detector

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A Monolithic Ge-on-Si CMOS Imager for Short Wave Infrared

B. Ackland, C. Rafferty, C. King, I. Aberg, J. O'Neill, T. Sriram, A. Lattes, C. Godek and S. Pappas.

NoblePeak Vision

500 Edgewater Dr., Ste 570, Wakefield MA 01880. USA.
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Detectors of size from 2 μm to 5.6 μm and imaging arrays with pixels of size 7 μm and 10 μm have been fabricated in this technology.

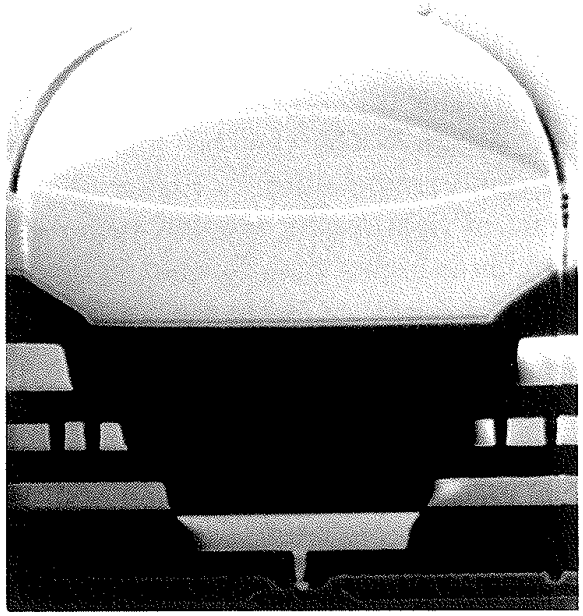

Figure 3 – Germanium diode embedded in CMOS

Smallest Sensors (endoscopes)

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400x400 pixel image sensor for endoscopy in 1.7mm^2 CSP package

Bram Wolfs [1], Cedric Esquenet [2], Walter Iandolo [3]

packaged, color sensor in the world. The sensor uses 2.8um pixels implemented using TSMC 0.18um CIS technology to achieve 400x400 resolution in a 1.78x1.78mm Chip Scale Package (CSP). A hybrid (analog/digital) fully differential I/O (patents pending) is capable of driving cables up to 5m long while keeping the total power consumption below 80mW.

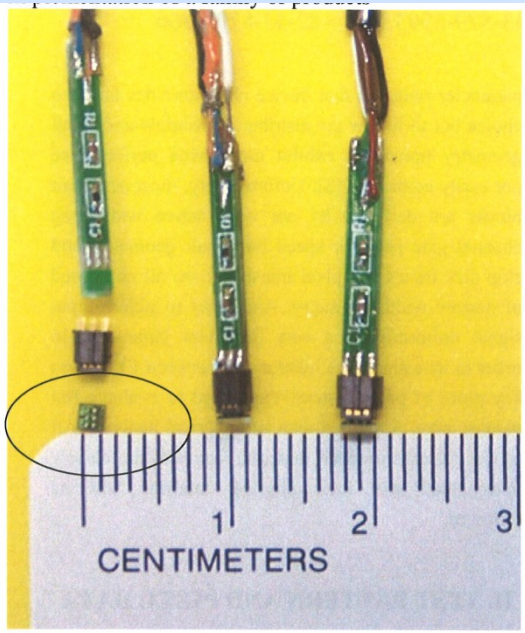

Figure 8 A family of 3 sensors (400x400 on the left) already connected to the tips of endoscopes[1]

Beauty

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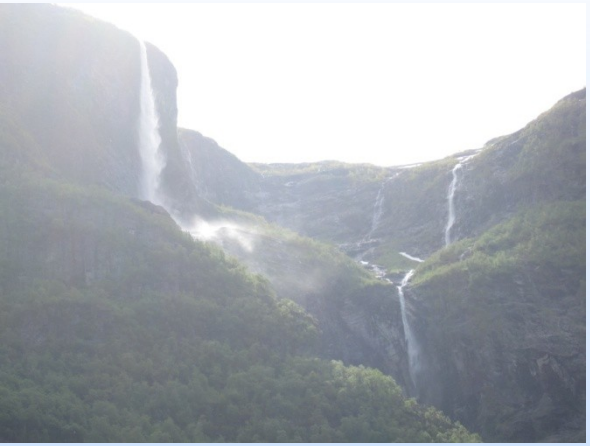

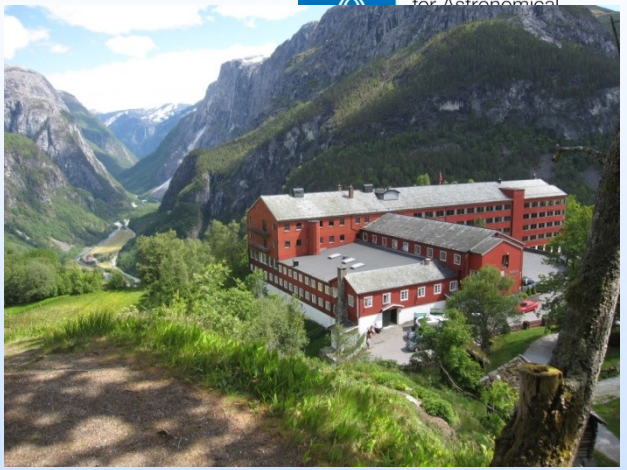





Fjords and Boats

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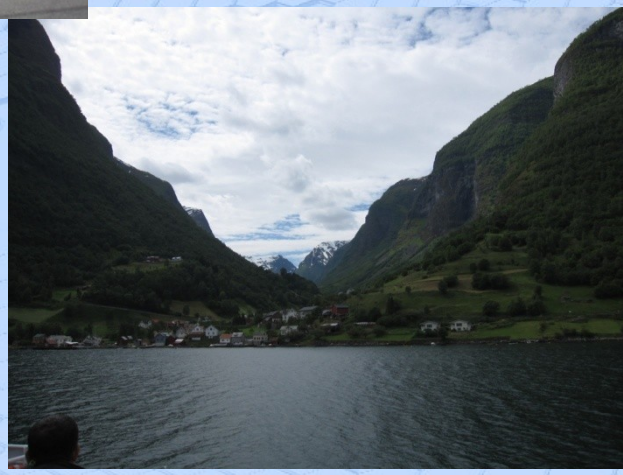

Art

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Food

New Friends

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RTS

noise [2]. Research has revealed that the dominated random noise sources in CMOS image sensors (CIS) are due to the lattice defects at Si-SiO_2 interface of the in-pixel source follower (SF) transistor [3, 4]. As CMOS processes scale down, the gate area of the transistors becomes so small that it easily happens to have only one active interface trap underneath the transistor's gate, which will induce the RTS noise. Because of this single electron trapping and de-trapping during the transistor operation, the RTS appears in pixels which have only one active interface defect and dominates the pixel temporal noise, which limits the imaging quality under low-light conditions [5]. Therefore, as long as a perfect clean gate interface can not be guaranteed, the 1/f or RTS noise will stay dominant in the random noise in pixels.

Fig.2 shows the pixel schematic and the operation diagram. The pixel schematic consists of a fully depleted photodiode (PD), a floating diffusion to convert the charge to the voltage (FD), a charge transfer switch (M1), an lateral over-flow integration capacitor (LOFIC), a switch between the FD and the LOFIC (M3), a reset switch (M2), a pixel source follower (M4) and a pixel select switch (M5). The basic concept in this pixel circuit is to use the switch M1 for a suitable overflow path of saturated photoelectrons and integrate overflowed photoelectrons in the FD and the LOFIC during a charge integration period.