High QE, 3e- RoN, fast 700fps, 1760x1680 pixels CMOS Imager

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ABSTRACT

The success of the next generation of instruments for ELT class telescopes will depend upon improving the image quality (correcting the distortion caused by atmospheric turbulence) by exploiting sophisticated Adaptive Optics (AO) systems. One of the critical components of the AO systems for the E-ELT has been identified as the Laser/Natural Guide Star WFS detector.

The development of the high resistivity silicon CMOS Laser/Natural Guide Star WFS detectors for the E-ELT is well advanced. The combination of large format, 1760x1680 pixels to finely sample the wavefront and the spot elongation of laser guide stars, fast frame rate of 700 frames per second (fps), low read noise (< 3e-), and high QE (> 90%) has made the development of this device extremely challenging. Two generations of the CMOS Imager will be built. The pioneering quarter sized device of 880x840 pixels capable of meeting first light needs of the E-ELT called NGSD (Natural Guide Star Detector) is in production and will be tested in the coming months. This will be followed by the larger full size device, the LGSD (Laser Guide Star Detector). The final detailed design is presented including the chosen pixel architecture; the approach of using massive parallelism (70,400 ADCs) to achieve the low noise at high pixel rates of ~3 Gpixel/s; the 88 channel LVDS data interface; the restriction that stitching (required due to the 5x6cm size) posed on the design and the solutions found to overcome these limitations. To enable read noise closer to the goal of 1e- to be achieved, a split wafer run has allowed devices to be manufactured using more speculative, but much lower read noise, Ultra Low Threshold Transistors in the unit cell.

1. INTRODUCTION

Spot elongation[1] of LGS is considered one of the major challenges of Adaptive Optics (AO) WaveFront Sensor (WFS) systems of ELTs. The spot elongation is due to the finite thickness of the sodium layer and the offset between the laser projection point and the sub-apertures of a Shack-Hartmann (SH) WFS. The

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elongation or spreading of the Laser Guide Star (LGS) image results in a decrease in the signal to noise ratio (SNR) resulting in an increase of the centroid error, and subsequently increased error of the wavefront phase reconstruction.

The current LGS WFS system for the E-ELT (an adaptive Telescope) baselines the following: 1) 4 Continuous Wave (CW) Sodium LGSs projected from the sides of the telescope; 2) enough laser power to provide 1000 photons per sub-aperture per frame, 3) high spatial sampling up to 84 x 84 sub-apertures (goal of 126 x 126 for later upgrade) and 20 x 20 pixels per sub-aperture to adequately sample the spot elongation, and 4) high temporal sampling of 700 Hz.

From the top level science requirements, the following requirements for a large LGS/Natural Guide Star (NGS) AO WFS detector[2] (called named LGSD) have been justified:

1) Minimum format size of 1680x1680 pixels,
2) Big pixels of 20-28µm, to ease the optical system design (mechanical alignment and stability), but small enough to avoid excessive dark current/counts, charge transfer inefficiency (image lag), or manufacturability problems,
3) Versatility of 100% fill factor for maximum flexibility; to make it possible to decide later to change laser projection site and/or mix of sub-apertures/pixels,
4) Low dark current and read noise such that total noise is < 3e- rms,
5) High Quantum Efficiency (QE) over wavelength of 450-950nm (for NGS applications) and especially at 589 nm (LGS wavelength),
6) Equivalent exposure time of frame rates from 100fps to 700fps with goal of 1000fps with slightly (gracefully) degraded performance,
7) Low read out latency (time between end of exposure and image available at output pin < 7 % of exposure time) so that corrections can be computed and applied as quick as possible after the exposure ends,
8) Detection signal limit of 4000e-/pixel; laser power will be limited so the system will be photon starved (expect only 1000 photons per sub-aperture per frame),
9) Good spatial characteristics, Point Spread Function (PSF) < 0.8 pixel FWHM (Full Width at Half Maximum), to accurately determine where the photons arrived,
10) As cosmetically defect-free as possible; < 0.1% defective pixels,
11) Ease of use/compact size:
    a. Low pin count; goal < 200 pins,
    b. Integrated read-out electronics with all video processing (including Correlated Double Sampling (CDS), noise

bandwidth limiting, and programmable gain) and digitizing of signal (ADCs) on-chip,

c. Simple digital serial data interface with minimal glue logic to a FPGA,

d. Integral Peltier cooled package for compact size, maintenance free, and minimal support equipment. As a Peltier cooler is not able to remove a large amount of heat at great efficiency, an upper limit on the power consumption of < 5W is imposed on the detector.

To progressively retire risk, a multi-phased development plan was adopted for the development of LGSD in order to have detectors available on time for first light AO systems of the E-ELT in 2023. The phases being: (1) The Design Study which concluded that for the pixel size, format size, and frame rate, the most likely technology to succeed is a monolithic Backside Illuminated (BSI) CMOS Imager, (2) Technology Validation which retired pixel risks, (3) the current phase of designing, building, and testing the Natural Guide Star Detector (NGSD), a pioneering, ¼ sized, scaled down demonstrator, to retire architectural and process risks, (4) The LGSD, the full scale development which should mostly be an engineering exercise, and (5) The Production Run where 30-50 devices will be manufactured.

2. CONCEPTUAL DESIGN OF NGSD/LGSD

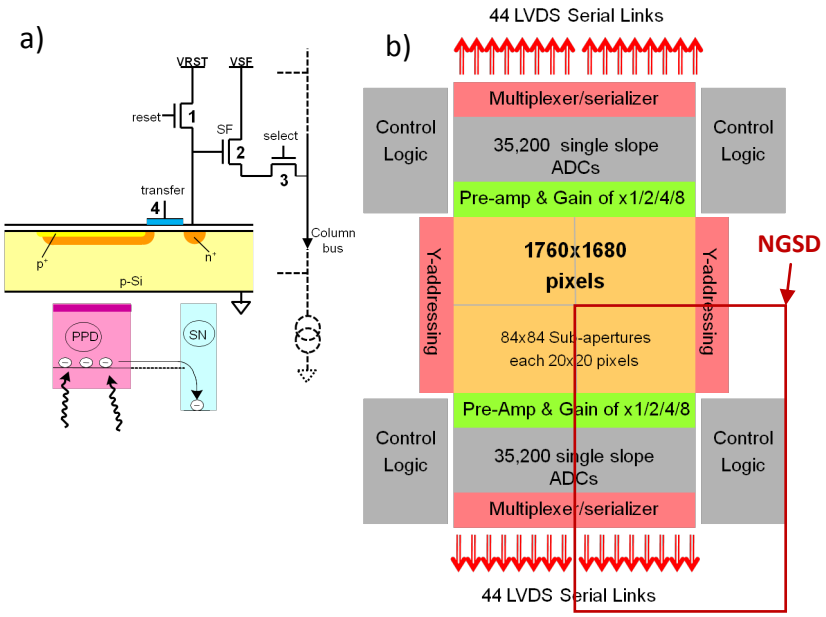

Figure 2-1 : NGSD/LGSD CMOS imager: (a) 4T PPD charge coupled pixels, (b) e2v's conceptual block diagram of the LGSD built using BSI CMOS Imager. The outline of the quarter sized NGSD scaled down demonstrator is shown in red.

Conceptual block diagram (Figure 2-1) of the LGSD (BSI CMOS Imager) consists of a 24µm 1760 x 1680 array of 4T Pinned PhotoDiode (PPD) pixels addressed from either side and read out from both top and bottom. The central 1680x1680 pixels are light sensitive while the outer 40 columns either side will be optically masked and used as reference pixels if required. Many rows of pixels are read in parallel to allow enough processing time per pixel to beat down the noise and the ADCs to digitize the signal. The data is multiplexed and transferred off-chip through high speed LVDS digital interface. Calculations showed little difference in power consumption of including ADCs on-chip as opposed to using high speed analog drivers to transport the signal off-chip. Including ADCs on-chip provides a simple digital interface, and a better chance of achieving and maintaining low noise performance.

Many design trades exist. More rows read in parallel reduce the read noise, but at the expense of longer latency, greater silicon real estate area, longer higher capacitance signal drive lengths, and higher power dissipation. The optimum number of rows processed in parallel was determined to be 40; half each (20) at top and bottom. With forty rows read in parallel at 700fps, the pixel processing time is ~ 34µs. This was demonstrated in the Technology Validation phase to be adequate time to do the video processing and digitize the signal to achieve < 3e- rms read noise while still meeting the low latency requirements.

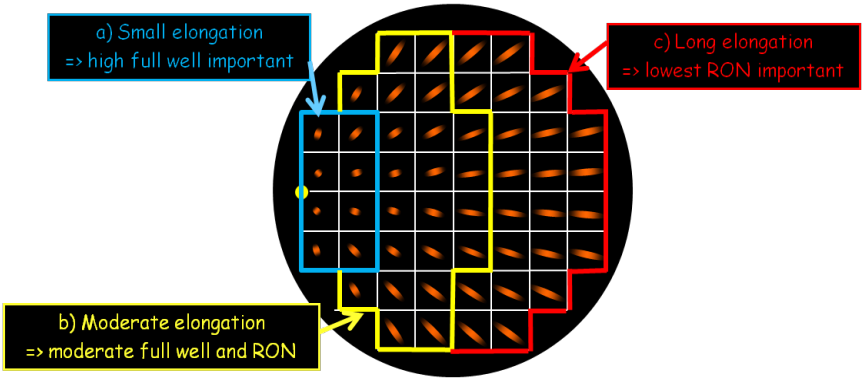

Figure 2-2 : Shows why 9-bit resolution ADCs combined with regions that can be programmed with different gains is an acceptable compromise. Image shows a typical spot elongation pattern for side projected laser. Three different regions are identified: a) region of small elongation where detecting high signal is important, b) region of moderate elongation where moderate signal detector limit and read noise are acceptable, c) region of long elongation where lowest read noise (RON) is important.

In the design of the ADCs, there are trades between: a) the type of ADC, b) the number, c) the conversion rate, d) the silicon real estate area, and e) power dissipation. While several types[3] (cyclic, successive approximation, and single slope) of ADCs have been used in high speed CMOS imagers, a column parallel single slope[4] ADC was preferred for its small size, simplicity, robustness, low noise, and excellent differential non-linearity (DNL). One of the disadvantages of the single slope ADC is the trade between resolution and clocking rate. Each n-bit

ADC conversion requires 2^n clock periods. Complicated techniques such as non-linear[4] and multiple slope[4] ramps have been proposed to overcome this trade. However, by analyzing the LGS spot illumination patterns (Figure 2-2), one notes that apertures close to the laser launch site have the signal contained within a few pixels while those far away have the signal spread over many. An acceptable compromise is to have a 9-bit resolution ADC combined with regions that can be programmed with different gains. Sub-apertures close to the launch site can then be programmed with low gain where detecting high signal is important while those far away can have a high gain where low read noise is more important.

Serial LVDS[2] lines (with no coding) operating at 220Mbit/s were chosen to transfer the data off-chip. Eighty-eight lines are required to handle the 18.6Gbit/s (= 1760 x 1680 pixels x 700fps x 9 bits conversion) bit rate of the LGSD. The NGSD being quarter sized only requires 22. This solution was considered the best conservative trade between the number of package pins, serial data rates, data transmission reliability, and power dissipation. With the proposed use of two supply pins per line, 352 (88*4) package pins will be required for the serial interface in the LGSD. During NGSD evaluation, the possibility of transmitting data at higher bit rates (e.g. doubling to 440MBit/s) will be tested to investigate whether the number of lines and thus pins can be considerably reduced in the LGSD.

3. TECHNOLOGY VALIDATION

Several small devices were built to assess and validate various CMOS technologies, their capability to meet key requirements (especially of image lag, read noise, and speed), and scalability to full-size devices: 1) Arrays of pixel variants were built and tested to compare: a) different geometries and threshold voltages of the pixel transistors, b) the performance of 3T and 4T pixels and whether extra implants in the 4T pixel photodiode could reduce image lag; a measure of how well charge is transferred from the photodiode to the floating diffusion (sense node). Up until this time, very little was known about the image lag performance of large 24µm pixels as most other applications in the literature were interested in much smaller (6µm or less) pixels. 2) In addition, critical elements of the video processing and ADC circuits were tested.

While both 3T and 4T pixel architectures achieved the required performance, 4T pixels were preferred as they only require a single ADC conversion when coupled with an analog CDS (aCDS) circuit, while the former requires two conversions (reset+signal) to implement digital CDS (dCDS). Power consumption and complexity of the ADCs and multiplexer/serial data interface was already considered difficult enough without a doubling of the speed requirements (as in the case of the 3T pixel).

The Technology Validator (Figure 3-1) built by e2v technologies featured 60x60 4T pixels, 1200 (60 x 20 rows read in parallel) single slope ADCs, and a read out speed that is consistent with a frame rate of 700fps in the final device. Measured

[2] LVDS - http://en.wikipedia.org/wiki/Low-voltage_differential_signaling

results clearly validated the 4T pixel CMOS imager approach by reporting read noise of < 3e- rms at the required pixel speed, low image lag of < 0.1%, and good linearity to full well of > 4000e-. Measured pixel conversion gains were in excess of 100µV/e-. The best pixel variant, video processing, and ADC design was selected to go forward to the NGSD phase.

a) b)

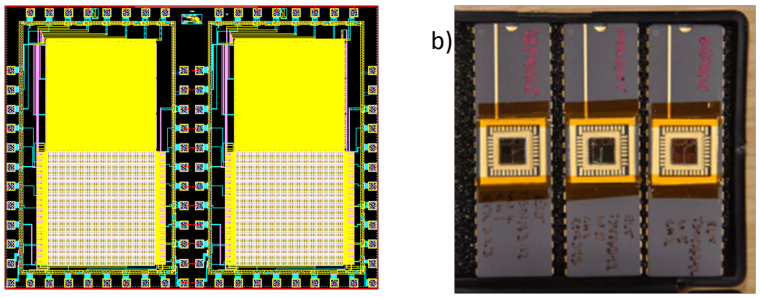

Figure 3-1 : The Technology Validator built by e2v technologies: (a) chip mask layout, (b) Photograph of devices tested. The device featured 60x60 4T pixels, 1200 (60 x 20 rows read in parallel) single slope ADCs, and a read out speed that is consistent with a frame rate of 700fps in the final device.

4. NGSD/LGSD DESIGN

At the start of 2012, the go ahead was granted to e2v, with Caeleste[3] as design sub-contractor, to develop the quarter sized (880x840pixels) NGSD. This development was funded by FP7[5] OPTICON network and the E-ELT Design Study. The purpose of the NGSD was twofold: a) to retire architecture and process risks without the high costs of stitching (required for the final device) or custom Peltier packages; i.e. to be a low cost (relatively) scaled-down demonstrator, and b) to be large enough (> 672x672 pixels) to be able to be used as a detector for first light AO systems on the E-ELT (requiring 8x8 pixels per sub-aperture and 84x84 sub-apertures). The NGSD (see Figure 2-1 for size comparison with LGSD) was designed to meet all requirements of the final full size device, the LGSD, except for the pixel format size.

The reader is referred to Figure 4-1, Figure 4-2 and Figure 4-3 to help with the understanding of the following description of the read out of the NGSD/LGSD. Twenty rows of pixels (one complete row of sub-apertures) are read in parallel at the bottom in the case of the NGSD and at both top and bottom (40 pixel rows in total) for the LGSD. This gives a snapshot shutter effect (time synchronous) within each row of sub-apertures. Each pixel in these 20/40 rows (1760*40 in case of LGSD) is read out through its own pre-amplifier, comparator and double data buffer (Register A and B). The pre-amplifier has four programmable gains of x1, x2, x4, and x8 that can be set on a granularity of a single sub-aperture (20x20pixel sub-array). The comparator and Register A along with the common ramp generator and Gray Code Counter implement the single slope ADC. For pipelining purposes, so that data can be serialized and transmitted off-chip while a fresh sample is taken, the ADC data is copied at the end of the conversion to a

[3] Caeleste, http://www.caeleste.be/

second (shadow) Register B so that it is ready to be serialized during the next sub-aperture read period.

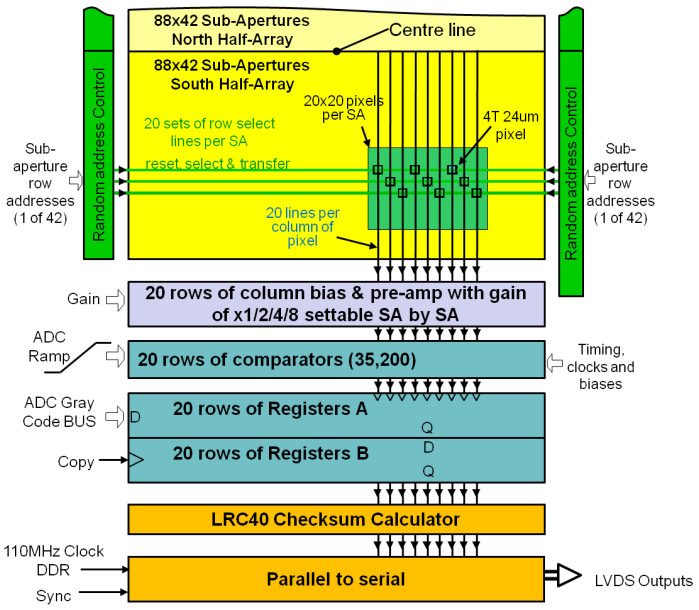

Figure 4-1 : Block diagram of the layout of the read out of NGSD/LGSD.

The pre-amplifier gain, Y-address (sub-aperture row address), and various programmable options of the next sub-aperture to be read are up-loaded through a SPI serial link during the current sub-aperture read. Rows of sub-apertures can thus be addressed sequentially (normal mode) or in any random order (e.g. for reading a sub-region) and gains of each sub-aperture can be independently updated on the fly. For each 40 columns of pixels (width of two columns of sub-apertures), a shift register serializes the 20 rows of pixel data one row at a time using a 110MHz Double Data Rate (DDR) clock, and transmits the data off-chip through one of the 22 (NGSD) or 88 (LGSD) 220MHz LVDS serial links. A 40 bit LRC40 (Longitudinal Redundancy Check[4]) Checksum (detects single bit errors) is calculated each read cycle and can be optionally appended to the data stream.

The LGSD/NGSD have testability built in. Digital test patterns can be generated on-chip to check the serial data transmission and confirm correct operation of the Gray Code counter and associated control circuitry. Special switched bias structures at the top and bottom of the pixel array enable the CDS and ADC to be separately characterized for noise, linearity, monotonicity, and other functional tests. This testability as well as being very important for functional testing and characterizing the detector during development will be available for use to test the operation of the camera electronics during its development and more important to confirm the operation of the camera in the field.

[4] http://en.wikipedia.org/wiki/Longitudinal_redundancy_check

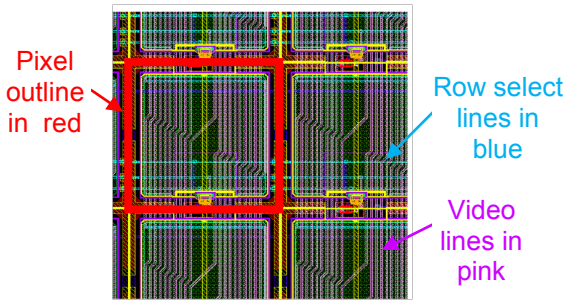

Figure 4-2 : Layout of the pixel showing the three pixel select lines (reset, select and transfer) and the 20 long video lines that run the length of chip up and down from the center lines.

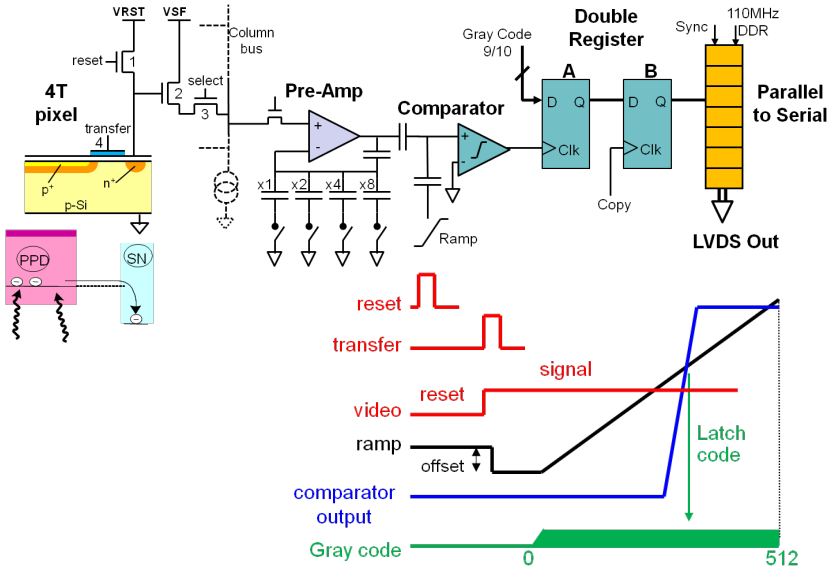

Figure 4-3 : Details of the video processing chain showing pixel, programmable gain pre-amp, single slope ADC (consisting of comparator, Register A, Gray Code counter, and ramp generator), shadow Register B, and serializer (parallel to serial converter).

Further to ensure testability of the NGSD, a Mixed Boundary Scan technique is used to program the possibility of injecting and observing signals at various points in the video chain of a column of pixels. This provides the capability to separately characterize individual components of the video chain, or, if performance issues occur, isolate the fault to a particular component.

The LGSD will be ~ 45mm x 50mm in size and thus will require stitching. The NGSD was sized to fit within a single reticle of 25.5mm x 32.5mm and thus not stitched. Even so the NGSD has been designed with stitching in mind (in order to be a true demonstrator). A tentative stitching plan[6] has been worked out,

however, further work is required before the guidelines imposed by TowerJazz are fully met.

NGSD was manufactured on 18µm EPI layer of high resistivity silicon (1000Ωcm) by TowerJazz using their APD5 0.18µm process with the options of MIM capacitor and 6 layer metal. While warping of the wafer and not achieving the final flatness specification was a consideration (assessed to be within acceptable limits), going to 6 layer metal was thought critical to reduce IR (current*resistance) drops (more, wider, thicker tracks) and thus the possibility of cross-talk between different parts of the design. Half of the wafers were manufactured using the more speculative, but much lower read noise (goal of 1e-), Ultra Low Threshold Transistors in the unit cell. Both types of devices will be tested and the best one selected for delivered devices. Wafers are currently being thinned to 11µm to achieve PSF < 0.8 FWHM, backside treated and AR coated using e2v standard processes.

Wafers will then be diced and glued to a simple but custom 63 mm square, AIN, 370pin PGA package (Figure 4-4) designed to fit a 3M Textool socket style 1357. For temperature monitoring, two AD590MF sensors are glued on the front face at top and bottom close to the die. At the rear in the center of the package, an area as large as practical has been kept free of pins for clamping of a cold finger.

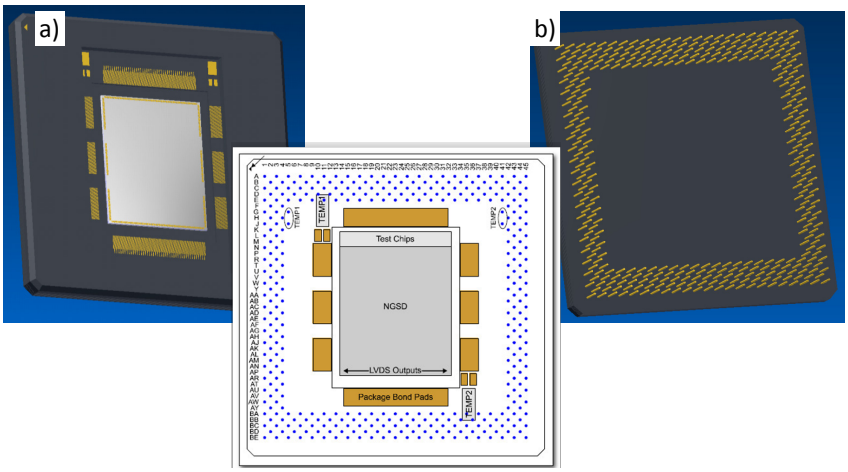

Figure 4-4 : Model of the custom 63 mm square Aluminum Nitride (AIN), 370pin PGA NGSD package, a) front and b) rear view.

Finished BSI devices will be available for testing in Q1 2014. In the interim, one of the process Test Wafers (30 Ωcm) is being diced and packaged and used front-side illuminated to commission the Test Equipment at e2v, check device functionality and do first-light characterization.

To ensure that devices are available for first light of the E-ELT, a possible production run of ~15 NGSD devices is envisaged. Upon successful demonstration of the NGSD, the full scale device will be developed (mainly an engineering exercise by this time) followed by a production run of 30-50 LGSD devices.

e2v has developed a Test Bench to fully characterize the NGSD. In parallel, ESO has built a simple bench prototype for initial assessment of the NGSD using several of the components (detector boards) developed by e2v for their Test Controller. Meanwhile a more substantial camera[7] that can be used at the telescope is being developed with first prototype scheduled to be available for device testing late 2014. As part of FP7, the same team[5] that successfully commercialized OCam for the CCD220 is developing a camera[8] for NGSD.

5. CONCLUSION

BSI CMOS Imager has been identified as the best technology to fulfill the requirements of the LGSD. Measured results of < 3e- read noise at speed, good image lag and linearity have clearly validated the CMOS imager approach. ESO has formed a good partnership with e2v and Caeleste to develop the NGSD/LGSD. The first generation, quarter-sized, 880x840 pixels NGSD has come out of production and is in the process of being thinned, backside processed, diced and packaged. Front-side devices will be available within the next month for testing with BSI devices available Q1 2014. ESO is well advanced in its camera development.

6. REFERENCES

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