Optimization and Deployment of the e2v L3-Vision CCD220

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ABSTRACT

From concept to reality, 15 AO WaveFront Sensing cameras (code named AONGC) have now been delivered to the ESO VLT SPHERE[3] and AOF[4] meeting all minimum requirements, and in most cases, the goals as well. Another three are requested for ERIS[5]. AONGC uses the compact packaged Peltier cooled 1500fps 240x240 pixels L3-Vision (for < 0.1e- read noise) CCD220 custom developed by e2v technologies on behalf of ESO and OPTICON.

Presented are test results and more important the optimizations performed including amongst others the trade between spatial performance of PSF and dark current and how "intrinsic dithering" enables a better trade to be found especially for devices made in thicker Deep Depletion silicon (for better red response); the optimization of the PID controllers in the feedback loop of the resonant circuit of the HV clock design; the investigation into improving serial CTE; and the reduction of fixed pattern and read noise whereby now the manufacturer's design targets of read noise and dark current are routinely achieved.

In the near future, further work will be carried out to increase the frame rate of the camera to goal of 2500fps in order to extend its use to XAO for the E-ELT.

1. INTRODUCTION

ESO has a long history of developing custom devices to meet the demanding requirements of Adaptive Optics (AO) WaveFront Sensing (WFS). Detectors with the required combination of fast frame rate, high quantum efficiency, low read noise, and large number and size of pixels are not available off the shelf and thus specialized custom developments are necessary.

From concept to reality, 15 AONGC cameras are in an advanced stage of acceptance for use on 2nd Gen. VLT instruments and another three are in production for ERIS[5]. AONGC uses the 1500fps, 240x240 pixels, ultra low read noise (< 0.1e-) CCD220 developed by e2v technologies on behalf of ESO and OPTICON.

This paper reports not only on the impressive test results, but more important the optimizations: a) how Tri-Level clocking and "intrinsic dithering" allowed a

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[5] http://www.eso.org/sci/facilities/develop/instruments/eris.html

better trade between PSF and dark current; b) how the stability of the HV clock generator was much improved by replacing the integrator in the feedback loop with a properly designed PID; c) how serial CTE was improved.

2. DEPLOYMENT OF CCD220 ON VLT INSTRUMENTS

ESO and OPTICON[1] funded e2v to develop a compact Peltier cooled sensor, the CCD220, to meet the requirements of WFS for 2nd Generation of VLT instruments (SPHERE, ERIS, AOF – MUSE and HAWK-I).

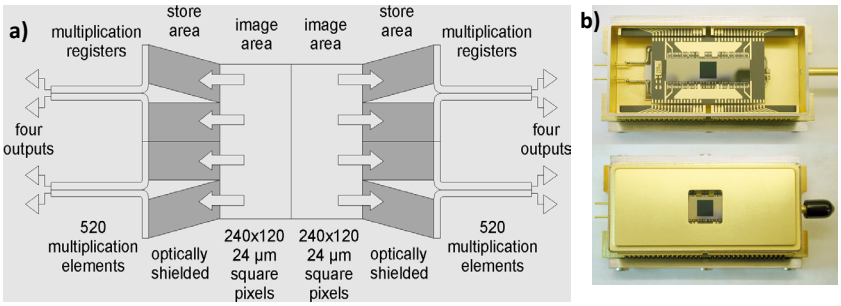

Figure 2-1 : a) Schematic of e2v 240x240 pixel L3Vision CCD220. Eight L3Vision registers enable sub electron noise at frame rates of 1500 fps. b) Photograph of CCD220 package.

The CCD220[2][3] (Figure 2-1) is a 24 µm square 240x240 pixels split frame transfer back illuminated L3Vision CCD. The image and store area (store is optically shielded) are built with 2-phase metal-buttressed parallel clock structures to enable fast line shifts in excess of 7 Mlines/s for total transfer time from image to store of 18 µs and low smearing (when run shutterless) of under 2% at 1,200 fps. Eight electron-multiplying L3Vision gain registers operating at greater than 13 Mpixel/sec enable sub electron noise to be achieved at frame rates beyond 1,500 fps. With a measured output amplifier read noise of 60-70e- at unity gain and L3Vision gain of 1000 applied, an overall effective read noise < 0.1 e- (70 e- RON/1000) is possible. The CCD220 is encapsulated in a 64 pin integral Peltier package (Figure 2-1b) that can cool the CCD below -50°C to achieve the requested < 0.05 e-/pix/frame dark current at 100fps and above.

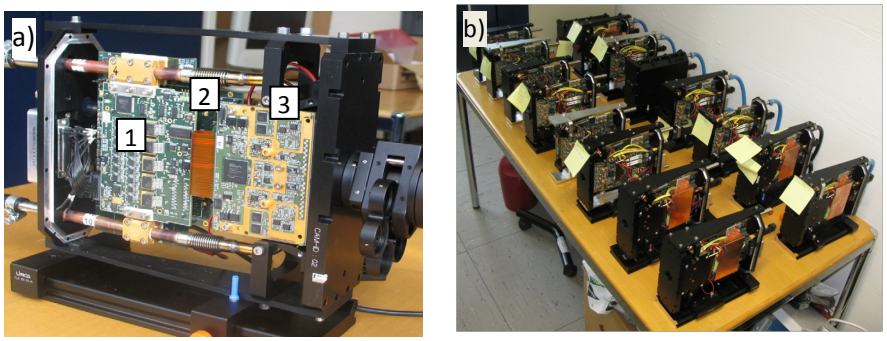

Figure 2-2 : a) Photograph of AONGC with covers and radiation shields removed: 1) Bias, 2) Main, and 3) Analog Front End boards; b) Photograph of assembled cameras.

To deploy the CCD220, ESO has developed the AONGC[4] camera. While the majority of AONGC (Figure 2-2) was developed in-house, the Analog Front End board was developed in collaboration with Flight Light Imaging[6]; the company set up to commercialize the OCam camera. Production run of 25 AONGC is nearly completion (Figure 2-2b) with many cameras already delivered to AOF and SPHERE and the rest by Q1 2014.

The exceptional performance shown in Table 2-1 is now routinely achieved. All expectations are met. Previous reported problems of high Dark Fixed Pattern and read noise have now been fixed with improved board layout and design of the HV Clock generator. The e2v L3Vision register requires a HV Clock of up to 50V switching at pixel rate.

Table 2-1 Performance of science grade "standard silicon" and "Deep Depletion" e2v CCD220 routinely met with AONGC cameras.

Requirement	Measured Result	Specification
Frame Rate (fps)	> 1500	>1200
Read noise at gain of 1000 and 1500fps	< 0.1e-	< 1.0e-
Image Area Full Well (e-)	> 160k	>5,000
Serial Charge Transfer Efficiency	0.99999	> 0.9998
Cosmetic (number of traps, bright, and dark defects)	0	< 25
Dark Current at 1200fps and -40ºC (e-/pixel/frame) Dark Current at 100fps and -50ºC (e-/pixel/frame)	< 0.02 < 0.05	< 0.05

3. DEEP DEPLETION CCD220

As well as standard silicon (StdSi) devices, more speculative, thicker (40µm), Deep Depletion silicon (DD) devices were manufactured. The later provide much sought after higher (75 % improvement Figure 3-1) Quantum Efficiency (QE) in the "red" for instruments that use Natural Guide Star (NGS) WFS such as SPHERE, ERIS, and AOF tiptilt.

AO WFS requires good spatial performance of PSF < 0.9 pixel FWHM over the wavelength of 460 to 950nm. While there is no question of meeting this specification with the StdSi device (Figure 3-4b), the DD device has potentially worse PSF due a larger undepleted region at the back of the CCD as a result of: a) its extra thickness (40 µm versus 13 µm), and, b) the inclusion of a necessary buried p-layer implant to ensure the correct operation of the L3Vision gain register when built on high resistivity silicon. The implant acts as a barrier to the electric fields of the image area clocks reducing their penetration depths.

If the DD device is simply run into inversion for lowest dark current during charge integration like with the Standard Silicon device, poor PSF results (see slit image of IntegVolt=-8V in Figure 3-2). If on the other hand, the high level of the image area clock is used to integrate charge, Clock Induce Charge (CIC) and dark current becomes excessive. When operated out of inversion, surface dark current dominates and is two orders of magnitude higher.

[6] Flight Light Imaging - http://www.firstlight.fr/

The solution is to use Tri-Level clocking (Figure 3-3) to provide greater flexibility in optimizing the clock voltages to obtain the best trade between PSF, CIC and dark current:

a. a Very High Level, VHL, for integrating charge to achieve the desired PSF.
b. a High Level just right for good charge transfer and low CIC.
c. a Low Level that takes the device into inversion once per frame to reduce the dark current by a technique known as "intrinsic dither mode"[5]. At low temperature and fast integration times, the trap-release time constants are long enough such that holes will not have time to travel away from the surface through the column channel stops to substrate. By taking the device into inversion once or a few times per frame, close to inversion dark current becomes possible.

Measured results (Figure 3-2 and Figure 3-4) of PSF versus wavelength at different collection phase voltages of the DD CCD220 shows that the PSF improves substantially as the collection phase voltage (the VHL of the Tri-Level clocking) is increased. At VHL > +2V, minimum specification of 0.9pixel FWHM is reached, and, at VHL > +8V, goal of 0.55pixel is possible.

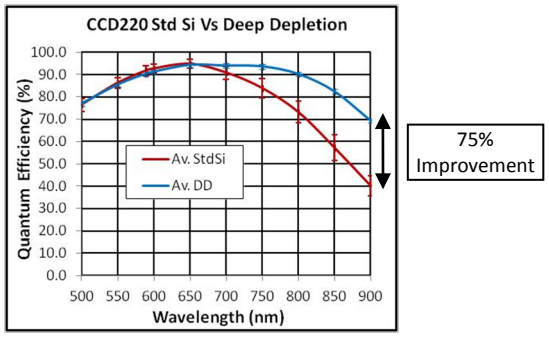

Figure 3-1 : Measured average QE (e2v) of the 16 StdSi and 4 DD CCD220s. The >75% higher QE in the "red" illustrate why the DD devices are highly sought after.

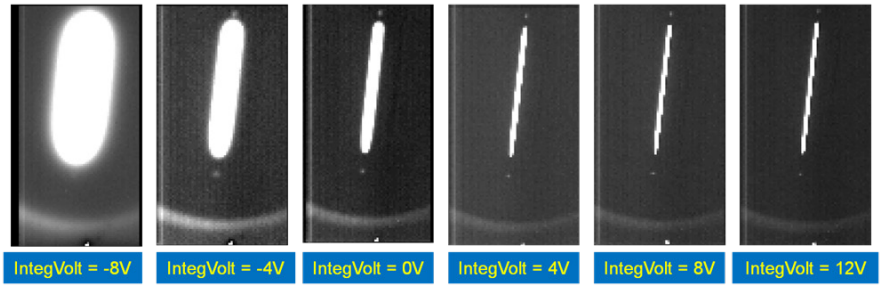

Figure 3-2 : Images of a narrow slit projected onto a Deep Depletion CCD220 at different collection phase voltages (IntegVolt) from -8V to +12V at wavelength of 660nm.

Measured results of dark current VHL (collection phase voltages) is varied for frame rates of 1200fps, and 100fps show: a) Dark current of the DD device when run into inversion (VHL < -8V) is only slightly higher than the Standard Silicon device; b) Dark current does increases as the device is taken out of inversion

during integration, however, once out of inversion (VHL > -4V), dark current does not increase further as VHL is further increased; c) at 1200fps, dark current only increases a little when the device is run out of inversion indicating that at this frame rate, dark current is mostly dominated by CIC; d) at 100fps, dark current only quadruples. At this frame rate, dark current should be dominated by surface channel and be two orders of magnitude higher if not for “intrinsic dithering. This clearly validates this approach.

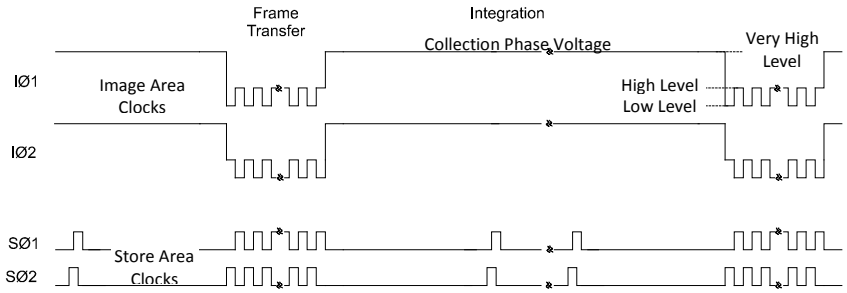

Figure 3-3 : Timing diagram of the implemented Tri-Level clocking of the image area which allows a much better trade between PSF, CIC and dark current to be found.

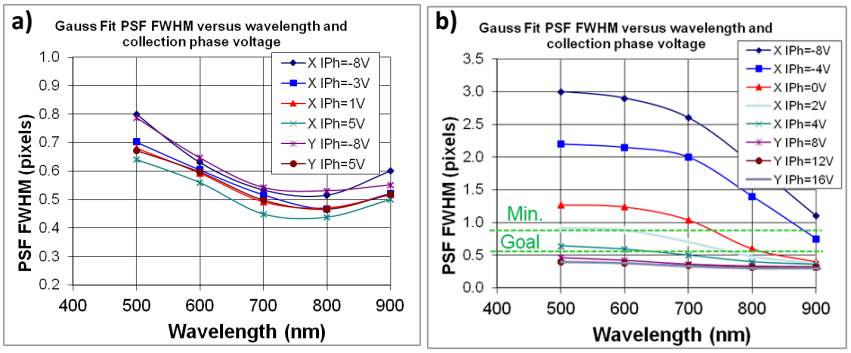

Figure 3-4 : Measured results of PSF versus wavelength as the collection phase voltages (IPh) is varied for a) Standard Silicon and b) Deep Depleted CCD220.

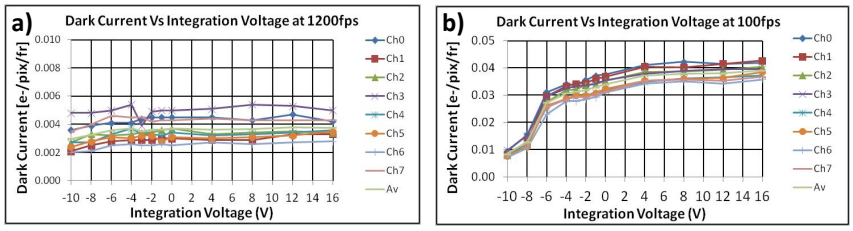

Figure 3-5 : Plot of dark current, at frame rates of a) 1200fps and b) 100fps, for individual channels and the average of Deep Depletion CCD220 at gain of 1000 as VHL (Integration Voltage) is varied.

4. IMPROVEMENT TO THE DESIGN OF THE HV CLOCK

The e2v L3Vision gain register requires a HV Clock at pixel frequency (12MHz and beyond) whose amplitude can be programmed to vary from 20V up to 50V in order to change the gain from unity to 1000 over the lifetime of the device. This can be either a square or sine wave. A common simple low power method of implementing this HV clock is to use a resonant circuit as depicted in Figure 4-1 to generate a HV sine wave. The design consists of a) a LC resonant circuit tuned to the pixel frequency; the L is the inductance of the transformer and C is the combination of the capacitance of the CCD phase and an external (trimmable) capacitor; b) a switch that controls the clock phase and excites the resonance circuit to oscillate at the pixel frequency; c) two feedback circuits to stabilize the high and low levels of the sine wave by integrating on and correcting for the difference between the measured peaks and the desired voltage.

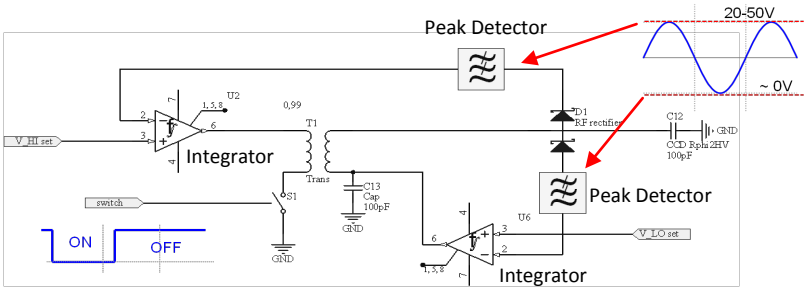

Figure 4-1 : Original design of the HV Clock; simple integrators used in feedback circuits.

The problem with this design is that the gain of the L3Vision register is observed to vary during the read out. This is clearly evident when comparing Flat Field images with and without gain. With unity gain, the Flat Field image is very flat (Figure 4-2a), however, with gain applied (x200), the signal level of the image varies during the read out (Figure 4-2b). Observing the HV clock during readout with an oscilloscope, the high and low levels of the sine wave are seen to vary in a way consistent to that of the column plots of the Flat Field and the variation increases with illumination level.

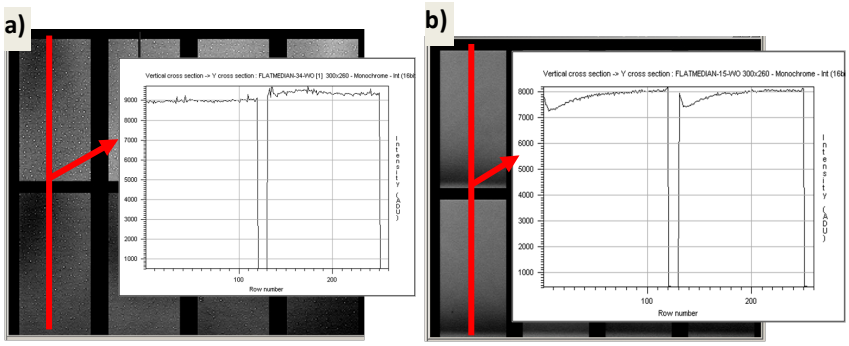

Figure 4-2 : Images and column plot of Flat Fields at unit and gain of 200. With gain, the Flat Field is not flat and varies during read out.

To understand what is happening, the complete design of the HV clock was simulated using a spice simulator, SiMetrix[7]. The transformer was modeled in spice by extracting the scattering parameters measured by a Vector Network Analyzer as described in [6]. Results of both measurements and simulations show: a) excellent agreement between the simulations and hardware; b) the resonance circuit is very sensitive to any change in the load. The load (the CCD HV clock phase) changes during read out due to changes in the clock inter-capacitances; c) the circuit has far too slow response (Figure 4-3) to a transient disturbance which needs to be improved.

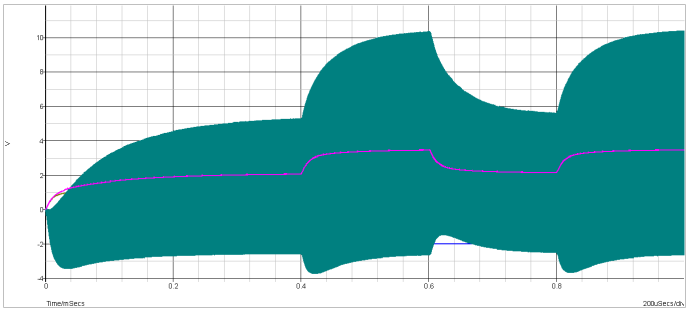

Figure 4-3 : Slow step response of the original design (Figure 4-1) of HV Clock generator.

To improve the transient response of the HV clock, the two integrators in the feedback circuits were replaced by full PID controllers (Figure 4-4). The optimal values of the PID terms were determined using the spice simulator. This provided the advantage of being able to use a multi op-amp design to independently and separately adjust the PID terms as opposed to the much more restrictive single op-amp design of the final hardware implementation. This is a common approach to solve this type of problem. Once optimal values were obtained by trial and error, a single op-amp design with equivalent frequency response was easily found and implemented. Figure 4-5 compares the step response of the simulated circuit and the final hardware (oscilloscope trace of HV clock). Both are very similar and show the much improved transient response. The "proof of the pudding" is shown in Figure 4-6; a very much improved Flat Field image with gain.

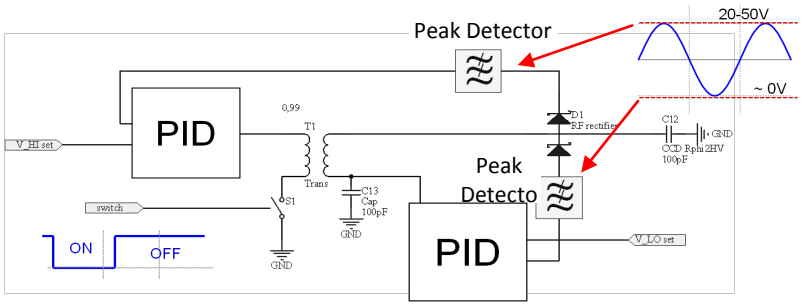

Figure 4-4 : Design of HV Clock improved by replacing integrator by PID controller.

[7] http://www.simetrix.co.uk

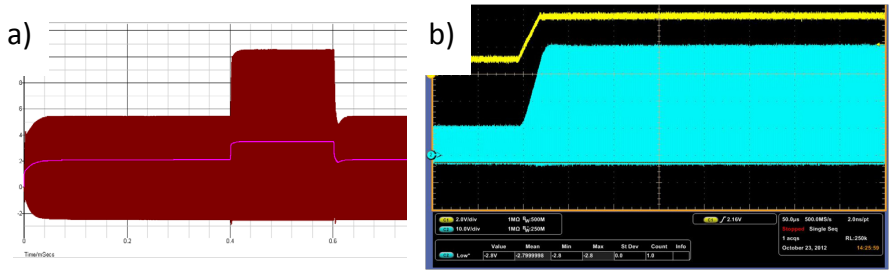

Figure 4-5 : Much faster step response of the improved design (Figure 4-4) of HV Clock generator; a) results of simulation; b) design implemented and measured by oscilloscope.

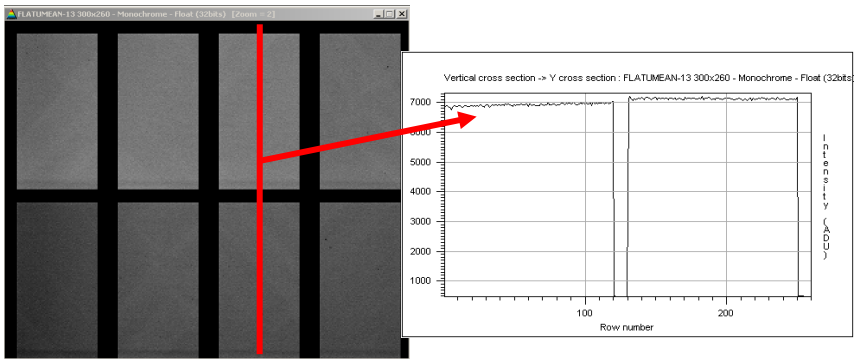

Figure 4-6 : "Proof of the pudding", Column plot at gain of 200 shows very little variation of the Flat Field during read out. Note that the Flat Field is averaged over 500 frames.

5. SERIAL CTE – THE LONG TAIL OF RESIDUAL CHARGE

The CCD220 when L3Vision gain is applied exhibits a long tail of residual charge (Figure 5-1). This is currently typical of this technology. A special technique of: a) reverse clocking the serial register so that all charge from the line transfer is summed into a single pixel at the start of the serial register; and b) read out the full line in the forward direction, was developed to observe the response of the L3Vision register to a delta function.

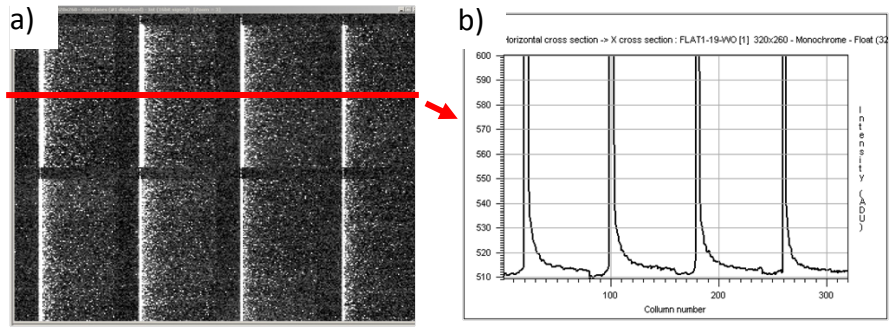

Figure 5-1 : a) Image showing the long tail of residual charge in the serial register direction when multiplication gain is applied. Charge is summed into a single pixel by reverse clocking the serial register after the line transfer and before reading out.

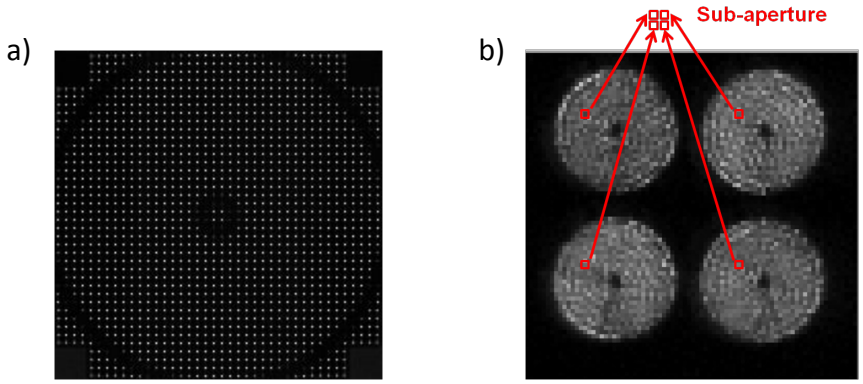

Figure 5-2 : Typical illumination patterns of a) Shack-Hartmann and b) Pyramid WFS systems.

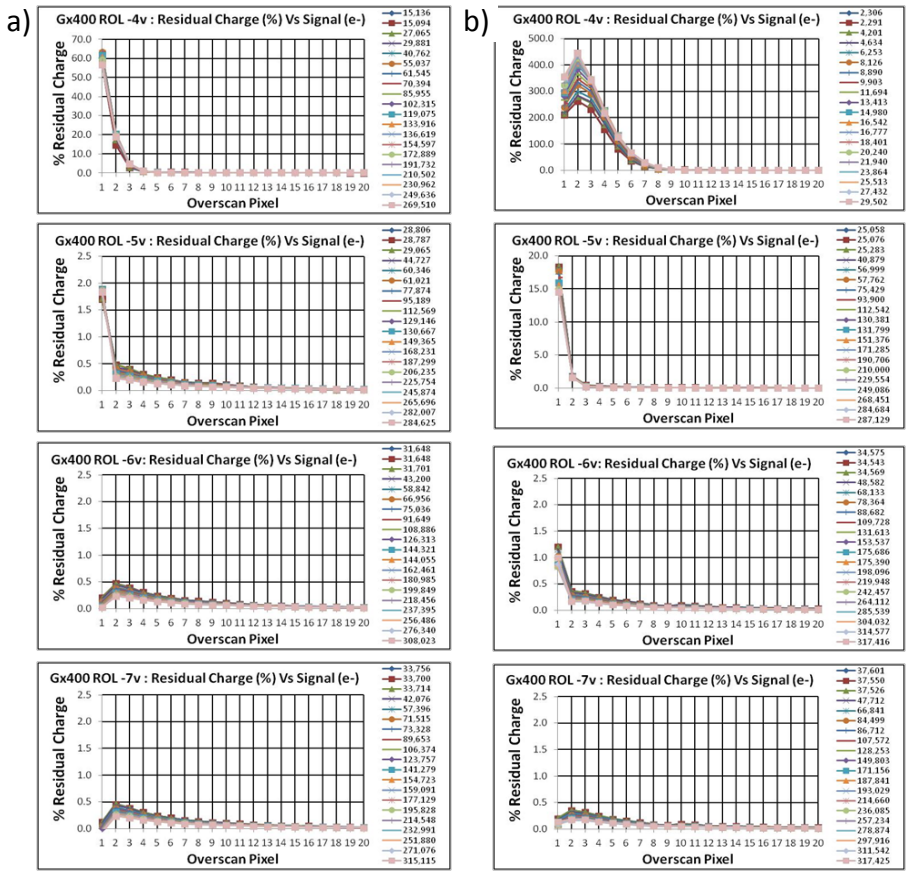

Figure 5-3 : Line plots of % residual charge for different signal levels at gain of 400 as serial clock low voltage, ROL, is varied for the a) best; and b) worse amplifier.

For the original application of Shack-Hartmann WFS (Figure 5-2a), the less than ideal SCTE of the CCD220 was not considered an issue. As long as the SCTE does

not vary much with signal level then it will appear as a simply fixed offset in the centroid of the spots that can be corrected; in reality it just simply calibrates out. However, with pyramid WFS, any residual charge will appear as cross-talk into its neighboring sub-aperture (Figure 5-2b) thus it is important for the residual charge to be low and to be safe to be < 1% of the signal.

An investigation into how to improve SCTE concluded that the low voltage level of the serial clocks (ROL) was the most sensitive parameter. Plots (Figure 5-3) of the % residual charge in the trailing (overscan) pixels for different signal levels clearly shows an improvement in the transfer efficiency as ROL is reduced and taken into inversion. It was further observed that CIC in the serial register does not increase significantly as it is driven into inversion. This is a welcomed but not totally unexpected result. It is highly likely due to the high speed clocking of the serial register and the holes that populate the surface during inversion not having time to move away [5]. Surface dark current also decreases dramatically as the register is clocked into inversion; however, as charge spends little time in the serial register, dark current from the serial register is already a non-dominating factor. The decrease of residual charge as the serial register is clocked into inversion tells us something about where the charge is trapped, and that is, the charge must be trapped in long lived surface states at the $Si\text{-}SiO_2$ interface.

To ensure that low level signal (single electron) is being properly transferred and detected, the set up (voltages and timing) of the output amplifier and the serial register was optimized by maximizing the amount of CIC and dark current seen in the image area. This guarantees that all charge is being detected.

6. CONCLUSION

This paper has reported on the characterization and optimizations performed on AONGC to extract the best performance out of the CCD220. With these improvements, manufacturer's design targets (performance goals) are routinely exceeded ensuring the success of these cameras and the success of AO systems on VLT 2nd generation instruments.

7. REFERENCES

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