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Organisation Européenne pour des Recherches Astronomiques dans l'Hémisphère Austral

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VERY LARGE TELESCOPE

New General Detector Controller (NGC)

Technical Report

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Prepared:	M.Meyer		
	Name	Date	Signature
Approved:	D.Baade		
	Name	Date	Signature
Released:	A.Moorwood		
	Name	Date	Signature

CHANGE RECORD

Issue	Date	Affected Paragraphs(s)	Reason/Initiation/Remarks
1.0	23/08/2004	All	First version
1.1	08/03/2006	All	Board REV1

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PURPOSE

This document describes operation of the New General Detector Controller REV1 hardware. It gives an understanding of the basic operation, tells about the implemented firmware and is also intended as a programmers guide for software evaluation.

Reference Documents

VIRTEX-I I Pro Platform FPGA Handbook	Xilinx

Links

FPGA	http://www.xilinx.com
ADC, DAC	http://www.analog.com
Printed Board	http://www.andus.de

List of Abbreviations/Acronyms

ADC	Analog to Digital Converter
AQ	Data Acquisition
DAC	Digital to Analog Converter
DFE	Detector Front-End Electronics
DBE	Detector Back-End Electronics
DMA	Direct Memory Access
FPGA	Field Programmable Gate Array
FIFO	First in First out Memory
IRACE	Infrared Array Control Electronics
IRQ	Interrupt request
NGC	New General Controller
RTC	Real-time Computer
Rx	Link Receiver
RxTx	Link Transceiver
Tx	Link Transmitter

1 INTRODUCTION

NGC is modular system consisting of the back-end module with PCI based connection to the data acquisition computer and the front-end module(s), creating and receiving detector signals. Data and control signals between back-end and front-end modules are on fiber-optic link(s) with transmission rates of 2.5 GBit. The modularity of the system allows many combinations as multiple back-ends or multiple front-ends or combinations as desired.
Emphasis is given to low power dissipation, what is mainly important for the front-end unit to allow operation without cooling units. A four channel system on one card of standard VME 6U size consumes less than 10 Watts. Add on cards are 32 video channel modules on a board of the same size and additional ~10 Watts of power consumption.
No processor on the front-end side is implemented. The data acquisition computer can address all front-end functions over the fiber link. Result is a quiet system without difficult to control processor bus activity during data acquisition.
There is no parallel video or communication data bus on the front-end. All data and communication transfer runs over high speed serial links with transmission rates of 2.5 GBit/s. Result is minimum disturbance for the anticipated low noise operation on the low level detector signals.
All voltages for clocks and bias of the detector are remotely programmable also during readout of the detector to allow maximum comforts for evaluation and test.
Digital galvanic isolated outputs for shutter, wobbling mirror and markers are provided and the system can accept a trigger input for synchronizing the detector read-out to external events.
Monitors for video and clocks are on front-panel connectors for evaluation and maintenance.
All detector bias voltages and currents can be measured with the implemented telemetry system.

A minimum number of different components are used, glue logic is not needed due fact that all digital logic is implemented in high density FPGAs. Only one type of FPGA, the VIRTEX-I I Pro type 2VP7 FF 672 from XILINX with 672 pins is used.
All this makes maintenance easy and reliability high.
The system will not require active cooling.

2 OVERVIEW

2.1 Block

There are two main groups of modules connected by fiber duplex connection :

- The Detector Back-End Electronics.
- The Detector Front-End Electronics consists of the Basic Module(s) and if needed additional AQ modules. These are interconnected by high speed serial links on copper for command and data transfer.

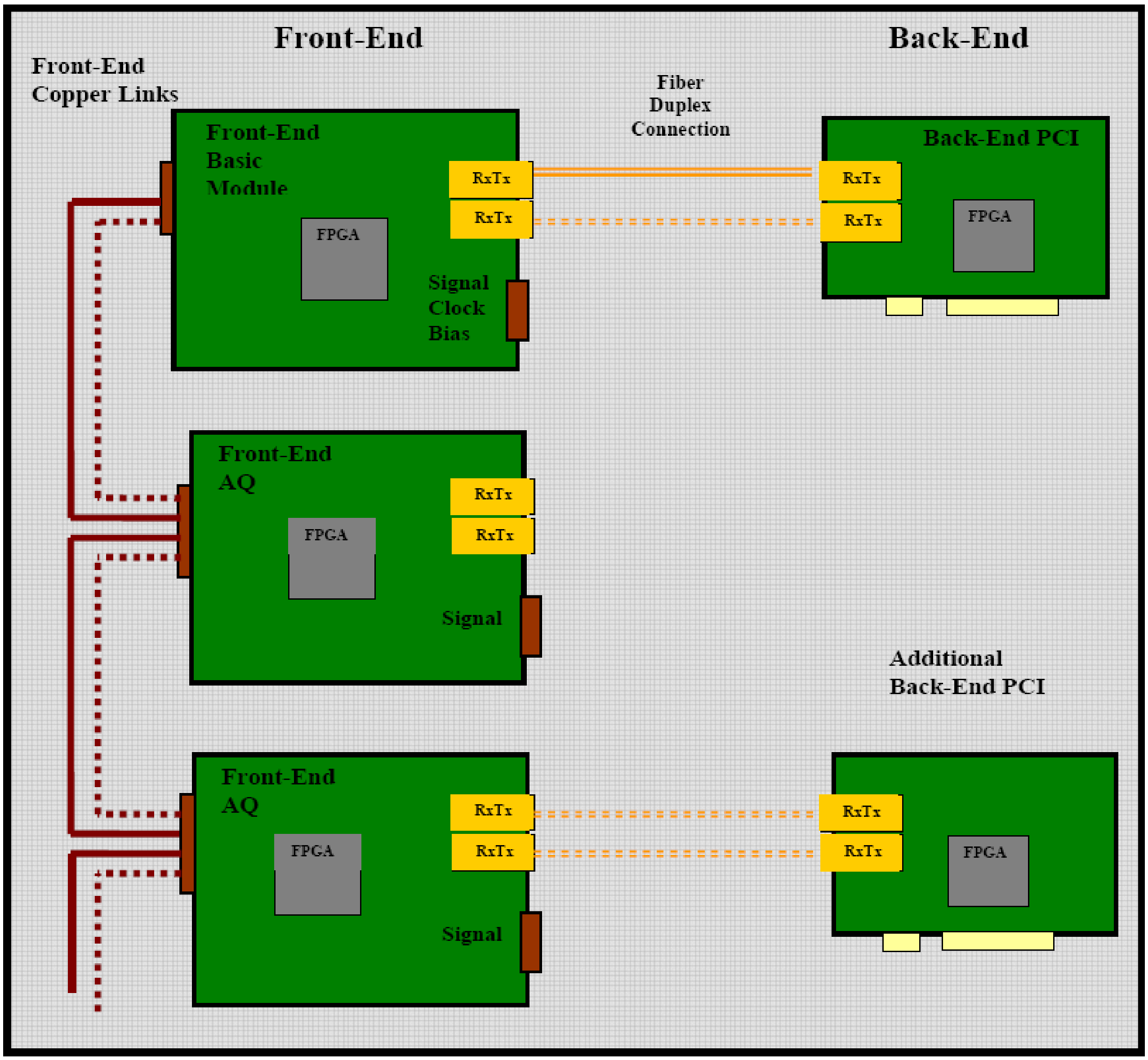

Fig. 1 System Block

The basic link configuration is the linear connection of modules. Commands are routed always from the Back-end to the first Detector Front-End Electronics module. Additional DFE modules are addressed by wormhole routing through previous modules. The same happens for answers or video data from DFE modules to DBE modules. If more bandwidth is needed two links in parallel can be used (needs different IP on FPGA).
Additional functionality can be provided if frames of video data are routed directly out of AQ modules to additional receivers, e.g. PCI based DBE's.

2.2 Minimum DFE System – Basic Board with Backplane and Backboard

A complete DFE consists of the main board(s), the backplane and the backboard(s).
The backplane establishes the inter board connections.
The backboard sets up the connection to external functions like clocks, biases, video inputs and fiber links. In addition the back board can hold special functionality not implemented in the main board.

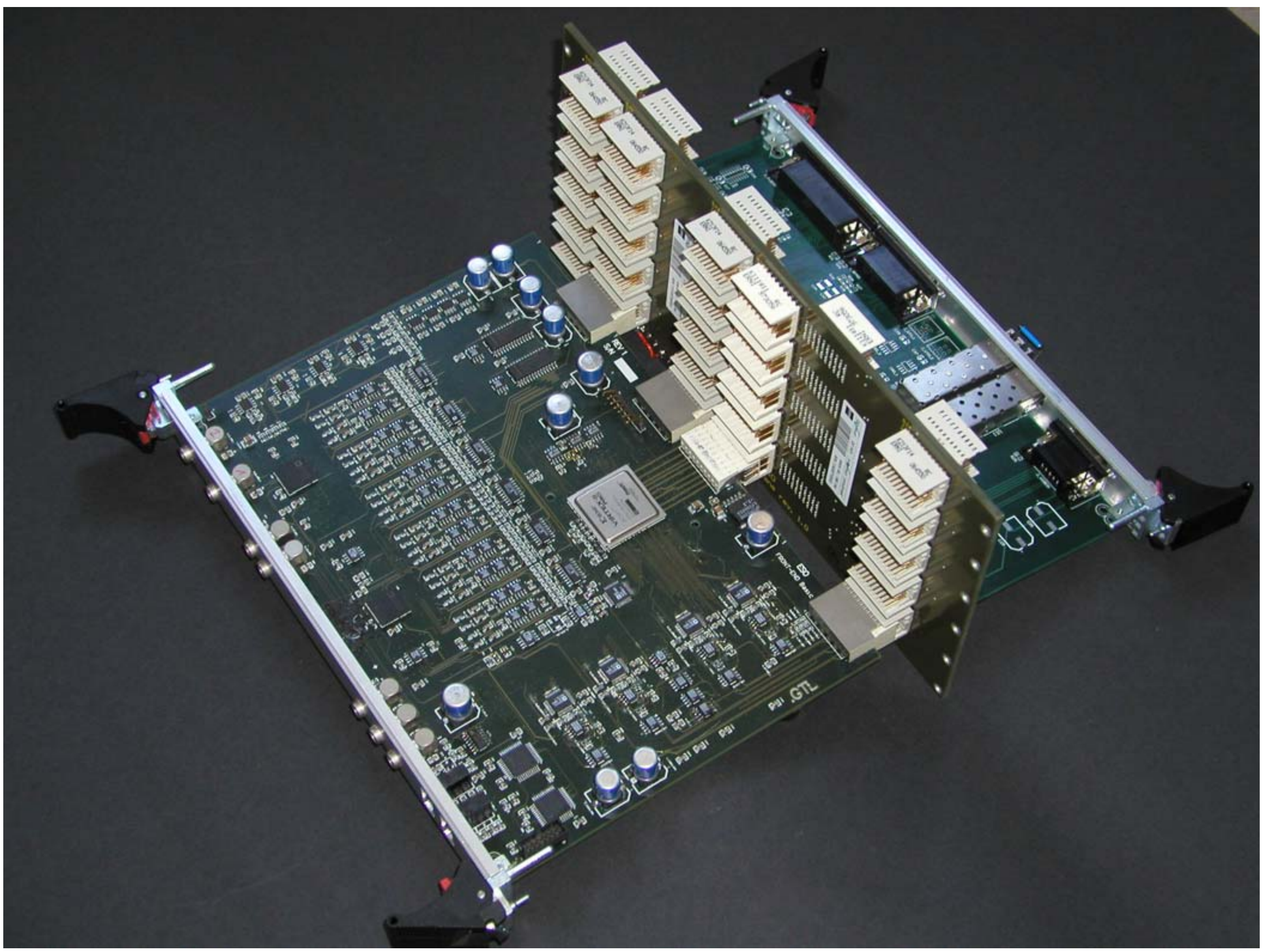

Fig. 2 NGC System with Basic Board, Backplane and Backboard

2.3 Back-end

- Back-End PCI is a module with connection to a 64 Bit PCI bus.
- Function is based on the XILINX Virtex Pro FPGA XC2VP7 FF 672 .
- A PCI master/slave interface with scatter/gather DMA is implemented.
- The slave IF is used for communication.
- The master IF is used for video data DMA transfers to PCI.
- Two RocketIO transceivers (2.5 GBit each) are used for Communication and data transfers, other options to increase bandwidth are possible (one FPGA contains 8 transceivers – space limit for PCI card size might be four).

Fig. 3 PCI Back-End

2.4 Front-End

2.4.1 Basic Module

The front-end Basic Module is based on the XILINX Virtex Pro FPGA XC2VP7 FF 672. Main functions of this module are

- **Communication**
- **Video data transfer**
- **Sequencer**
- **DAC voltage generator for clock and bias**
- **Clock drivers (16 clocks)**
- **Bias drivers (16 biases)**
- **Four data acquisition channels (can be installed with either 16 or 18 Bit ADC's)**
- **Telemetry**
- **Clock monitoring**
- **Video monitoring**

- ➢ Communication and data transfer to the back-end is handled with the FPGA's 3Gigabit transceivers.
- ➢ The sequencer is completely contained within the FPGA. The digital clock driver lines of the sequencer connect without glue logic to the clock driver switches.
- ➢ The ADC outputs of the four acquisition channels connect without glue logic to the FPGA due to the high pin count available there. Used ADC's are the AD76xx types from Analog Devices. The preamplifier input is fully differential
- ➢ Input range is +/- 2.5V within 0 to 3V if 16 Bit ADC's (AD7677) are installed
- ➢ Input range is +/- 4.0V within 0 to 5V if 18 Bit ADC's (AD7641) are installed.
- ➢ There is no clamp/sample implemented in the analog chain.
- ➢ Connection to additional multi channel AQ modules is over the backplane by copper with the high speed links of the FPGA.
- ➢ Telemetry of biases and clocks.
- ➢ Two independent Monitors for clocks.
- ➢ Monitor for video signals.

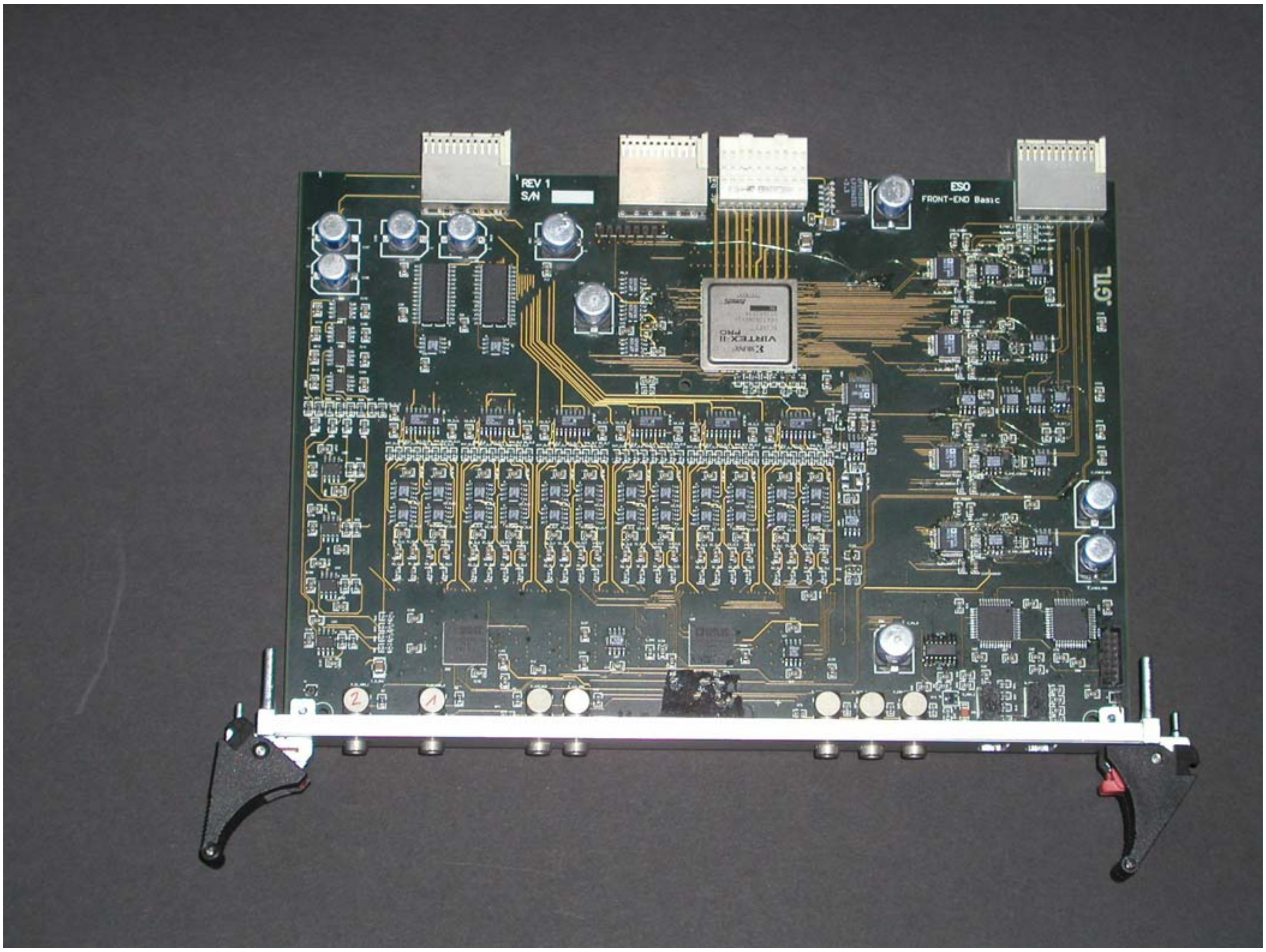

Fig. 4 Front-End Basic Module

2.4.2 AQ 32 Module (16 Bit)

The front-end AQ Module is based on the XILINX Virtex Pro FPGA XC2VP7 FF 672. There are 32 acquisition channels on 16 Bits.

- ADC outputs of the acquisition channels connect with little glue logic on a bus structure to the FPGA.
- ADC's are the AD7677 types from Analog Devices.
- The preamplifier is fully differential, input range is +/- 2.5V. There is no clamp/sample implemented in the analog chain.

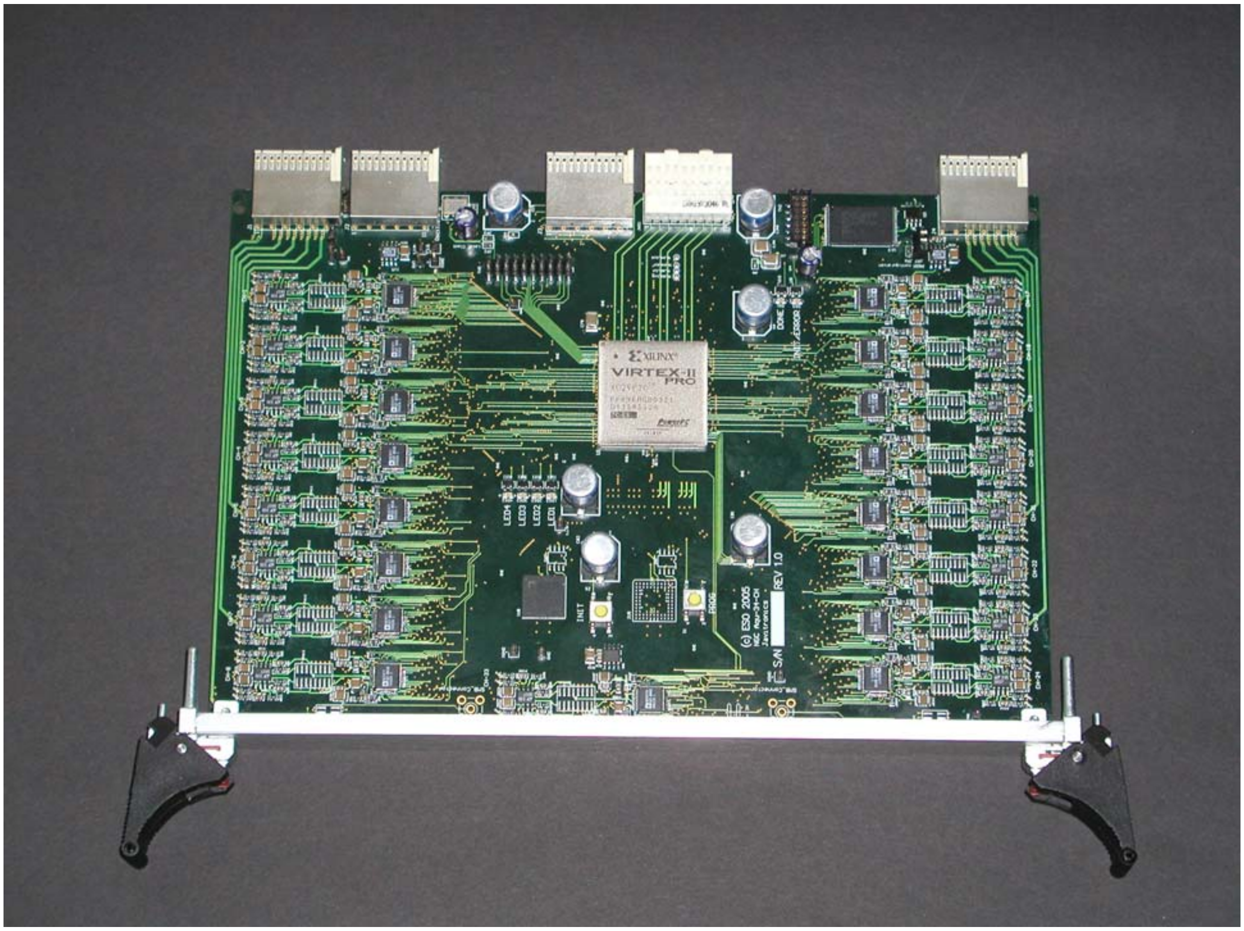

Fig. 5 Front-End Basic Module

2.4.3 AQ Module (18 Bit)

The18 Bit version is on the basis of the 16 Bit AQ module. Same layout and printed board only different ADC's installed.
ADC's are the AD7641 from Analog Devices
The preamplifier is fully differential, input range is +/- 4.0V. There is no clamp/sample implemented in the analog chain.

3 FUNCTIONAL DESCRIPTION

3.1 High Speed Links

Data transfer and communication works purely on serial links. The link architecture is determined by the connections on the backplane, the use of back panel external links and the firmware in the FPGA.
The standard configuration has one link to the Back-end (Back panel fiber) on the first slot and one link from each module downstream to the next.
If more bandwidth is required, a second link parallel to the standard configuration links can be implemented. Even more bandwidth and computing power is provided, if additional data channels are routed from Back panel fiber connections to further PCI interfaces.

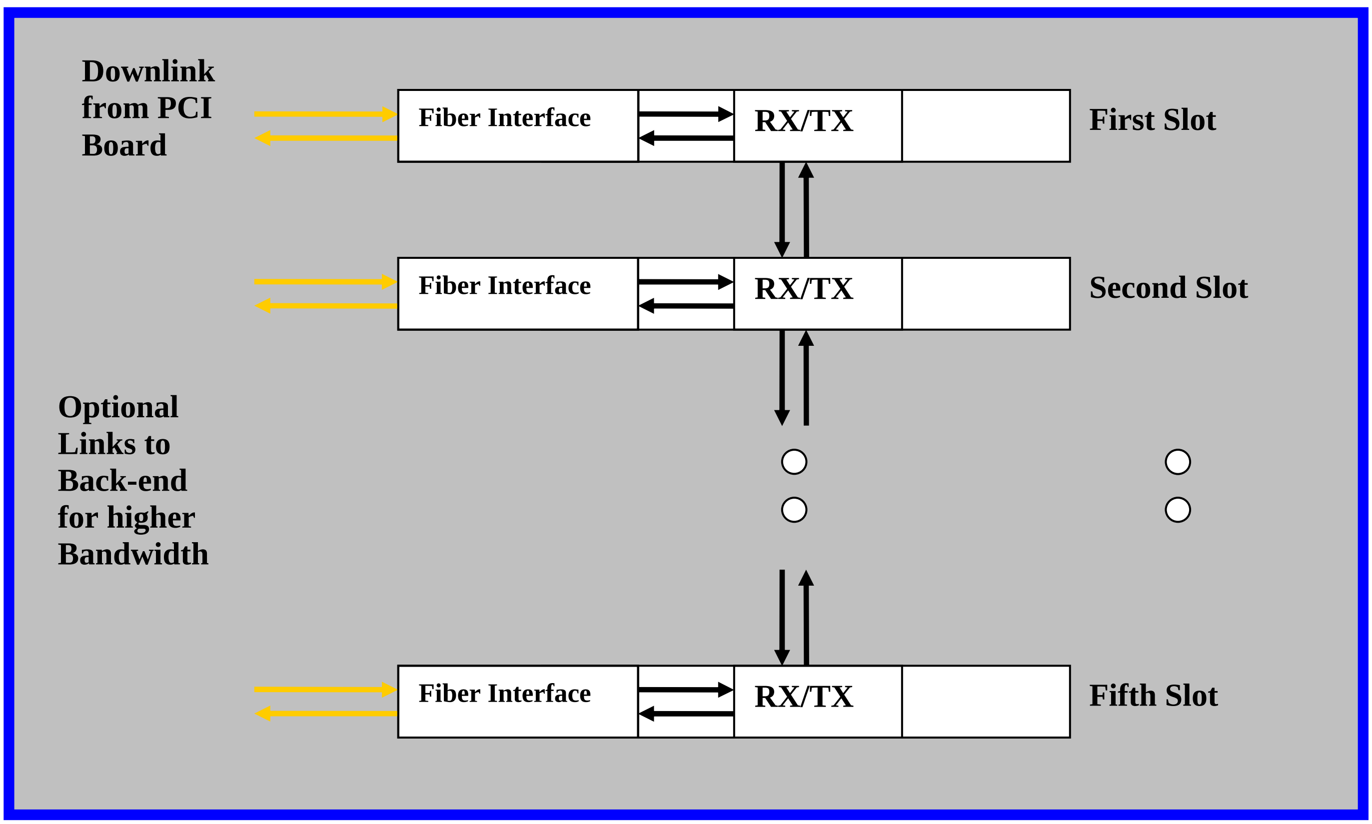

Fig. 6 High Speed Links

The bandwidth of one link is ~200MB/s and scales well with 33MHz PCI 64 ~ 256MHz. Two links scale with 66MHz PCI 64.

3.2 Link Transmission and Function Addressing

The communication between all system modules is based on packet transmission over serial links. The principle of communication is the same for all modules. A packet structure is defined to address a function (e.g. a register or memory in a front-end module) for read or write. Assume upstream of module1 is the back-end module. If a write to a function in module1 has to be executed, the packet addresses first RX COM (#2) then the address of the function (#ADDR). The next word determines that a WRITE (0) has to be executed. Then the data to write are in the next word (DATA).

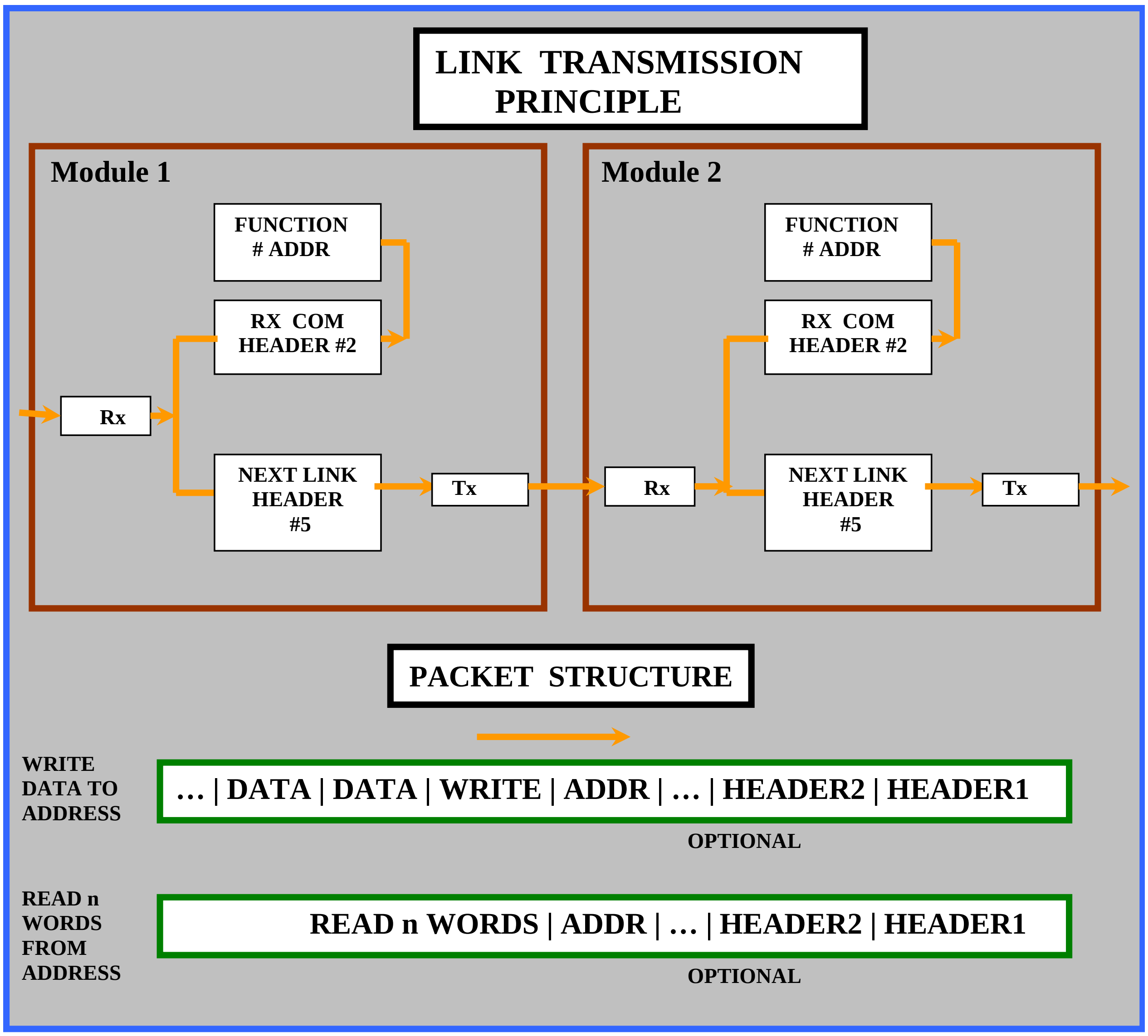

Fig. 7 Link Transmission

If more data statements follow, RX COM automatically increments #ADDR, and the writes are guided to consecutive locations.

A write to #ADDR in module2 has as first word NEXT LINK (#5) then the next word addresses RX COM (#2), next word is WRITE (0) then the DATA words follow.
Any word in the packet is 32 Bits wide.

Example

Write data word content 1 (Sequencer start) to Sequencer Command register #6000 in module1 :
Packet must be filled with : #2 #6000 #0 #1

If the sequencer would be in module2 on downstream link
Packet must be filled with : #5 #2 #6000 #0 #1

Reading data from a module has a similar structure. The function is addressed as before only the WRITE has to be replaced with a READ (#80000000) and then the number of words to read (#Number of Words). The read words are then automatically transmitted back to the receiver module (RX COM) in the Back-end.

Example

Read 10 words from sequencer memory in module1 (Sequencer RAM #4000)
Packet must be filled with : #2 #4000 #80000000 #A

If the sequencer would be in module2 on downstream1 link
Packet must be filled with : #5 #2 #4000 #80000000 #A

3.3 Back-End

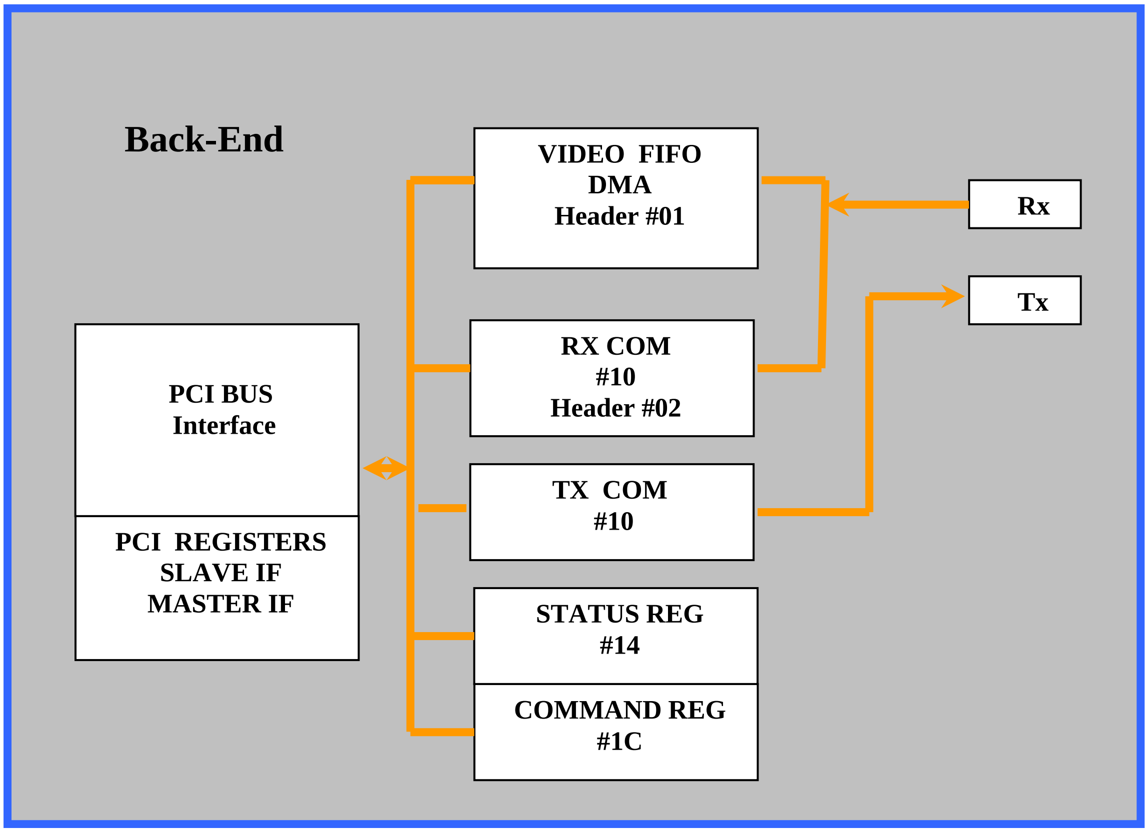

Fig. 8 Back-end Structure

The Back-end module connects to the data acquisition computer via a 64 bit PCI bus interface based on a XILINX IP module. The PCI bus interface has master and slave capabilities. The slave forms the communication interface to the front-end, the master is responsible for DMA transfers of video data to the computers memory. Commands and data transfers can run concurrently. The communication between back-end and any front-end module is based on packet transmission over high speed serial links. Data packets for communication have to be written to TX COM, read data packets from the Rx link are routed into RX COM. The COMMAND REGister initiates actions like fifo clear or transmission start. The STATUS REGister holds status information like fifo status or acknowledge bit. Video data from the link Rx are automatically routed to the VIDEO FIFO.
A transfer handshake protocol must always be followed for communication operations.

- **The packet has to be written from PCI to the back-end transmitter fifo (address #10).**
- **Then the transmission has to be initiated by writing from PCI to the command register (Write #10 to address #14).**

- **Then the Acknowledge register (address #14) has to be polled till acknowledge is received (Bit 7 set).**
- **Acknowledge register Bit 0 set declares a finished operation, Bit 1 successful operation on a valid address.**
- **Acknowledge register is cleared by reading the receiver fifo (address #10)**

Addresses

Relative address[Hex] Config Space		Function
C W		DMA Control Register
10 R/W		Read Rx FiFo / Write Tx Fifo
1C R/W		COMmunication Status/Command
68 R/W		PCI_Descr_Pointer #90 ADI
84 R/W		PCI_Addr_Reg
8C R/W		PCI_ DMA_Counter_Reg
90 R/W		PCI_Descr_Pointer

Relative address[Hex] DMA Space		Function
0		------
8 R		DMA Status Register

Registers

DMA Status Register – Read (Addr #8)

Bit 5	Data FiFo Empty
Bit 6	Data FiFo Full
Bit 7	Data FiFo Full – Write (Cleared by Clr Data FiFo)

Read Rx FiFo / Write Tx FiFo (Addr #10)

Bit 0..31	**Com Data**

COMmunication Status/Command – Write (Addr #1C)

BIT 0	**Clear Com FiFos**
Bit 1	**Clear Video FiFo**
Bit 4	**Transfer Enable TX**
Bit 7	**Test Box Enable**

COMmunication Status/Command – Read (Addr #1C)

BIT 0	**Ack Received**
Bit 1	**Valid Address accessed**
Bit 5	**Video FiFo Empty**
BIT 6	**Video FiFo Full**
Bit 7	**Overflow Error Flag (Write on Video FiFo Full - Cleared by Clr Video FiFo)**
Bit 8	**RX FIFO Empty**
Bit 9	**RX FIFO Full**
Bit 10	**TX FIFO Empty**
Bit 11	**TX FIFO Full**
Bit 12	**Link Channel Up**
Bit 13	**Link Hard Error**
Bit 14	**Link Soft Error**
Bit 15	**Link Framing Error**

INTR_Ctr_Reg (Addr #68)

Bit 21	**Interrupt Flag**

PCI_Addr_Reg (Addr #84)

Bit 0..31	**DMA Address**

PCI_DMA_Counter (Addr #8C)

Bit 2..12	**DMA Count**

PCI_Descr_Pointer (Addr #90)

Bit 4..31	**Initial DMA Descriptor**

DMA Command Register – Write only (Addr #A8)

BIT 1	**Start DMA**
Bit 2	**Abort DMA**
Bit 3	**Clear Interrupt**

3.4 Front-End

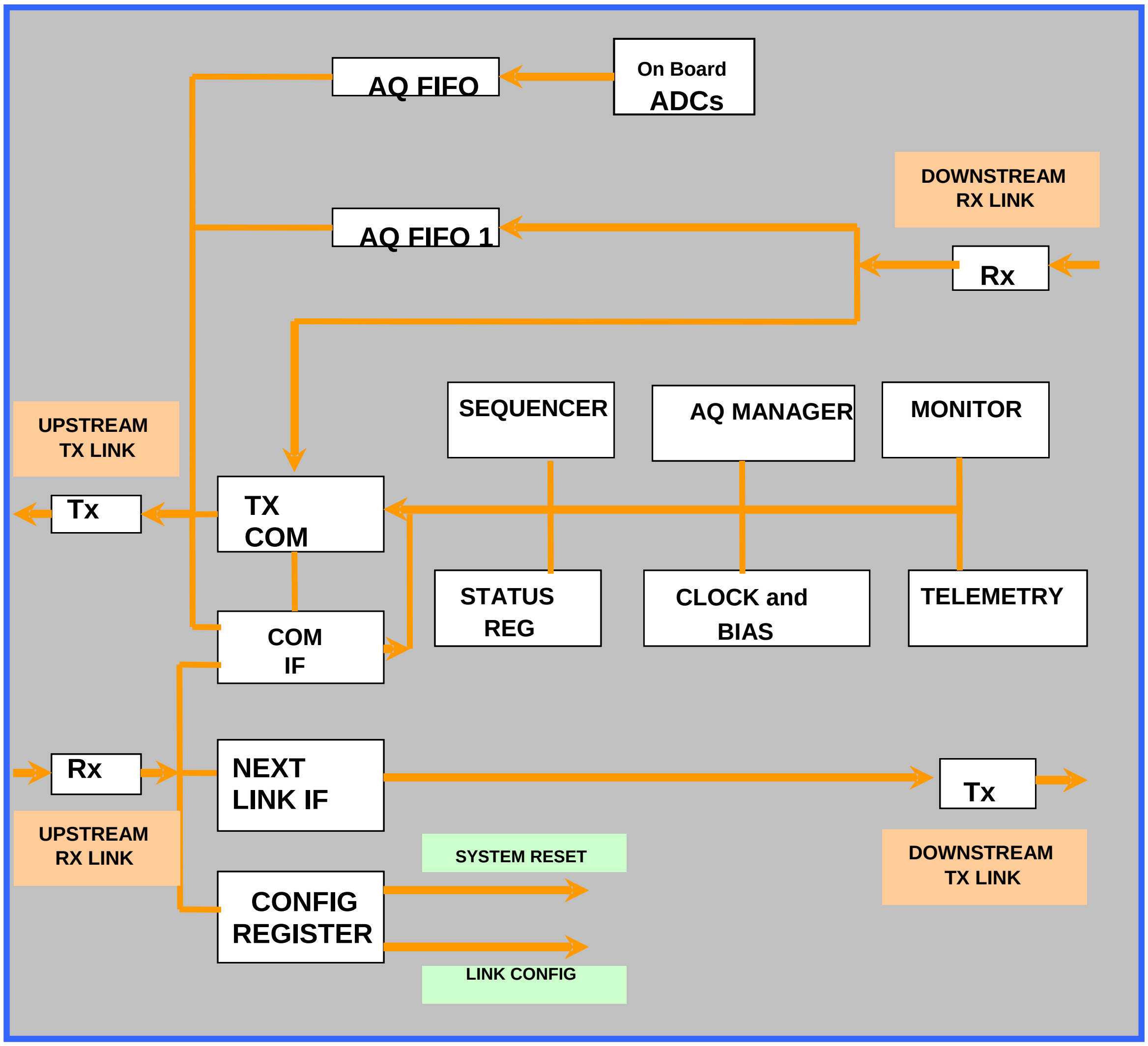

Fig. 9 Front-end Basic Module Structure

The Front-end Basic module is connected to the Back-end module with the upstream link. A downstream link on the Front-end Basic module connect to an additional module like AQ32 or other basic modules if more clocks or biases are required. From there again a link connects downstream to the next module.
Before any addressing of functions on Front-end modules the link structure of the Front-end system must be defined. This happens by writing the CONFIG register of each module.
RX_COM together with TX_COM form the communication interface to the modules on Front-end. The upstream links send all set-up and command information for the onboard functions to RX_COM where

Address and data are extracted and send to the individual on board modules, replies from the modules for the uplink enter TX_COM.
The Sequencer generates clock patterns. They are transformed to analogue clocks with the voltage settings of the Clock and Bias module. There also defines the dc biases for detector operation.
The Monitor module sets the clock and the video monitors to the channels chosen and routes the signals to the front panel Lemo connectors.
ADC data from the four onboard video channels or the downstream links are written to the AQ fifos.
The AQ Manager organizes the video data transfer to the downstream link.
The status register holds system information for control and debugging.
The Next Link module routes the upstream link packets to the desired header addressed downstream link.

3.5 Front-end Addressing

3.5.1 Front-End Configuration Register

Before any addressing of functions on Front-end modules the link structure of the Front-end system must be defined. This is accomplished in the Front-End Link Config Register. It is the only register on the Front-end where no handshake signals are generated, just because without structure definition no reply is possible. These registers are the first ones to set in any system set-up. The registers are addressed directly by header addressing in an order that the modules next to the Back-end have to be programmed first. A general module reset similar to power up can also be executed by this register.

Front-End Config Register **(Header 0X8)**

BIT 3..0	**Number of UpStream links till Back-end (Minimum is 1)**
Bit 15	**Global Reset** **Resets module to power up condition and puts global reset to backplane what resets all boards connected to the backplane.** **Not affected are sequencer memories and bias/clock voltage settings.**

Example :

Module1 (e.g. Basic Module) connected to back-end
= 1 upstream link
Module2 (e.g. first AQ32) connected to Basic module
= 2 upstream links
Module3 (e.g. second AQ32) connected to Module2
= 3 upstream links
Module4 (e.g. second Basic Module) connected Module3
= 4 upstream links

Packet Data :	**0X8 0x1**	**(Basic module)**
	0x5 0x8 0x2	**(first AQ36 module)**
	0x5 0x5 0x8 0x3	**(second AQ36 module)**
	0x5 0x5 0x5 0x8 0x4	**(second Basic module)**

3.5.2 Front-End Status

Front-end status contains two read only registers. The ID register contains an individual number derived from an on board ID Rom . The status register contains various module status information.

Status Register – Read   ADDR #1000

BIT 0	**UPSTREAM_CHANNEL_UP**
Bit 1	**DOWNSTREAM1_CHANNEL_UP**
Bit 2	**DOWNSTREAM2_CHANNEL_UP**
BIT 3	**DOWNSTREAM3_CHANNEL_UP**
Bit 4	**UPSTREAM_HARD_ERROR**
Bit 5	**DOWNSTREAM1_HARD_ERROR**
Bit 6	**DOWNSTREAM2_HARD_ERROR**
Bit 7	**DOWNSTREAM3_HARD_ERROR**
Bit 8	**TX_COM_FIFO_FULL**
Bit 9	**TX_COM_FIFO_EMPTY**
Bit 10	**NEXT_LINK_FIFO_FULL**
Bit 11	**NEXT_LINK_FIFO_EMPTY**
Bit 12	**0**
Bit 13	**0**
Bit 14	**0**
Bit 15	**0**
Bit 16	**TX_AQ_FIFO_FULL**
Bit 17	**TX_AQ_FIFO_EMPTY**
Bit 18	**TX_AQ_FIFO1_FULL**
Bit 19	**TX_AQ_FIFO1_EMPTY**
Bit 20	**TX_AQ_FIFO2_FULL**
Bit 21	**TX_AQ_FIFO2_EMPTY**
Bit 22	**TX_AQ_FIFO3_FULL**
Bit 23	**TX_AQ_FIFO3_EMPTY**
Bit 24	**0**
Bit 25	**0**
Bit 26	**0**
Bit 27	**0**
Bit 28	**0**
Bit 29	**0**
Bit 30	**OUTPUT ENABLED**
Bit 31	**SEQUENCER RUNNING**

ID Register – Read ADDR #1002 (Content 19-08-04)

BIT 0	**0**
Bit 1	**0**
Bit 2	**1**
BIT 3	**0**
Bit 4	**0**
Bit 5	**0**
Bit 6	**0**
Bit 7	**1**
Bit 8	**1**
Bit 9	**0**
Bit 10	**0**
Bit 11	**1**
Bit 12	**1**
Bit 13	**0**
Bit 14	**0**
Bit 15	**0**
Bit 16	**reserved**
Bit 17	**reserved**
Bit 18	**reserved**
Bit 19	**reserved**
Bit 20	**reserved**
Bit 21	**reserved**
Bit 22	**reserved**
Bit 23	**reserved**
Bit 24	**reserved**
Bit 25	**reserved**
Bit 26	**reserved**
Bit 27	**reserved**
Bit 28	**reserved**
Bit 29	**reserved**
Bit 30	**reserved**
Bit 31	**reserved**

3.5.3 Monitor

The monitor module routes buffered video channel inputs and two selected detector clocks to front panel Lemo connectors.
There is one register for the video channel and there are two registers corresponding to the clocks.

Video Monitor Register – Write ADDR #B000

BIT 1 .. 0	**Video Channel**

Clock Monitor1 Register – Write ADDR #B001

BIT 3 .. 0	**Clock Channel**

Clock Monitor2 Register – Write ADDR #B002

BIT 3 .. 0	**Clock Channel**

3.5.4 Detector Bias Generation

Detector Bias Generation is responsible for programming the voltages of clocks and biases. The module contains two register. The lower 14 Bits of the Bias Register set the bias value, the next five Bits the DAC number. Bit 31 programs an offset common to all DACs (no DAC number required – set to 0).

Physically there are two 32channel DAC's for the voltages of clocks and biases on the board.
DAC1 with channel number 0 to 31 determines clock low and clock high of the 16 clocks – pairs to clock low, impairs to clock high.
Detector biases 0 to 16 are on DAC2

V_OUT = 0.001259 * V_DATA_VALUE – 0.001076 * V_OFFSET_VALUE + Individual OFFSET

> Individual OFFSET is offset introduced by DAC and Buffer Amplifier (~ 100mV) on each channel individually – can be masked out by software for each board individually

Bias Register – Write ADDR #8000

BIT 13 .. 0	**Data Value**
Bit 21 .. 16 **(Bit 20..16 - DAC Channel** **Bit 21 selects DAC Chip** **- 0 Clocks** **- 1)**	**DAC Number** **(Clock_1 _low = 0** **Clock_1_high = 1** **Clock_2 _low = 2** **Clock_2_high = 3** **.** **.** **Clock_16 _low = 1E** **Clock_16_high = 1F** **DC_Bias_1 = 20** **.** **.** **DC_Bias_16 = 2F** **.** **DC_Bias_20 = 33)**
Bit 31	**Offset Select**

The Control register enables the clock and bias outputs to the detector, bit 15 resets all Biases to Zero Volts.

Control Register – Write ADDR #8001

BIT 0	**Enable Bias and Clock Outputs**
Bit 15	**Reset all Biases to Zero Volts**

3.5.5 Telemetry

Telemetry reads the voltage of clock levels and biases and digitizes with 16 Bit accuracy. The user has to write the channel address to examine, this issues automatically after a delay the conversion command and writes the telemetry adc data to a register. After the delay (~1ms) the data are ready for read. This is accomplished by a read of the telemetry register what transfers the data to the Rx Com register (Address #10 Address space PCI).

Channel 0 to 1F read the clock levels after a series resistor of 27 Ohms.
Channel 20 to 2F read the Bias levels before a series resistor of 100 Ohms.
Channel 30 to3F read the Bias levels after a series resistor of 100 Ohms.

Clock current measurements can be carried out by reading a voltage one time with output enable on and the other measure with enable off . Current can be calculated by dividing the voltage difference by the series resistor.
Bias voltage current measurements can be carried out by reading the voltage before and after the series resistance.

Telemetry Register – Write ADDR #A000

BIT 5 .. 0	**Channel address** **(Clock_1 _low = 0** **Clock_1_high = 1** **Clock_2 _low = 2** **Clock_2_high = 3** **.** **.** **Clock_16 _low = 1E** **Clock_16_high = 1F** **DC_Bias_1 = 20** **.** **.** **DC_Bias_16 = 2F** **.** **DC_Bias_20 = 30)**

Telemetry Register – Read ADDR #A000

BIT 15 .. 0	**Telemetry data**

3.5.6 Sequencer

The Sequencer generates the clock patterns for the readout of the detector.

3.5.6.1 Principle

The Pattern Ram (2048 x 64) is loaded with the clock patterns. Any pattern length between 1 and 2048 is possible. Pattern Ram Low holds Bit 31 downto 0, Pattern Ram High holds Bit 63 downto 32. The dwell time of a pattern word is included in the word as well as special function bits (see pattern ram description).
The Sequencer Ram (2048 x 32) holds the Seq Code Bits, the pattern address and the pattern repetition count. The Seq code Bits (see seq ram description) feed the Seq Code Interpreter. He decides if a pattern address is written into the Pattern Address Fifo and with the repetition count (16 bit) how often it is executed.
The Pattern Address Fifo contains the start address of the pattern supplied by the Sequencer Ram. The time counter loaded from the Pattern Ram determines the dwell time (16 bit – one bit = 10ns) of a pattern. The pattern address counter is incremented each time the time count is reached, in case the End of Pattern is present (bit 31) in the pattern word the next word, containing the start address of the next pattern, is read from the fifo. To avoid overrunning the Pattern Address Fifo (Empty read) at least eight patterns have to be written into the fifo.

The sequencer starts with the Sequencer Start Command (Command Register Bit 0). The first pattern is output after the code interpreter has written eight words into the pattern address fifo. The sequencer stops after the dwell time of a pattern when

1. the fifo is empty
2. a breakpoint in a pattern (bit 29 high word) is detected and the Sequencer Stop Command (Command Register Bit 1) was executed before (programmed end of sequence – option 1)
3. the Program End Bit (bit 30 high word) in a pattern is detected (programmed end of sequence – option 2)
4. Sequencer Reset Command (Command Register Bit 15) is executed (immediate stop)

In case 1,2,3 the status, counters, controls are as at stop time, so to start a new sequence or to restart the old one a Sequencer Reset Command has to be executed before.

If in a pattern word the Wait for Trigger (bit 28 high word) is set, the sequencer stops after the dwell time of this pattern and waits for a trigger signal, which may be set from external inputs or software (bit 7 Command Register). Hint : Wait for Trigger together with software trigger can be used for stepping through patterns and sequences.

The Sequencer Status register (see Sequencer Status register description) contains status information about code interpretation and sequence termination. This information is cleared with the Sequencer Reset command. Fifo status is always available.

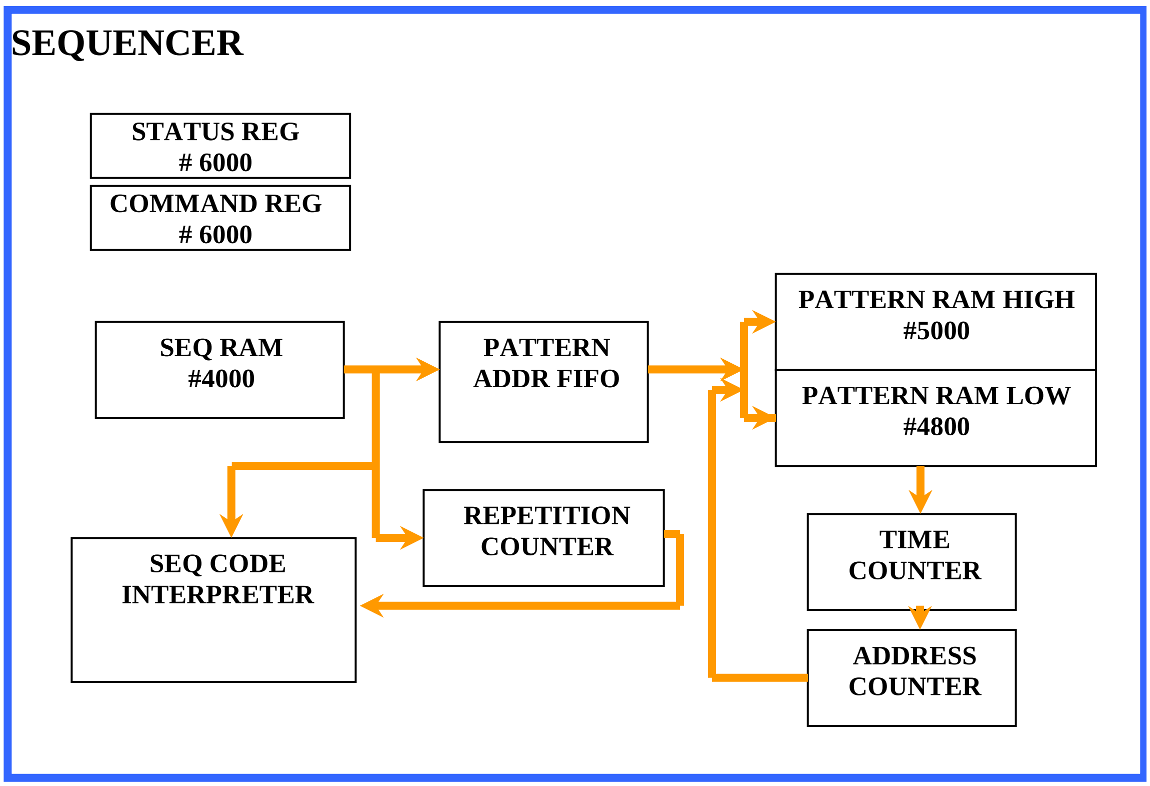

Fig. 10 Sequencer Block

3.5.6.2 Register Description

Command Register – Write ADDR = #6000

BIT 0	**Sequencer Run**
BIT 1	**Sequencer Run Disable (used if more than one SEQ are installed in a backplane - only one can be active)**
Bit 3	**Stop Sequencer at next Breakpoint**
Bit 7	**Software Trigger**
Bit 15	**Sequencer Stop and Reset (immediate)**

Status Register – Read ADDR = #6000

BIT 0	**Code Interpretion Running**
Bit 1	**Sequencer Running**
Bit 2	**Sequencer Waiting for Trigger**
BIT 3	**reserved**
Bit 4	**End of Program Signal**
Bit 5	**End at Breakpoint**
Bit 6	**Fifo Empty**
Bit 7	**Fifo Empty Read**
Bit 8	**Fifo Full**
Bit 26 ..16	**Pattern Ram Address**

3.5.6.3 RAM Description

SEQ RAM ADDR = #4000 till #47FF

BIT 10 .. 0	**Pattern Start Address**
Bit 26 .. 11	**Pattern Repetition Count**
Bit 27	**reserved**
Bit 30 .. 28	**Sequence Code**
BIT 31	**reserved**

PATTERN RAM LOW ADDR = #4800 till #4FFF

BIT 31 .. 0	**Clock 31 .. 0**

PATTERN RAM HIGH ADDR = #5000 till #57FF

BIT 0	**Convert 1**
BIT 1	**Convert 2**
Bit 3..2	**reserved**
Bit 4	**Utility Signal 1 (Routed to Opto Outputs)**
Bit 5	**Utility Signal 2 (Routed to Opto Outputs)**
Bit 7..6	**Pattern Ram (7 .. 0) Write Disable**
Bit 8	**Pattern Ram (15 .. 8) Write Disable**
BIT 9	**Pattern Ram (23 .. 16) Write Disable**
Bit 10	**Pattern Ram (31 .. 24) Write Disable**
BIT 11	**Pattern Ram (39 .. 32) Write Disable**
BIT 27 .. 12	**Pattern Dwell Time (Value x 10 ns)**
BIT 28	**Wait for Trigger (causes Sequencer Wait for Trigger)**
BIT 29	**Breakpoint (causes Sequencer to stop at this pattern after SEQ STOP command - Routed to Status)**
BIT 30	**End of Program (Routed to Status Register for inspection of correct Sequence Termination)**
BIT 31	**End of Pattern (causes fetch of next Pattern after Dwell Time of Pattern)**

3.5.6.4 Sequencer Codes

000	**Stop Pattern Interpretation**
001	**EXEC Pattern (Number of Pattern, Number of Repetitions)**
010	**LOOP (Number of Repetitions)**
011	**LOOP END**
100	**LOOP INFINITE**
101	**JUMP SUBROUTINE (Address)**
110	**RETURN SUBROUTINE**
111	**Stop Pattern Interpretation**

3.5.7 AQ Manager

Each board contains one AQ Manager. He is responsible for organizing the video data transfer of and through this board. The AQ Manager contains in addition a programmable video data simulator.
After conversion and packet formation as defined in the AQ Manager Command Register, the data are written automatically to the AQ FIFO's and transferred. Then AQ manager looks in the Transfer Counter if additional packets should arrive from the downstream link. If yes and arrived, these data packets are also written to the AQ FIFO's and transferred.

In simulation mode the video data are generated inside the FPGA.
In simulation mode 1 the video data are derived by a counter incremented by the conversion strobe.
In simulation mode 2 the video data are reflect the video channel number.

AQ Manager Command Register– Write (Addr #3000)

BIT 4..0	**NADC** **= Number of ADCs to read on this board**
BIT 7..5	**reserved**
BIT 15..8	**PACKETSIZE** **=Number of data words (32Bit) per Packet (must be multiple of NADC)**
BIT 19..16	**Transfer Counter** **(Number of packets arriving from Downlink -> 1 means 1 packet from Downlink)**
BIT 20	**Enable Conversion by Backplane Signal "Convert " for on Board ADC's**
BIT 21	**Enable Conversion by Backplane Signal "Convert1 " for on Board ADC's**
BIT 23..22	**reserved**
BIT 24	**Declare Module as First in Chain** **(module needs no transfer permission)**
BIT 27..25	**reserved**
BIT 28	**Simulation Mode**
BIT 29	**Simulation Mode : 0 =Numbers** **1 =Counter**
BIT 31..30	**reserved**

AQ Manager Status Register– Read (Addr #3000)

BIT 0	**AQ State “ IDLE ”**
BIT 1	**AQ State “ Waiting for CONVERT ”**
BIT 2	**AQ State “ Waiting for Downlink Data ”**
BIT 5..3	**Reserved**
BIT 6	**Error Condition : Data Overrun AQ FIFO**
BIT 7	**Error Condition : Data Overrun AQ FIFO1**

The AQ Manager Delay Register delays the conversion strobe to the ADC’s (in relation the sequencer generated clocks) by max 2.56 us.

AQ Manager ADC Delay Register – Write (Addr #3001)

BIT 7..0	**Delay of Conversion Strobe = (Value * 10ns + 10ns)**

3.5.8 Basic Board Front Panel

The Basic Board Front Panel green LED's indicate :

- Tx and Rx transfers
- Sequencer Running
- Bias and Clock output enable

The red LED's show :

- Link Lock Status of Uplink and Downlink

LEMO connectors carry :

- The buffered conversion signal
- Two digital markers
- A software selectable buffered differential video channel signal
- Two independently selectable buffered clock signals (copied at output connector)

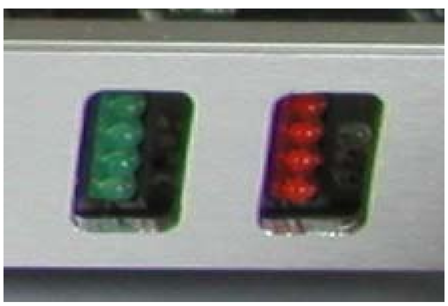

Fig. 11 LED's

Fig. 12 Basic Board Front Panel