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Organisation Européenne pour des Recherches Astronomiques dans l'Hémisphère Austral
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VLT PROGRAMME

VERY LARGE TELESCOPE

Interface Control Document for the **N**ew **G**eneral detector **C**ontroller (NGC)

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CHANGE RECORD

ISSUE	DATE	SECTION/PARA. AFFECTED	REASON/INITIATION DOCUMENTS/REMARKS
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1 INTRODUCTION

ESO has designed a standard controller for readout of both IR and optical detectors. It is a very compact design with emphasis on low power consumption, flexibility in structure, and modularity. The document describes the mechanical and electrical interfaces of the NGC controller for scientific detector applications, whereas document VLT-ICD-ESO-13660-4201 describes NGC for adaptive optics applications.

Note that this document is neither a design description nor a user manual. It only aims at providing the information needed by system engineering at the VLT instrument-level.

Because the mechanical design and some connector pin-outs are not yet finalized only prototype pictures of NGC are given in this release to give instrument designers a preliminary view of the necessary information.

1.1 List of Abbreviations & Acronyms

This document employs several abbreviations and acronyms to refer concisely to an item, after it has been introduced. The following list is aimed to help the reader in recalling the extended meaning of each short expression:

ADC	Analog-to-Digital Converter
AQ 32	32-Channel Acquisition Board
DAQC	Data Acquisition Computer
DCC	Detector Cryostat Cables
DFE	Detector Front-end
DFPS	Detector Front-end Power Supply
DPA	Detector Preamplifier
ESO	European Southern Observatory
FEB	Front End Basic Board
IWS	Instrument Workstation
LAN	Local Area Network
LLCU	Linux-based Local Control Unit
LSP	La Silla Paranal Observatory
NGC	New General detector Controller
HE	Height Unit
PCI	Peripheral Component Interconnect
SFP	Small Form Factor Pluggable
TBC	To Be Clarified
TBD	To Be Defined

1.2 Applicable Documents

(1) Next Generation detector Controller (NGC), Requirements, VLT-SPE-ESO-13660-3207, Issue 1.0, 11.03.2004

1.3 Reference Documents

(1) New General Detector Controller (NGC)
USER MANUAL
Doc.-No. VLT-MAN-ESO-13660-4510

(2) Adaptive Optics Interface Control Document for the New General detector Controller
Doc. No.: VLT-ICD-ESO-13660-4201

(3) Interface Control Document for a single Hawaii2RG based cryogenic detector setup
Doc. No.: VLT-SPE-ESO-14010-3853

2 System

2.1 Components

NGC consists of five major components (Figure 1):

- Data Acquisition Computer with integrated PCI interface (DAQC)
- Detector Front-end (DFE)
- Detector Front-end Power Supply (DFPS)
- Detector Cryostat Cables (DCC)
- Detector Preamplifier (DPA)

The Data Acquisition Computer is a 19-inch rack-mountable Linux workstation with integrated PCI interface. This connects to the Detector Front-end via a 2 GBit fiber optic link (1 km is a reasonable lower limit to the maximum length, which depends on the number of connectors). The Detector Front-end is accommodated in a custom-designed housing with an integrated mechanical interface to the instrument structure for optional passive cooling (high-performance systems need liquid cooling). The power supply for the DFE is a 19-inch 3HE rack-mountable unit (power supplies for large detector systems may be higher), which may be at a distance from the DFE of up to 12 meters (the shorter the better). The DCC between DFE and cryostat contain clock and bias lines and the video signals. The maximum length depends on application (< 2 m, maybe 3 m). The location of the Detector Preamplifier is application dependent – for IR systems inside the cryostat, for optical detectors the preamp is located outside the cryostat.

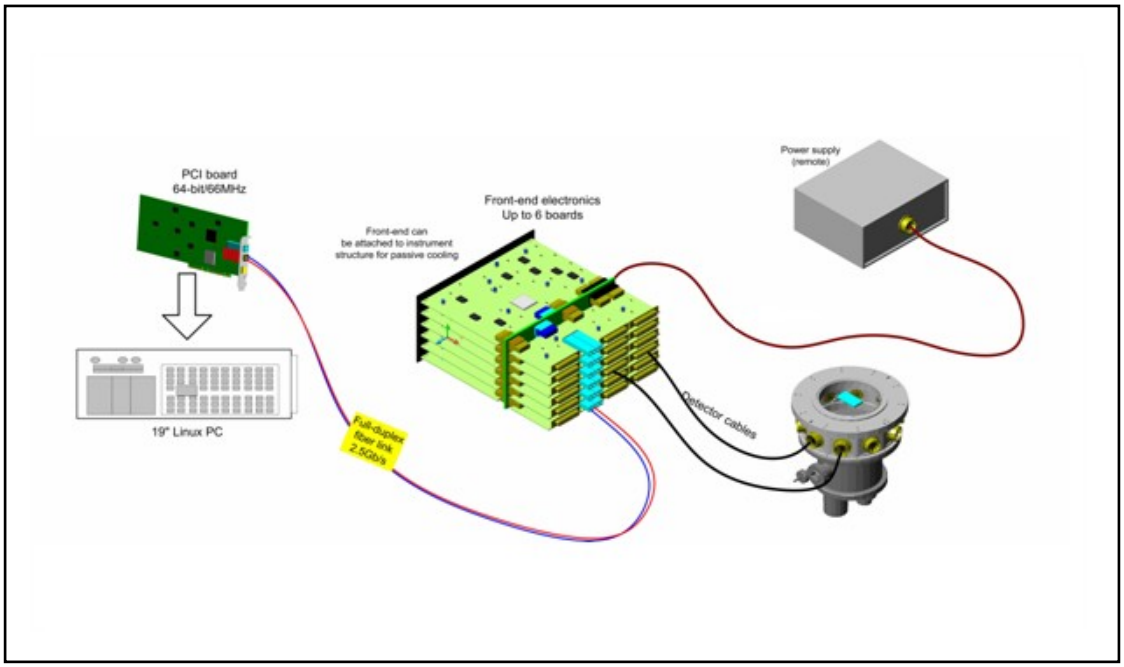

Figure 1 NGC Set-up

2.1.1 Data Acquisition Computer

2.1.1.1 Acquisition Computer

> **Note:** The information provided in this section will be updated regularly following the evolution of the standards adopted by ESO's SDD division for VLTSW.

The current (VLT2008) standard is a Dell PowerEdge 2950 III Server 19 inch rack-mountable. Details as provided by SDD (http://websqa.hq.eso.org/sdd/bin/view/SDDInfo/LinuxStandardHw) and integrated with data from Dell web page (http://www1.euro.dell.com/content/products/productdetails.aspx/pedge_2950_3?c=uk&l=en&s=bsd&cs=ukbsdt1) are listed in the table below.

Figure 2 Dell Power Edge 2950 III

Form factor	2U Rack-mountable chassis 74.4cm D x 44.43cm W x 8.64cm H with bezel attached Rack Weight 23 Kg, maximum configuration
Weight	Rack-mounted: kg 45.36, maximum configuration
Processors	2 x Quad Core Intel® Xeon® 5410, 4MB Cache, 2.33GHz, 1333MHz FSB
Memory	4GB 667MHz (4x1GB), Dual Ranked DIMMS
I/O Slots	PCI slots: either PCIe riser with 3 PCI Express slots [one x4 (x8 connector) and 2 x8] or 2 PCI-X 64-bit/133MHz and 1 PCI Express x8 slot NOTE: NGC requires PCI-X, therefore it is mandatory to explicitly request the option with PCI-X riser
Drives	24X IDE CD-RW/DVD ROM Drive PERC 5/i, x6 Backplane, Integrated Controller Card (internal RAID) (7) 1x6 Backplane for 3.5-inch Hard Drives 2/4/6 300GB, SAS, 3.5-inch, 10K RPM Hard Drive
Power supply	redundant 750W hot-plug auto-switching 110/220V AC
Energy Consumption	≤ 900 W (configuration dependent)
Video	Embedded ATI ES1000 with 16MB memory
Links	VLTSW standard: http://websqa.hq.eso.org/sdd/bin/view/SDDInfo/LinuxStandardHw Dell specs: http://www.dell.com/downloads/global/products/pedge/en/pe_2950_III_spec_sheet.pdf Dell web page: http://www1.euro.dell.com/content/products/productdetails.aspx/pedge_2950_3?c=uk&l=en&s=bsd&cs=ukbsdt1

2.1.1.2 Interface to Instrument Computer

Standard Gigabit Ethernet

2.1.1.3 Interface to the Front End

An ESO-made PCI64 board (Figure 3) with a fiber-optic connection to the Front End is installed in the Data Acquisition Computer. The maximum theoretical bandwidth per interface is 256MB/s, which matches the 2.5 GBit/s fiber transmission rate. The bandwidth for actual data transmission is about 20% lower. With 1MHz ADC's, one 32-channel Acquisition Board will generate a maximum data rate of 64 MB/s.

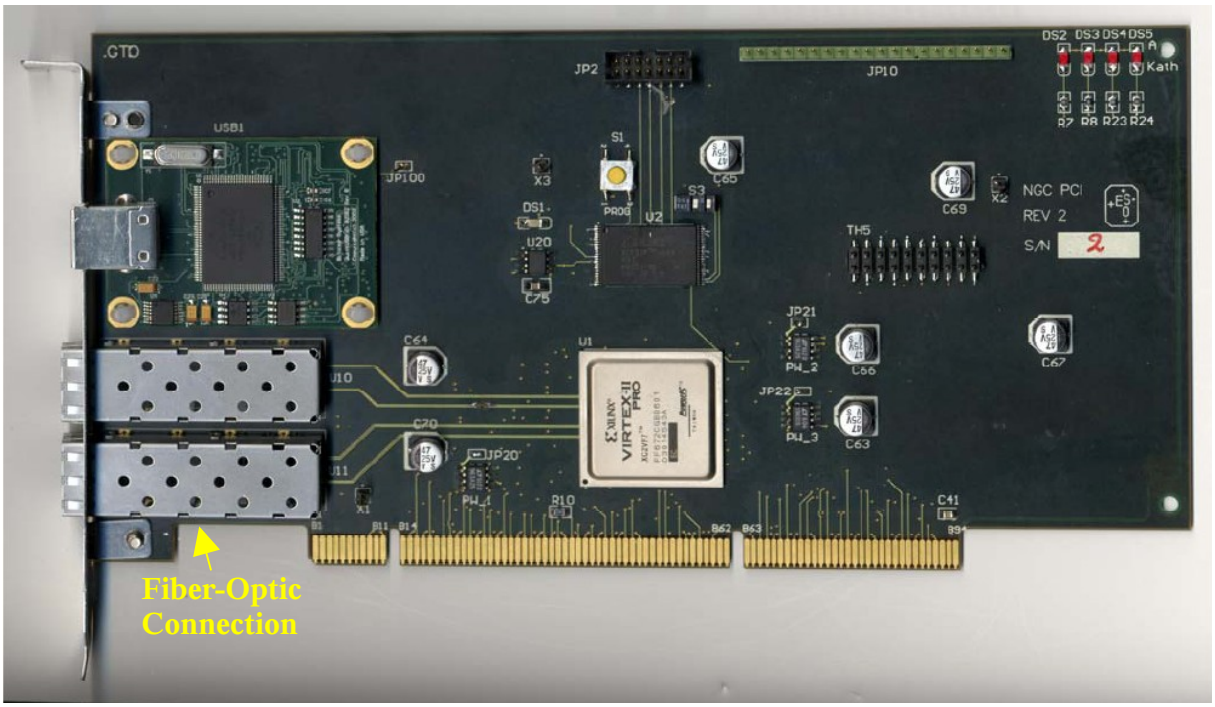

Figure 3 PCI Interface

2.1.1.3.1 Fiber-Optics Transceiver

The fiber-optic transceiver (Figure 4) used for all boards in the system is a laser transceiver (type FTRJ1321S1BTL, SFP body) from FINISAR. The transceiver wavelength is 1310 nm. Two transceivers are installed on each board.

Figure 4 Fiber-Optics Transceiver

2.1.2 Detector Front-end

The DFE has to be located close to or on the instrument (maximum detector cable length 2m – depending on the application, an extension up to 3m may be possible).

The modules, from which any NGC DFE can be built, are presently:

Basic Board – contains four video channels and clock/bias generation
Transition Board for Basic Board – contains external connections
AQ32 Board – contains 32 video channels
Transition Board for 32 Channel AQ Board – contains external connections

Every NGC system must include at least one Basic Board to supply the detector with clocks and biases. Each Basic and AQ32 Board must use the respective Transition Board. Depending on the characteristics of the detector system to be supported, many NGC configurations can be built with this tool kit.

So far, a two-slot system (targeted to the readout of small IR arrays or CCD mosaics with one Basic Board and one 32 Channel AQ Board), and a six-slot system (for more complex detector systems) have been built. Each slot can house either a Basic Board or an AQ32 board (plus associated Transition Board).

In order to prevent damage from overheating, all housings are equipped with a TBD thermal sensor that can shut off the power to the NGC box concerned and interface to the Paranal Central Alarm System (CAS).

2.1.2.1 View

A two-slot system with one Basic Board and one 32-Channel AQ board (plus associated Transition Boards) is shown in Figure 5 and Figure 6.

Tests by ESO have shown that even a single-board system does not fulfil the VLT Environmental Specifications if it is not actively cooled. Because the volume of an active cooling system dominates the total volume, only a six-slot actively cooled system is offered.

On specific demand, ESO can make available an uncooled 2-slot housing. This housing is safe for usage in the laboratory. However, if a project wants to deploy it in one of the LSP domes, the project will have to demonstrate that the dissipated heat is carried away such that the VLT Environmental Specifications are fully met.

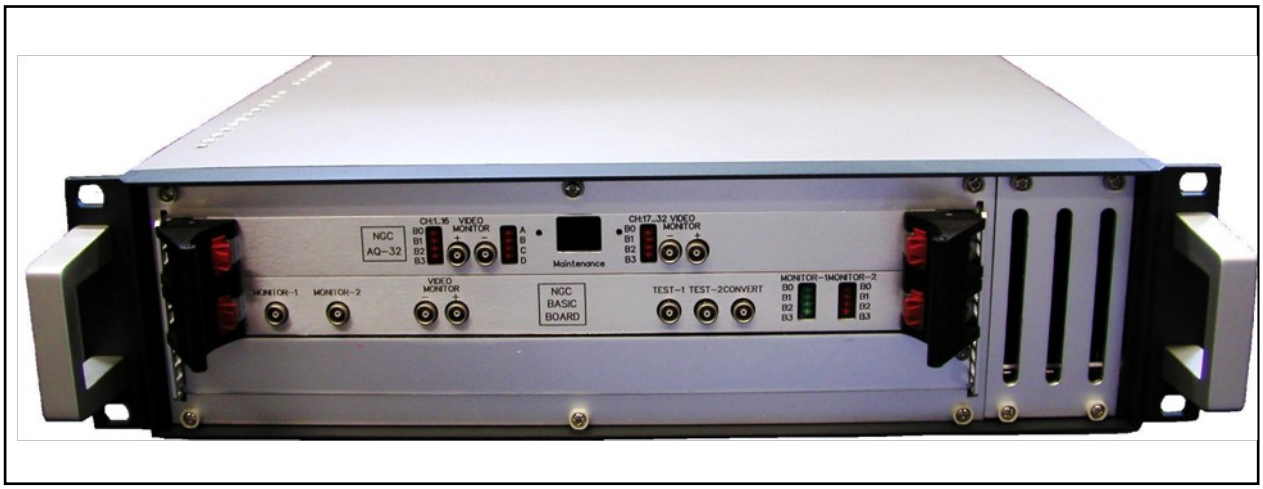

Figure 5 NGC Two-Slot System - Front side view

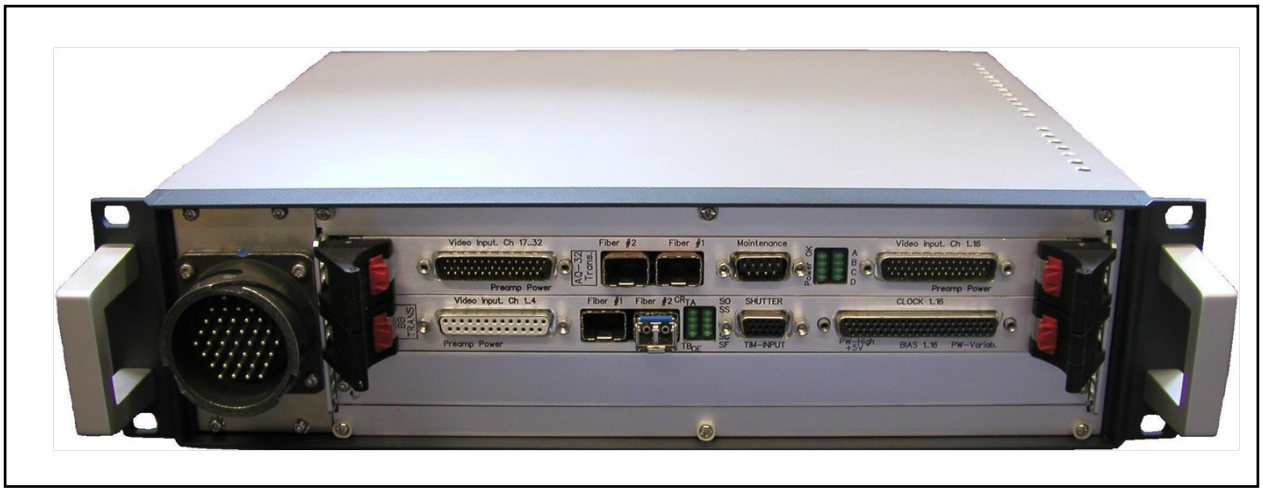

Figure 6 NGC Two-Slot System – Back side view

Figure 7 shows the final drawings of a water-cooled NGC six-slot system (to be produced Sep 08).

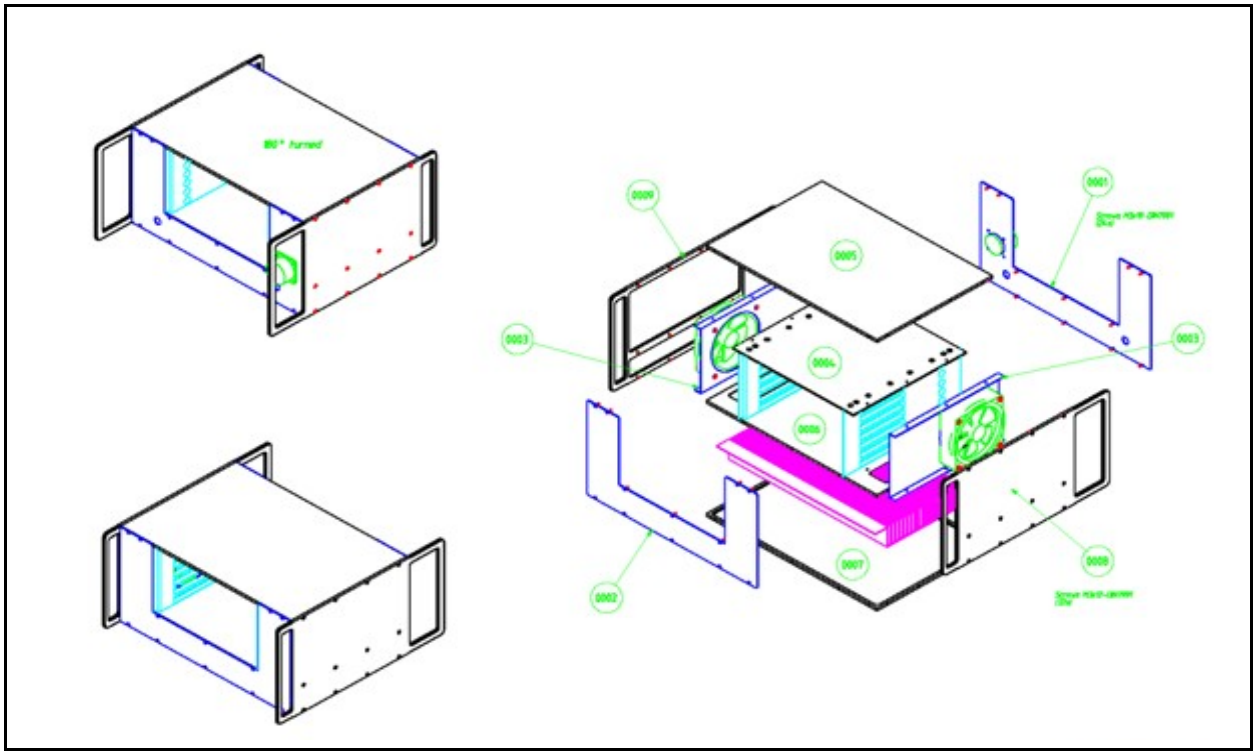

Figure 7 NGC – Six-slot system – final drawings

A prototype six-slot system with integrated temperature controller is shown in Figure 8 and Figure 9.

Figure 8 NGC – Six-slot system – front side (Prototype)

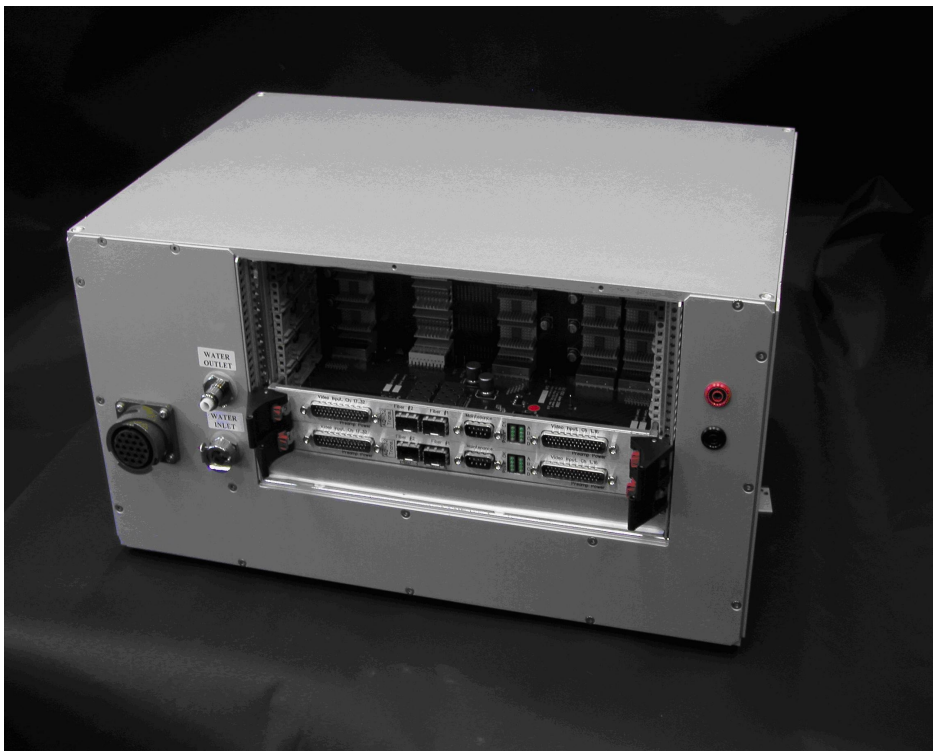

Figure 9 NGC- Six-slot system – back side (Prototype)

2.1.2.2 Size and Weight

NGC - two slot system

Height	:	90	mm
Depth	:	362	mm
Width	:	375	mm
Weight	:	4.2	Kg

NGC - six slot system

Height	:	216,5	mm
Depth	:	421	mm
Width	:	442	mm
Weight	:	~ 15	Kg

2.1.2.3 Power Consumption

~15 Watts per Basic Board
~20 Watts per 32-Channel AQ Board

2.1.3 NGC Module Connections

All NGC connections to the external are handled via transition boards on the back side of the system modules like FEB,AQ32 (Figure 10 and Figure 11).

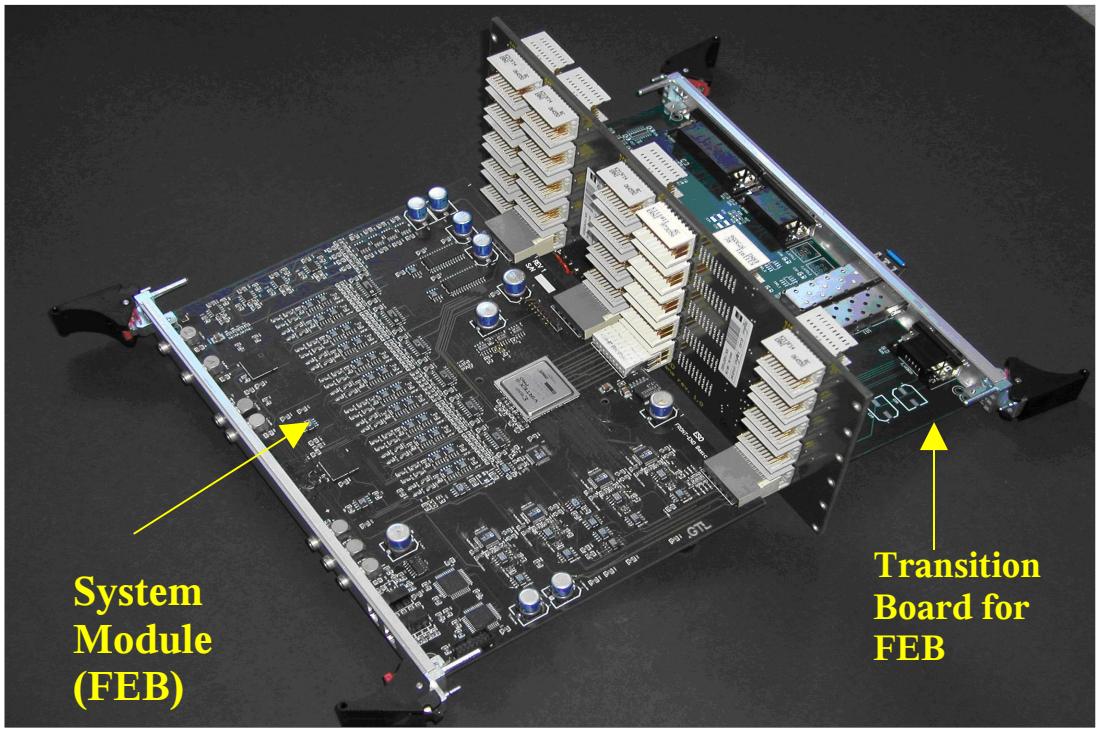

Figure 10 NGC System Setup

2.1.3.1 Transition Boards of Basic Board (FEB) and 32 Channel Board (AQ32)

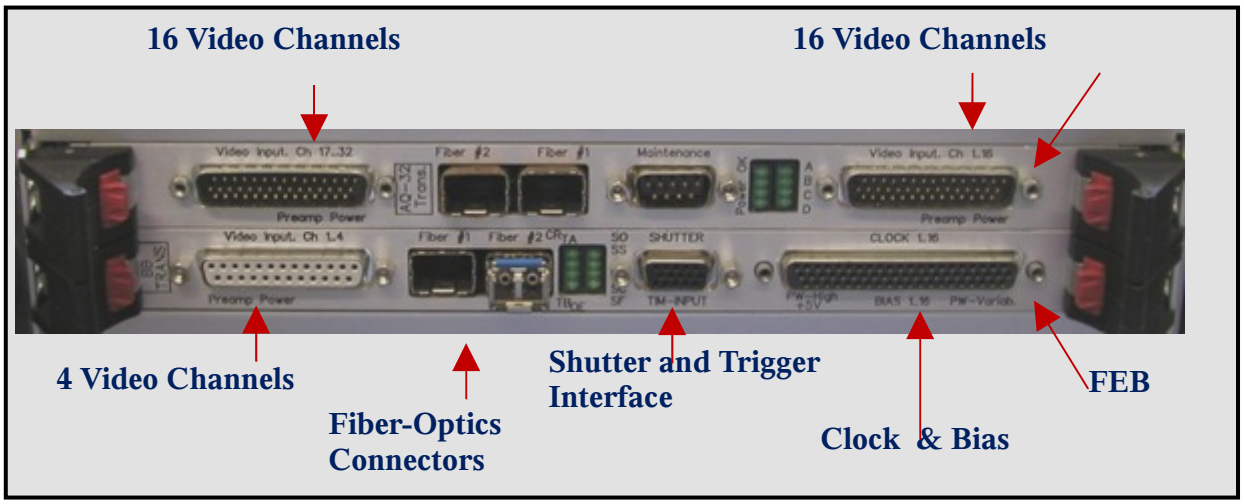

Figure 11 Transition Board of Basic Board with External Connections

2.1.3.1.1 Video Inputs

The FEB video input is accomplished via a female DB 25 connector (Figure 12) on the Transition board of FEB. On the connector are 4 differential video inputs VID_POS1..4, VID_NEG1..4), Preamp Power (POWER_MINUS_PREAMP, POWER_PLUS_PREAMP) as well as four programmable digital outputs (I2C_CLK and I2C_SDA (not galvanically isolated) for the control of the gain and the bandwidth on the preamp, GPIO_8 (galvanically isolated) for general purpose use and GPIO_9 (galvanically isolated) for the DC restoration on the preamp.

The cable connecting to this connector should be made of 4 pairs of twisted-pair cables for the video and 7 single wires. A shield surrounding all cables should be implemented. It shall be connected to the housing on both sides of the cable.

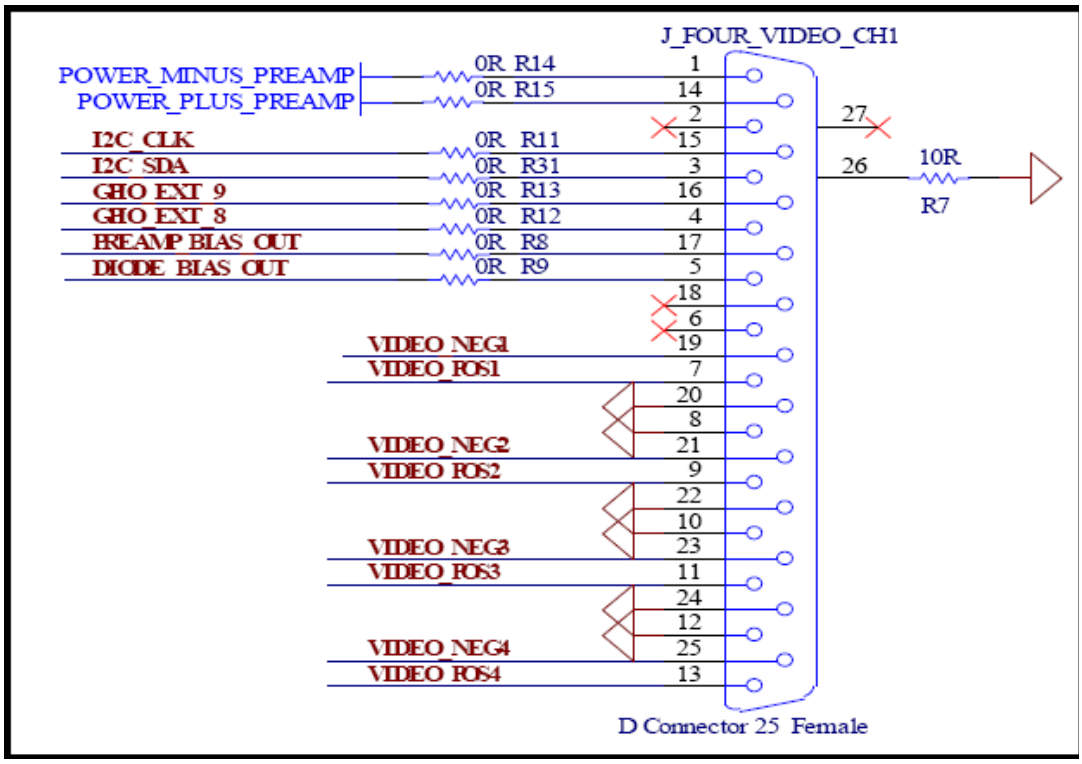

Figure 12 Video Input Connector Basic Board

The AQ32 video input is accomplished via two female HD 44 connectors (Figure 13) on the transition board of AQ 32. The AQ32 has 32 video channels and is intended for the use with infrared detectors. Each HD44 connector on the Transition board features 16 differential video inputs and 4 power lines for cryostat internal circuitry. The pin-out is the same for both connectors with HD1 (right) being used for channels 1 to16 and HD2 (left) for channels 17 to 32.

The cable connecting to these connectors should be made of 16 pairs of twisted pair cables for the video and single wires for the power supply connection. A shield surrounding all cables should be implemented. It shall be connected to the housing at both ends of the cable.

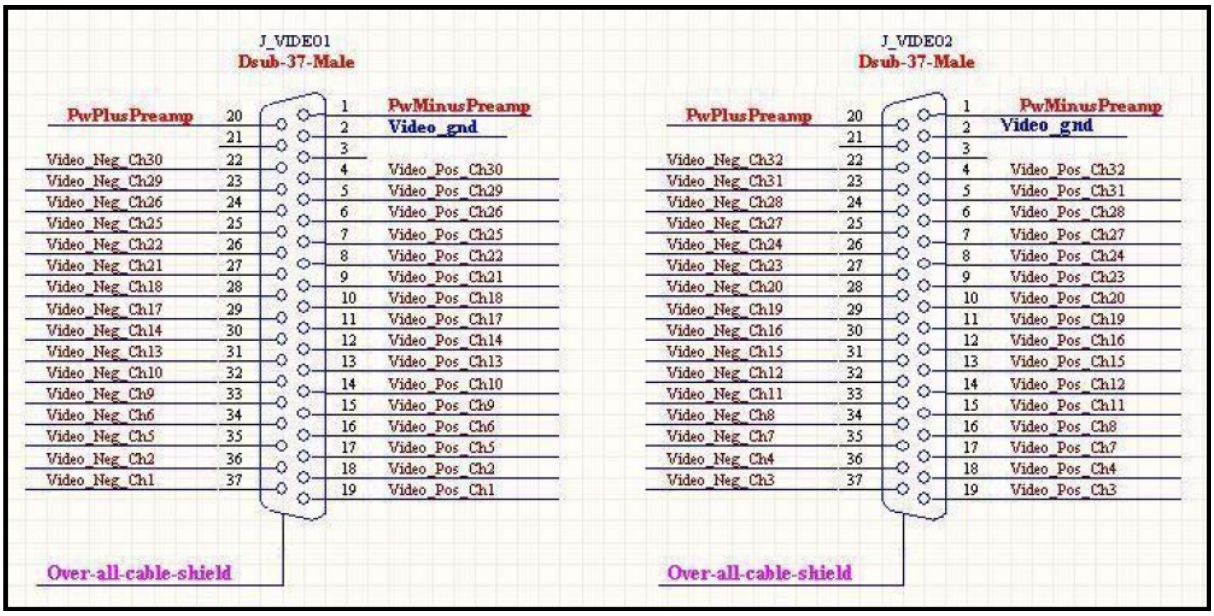

Figure 13 Video Connectors AQ 32

2.1.3.1.2 Clock and Bias

The clock and bias output is accomplished via a female HD62 connector (Figure 14) transition board of the Basic Board. On the connector are 18 clocks, 20 bias voltages, 5 power lines and one isolated enable output (5Volt high/low only) to control external clock and bias drivers.

Bias and clock voltage lines should use coax cables to connect to the detector. An overall shield connected on both sides should be used.

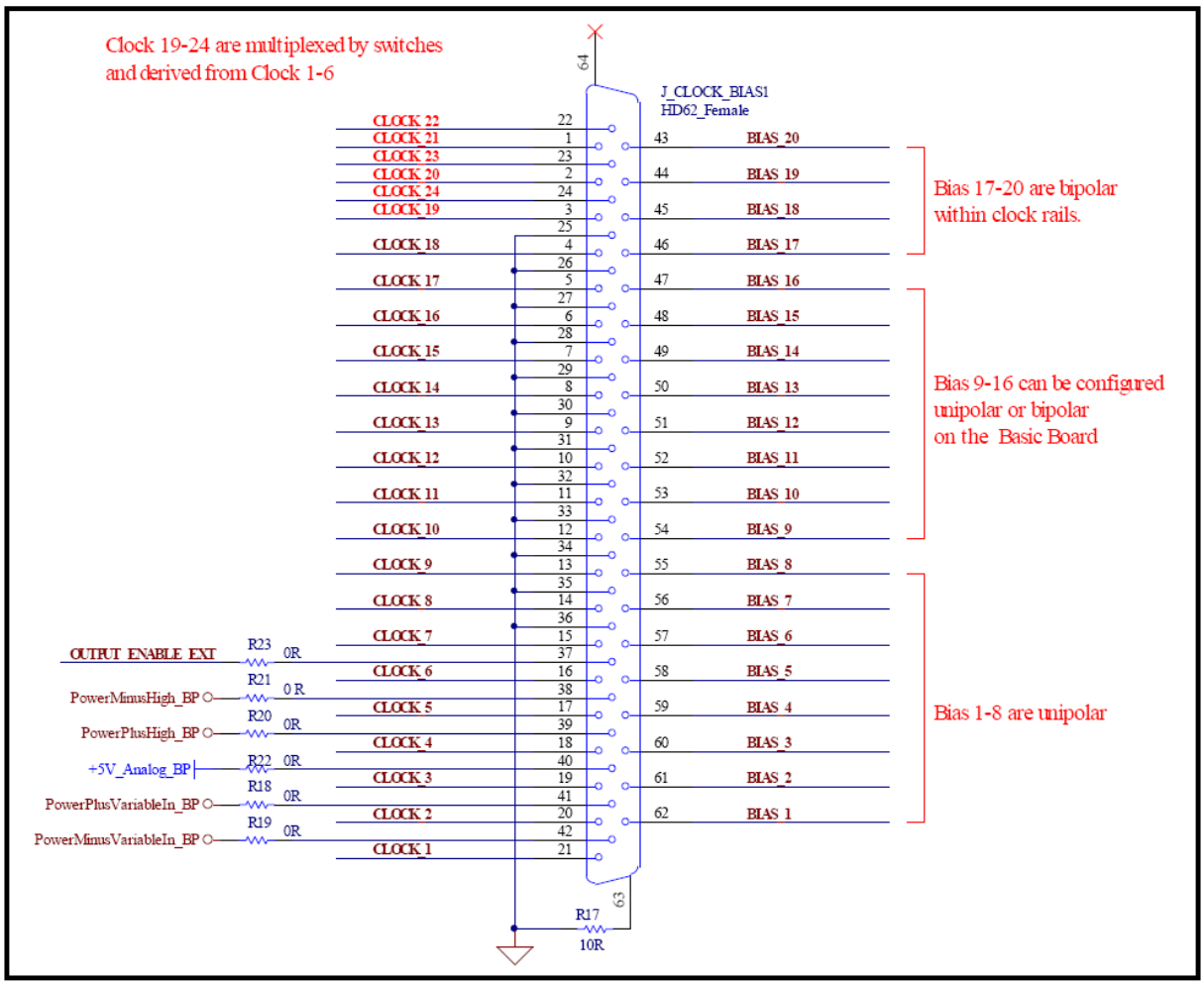

Figure 14 Clock and Bias Connector

2.1.3.1.3 Shutter Interface and Trigger Input

On the Transition Board of the FEB an HD15 connector (Figure 15 and Figure 16) with galvanically decoupled lines carries the signals for shutter output and trigger input. Additionally, external power inputs for the galvanic isolator are on this connector.

2.1.3.1.3.1 Optical Instruments

The shutter control of NGC-based CCD detector systems is implemented in the FPGA of the Basic Board.
***IMPORTANT*:** In order for NGC to control a shutter, the shutter must provide the power for the galvanically isolated interface on the transition board. This is carried out by connecting external +5V and ground to pins 7 and 8, respectively, on the HD15 connector.

The direction and functionality of the shutter signals is:

- *ShutterOpenCommand* (Output): To drive the open and close of the shutter.

- *ShutterCloseStatus* (Input): Driven by shutter to signal that the shutter is fully closed.
- *ShutterOpenStatus* (Input): Driven by the shutter to signal that the shutter if fully open.
- *ShutterFail* (Input): Driven by the shutter to signal that error occurred.

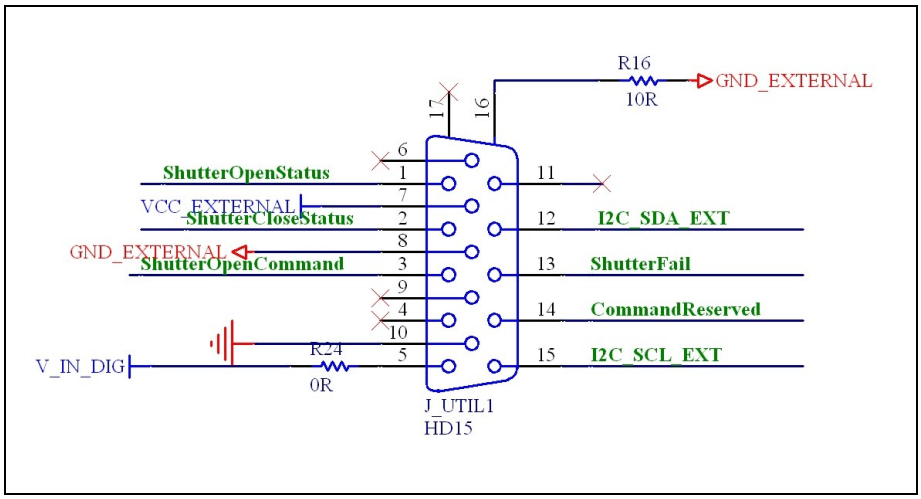

Figure 15 Connector Layout for optical Systems

2.1.3.1.3.2 Infrared Instruments

Three input signals supply the triggers to the read-out control system. The trigger signals are positive edge sensitive.

For wobbling mirror applications two signals are used. Trigger_Phase1 starts the readout on mirror position 1, Trigger_Phase2 the readout on mirror position 2.

An immediate trigger can be executed by the Trigger_immediate signal. Connector lay-out is shown in Figure 16.

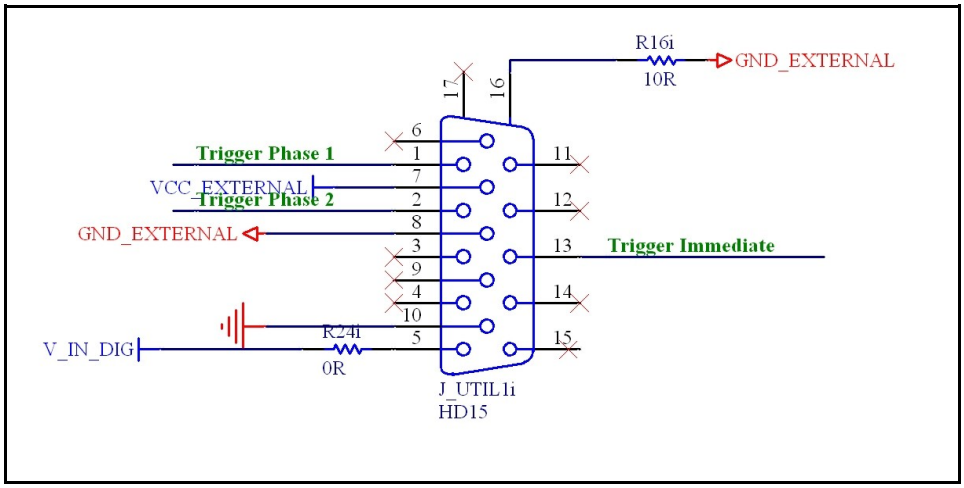

Figure 16 Connector Layout for IR Systems

2.1.4 Detector Front End Power Supply

Due to the different configurations, the weight and size of the power supply rack may vary significantly depending on the application and the detectors used. Figure 17 shows the standard configuration for small to medium size systems.

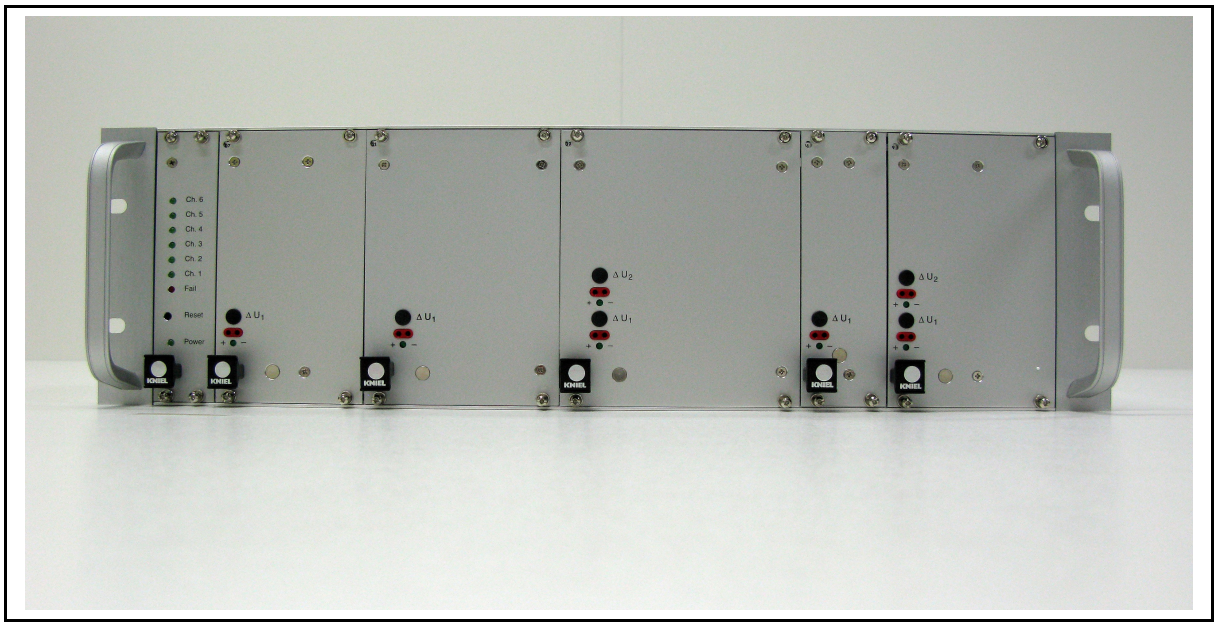

Figure 17 Power Supply

2.1.4.1 Size

The power supplies are mounted in an industry-standard 19-inch rack. The Vero KM6 II complies to DIN 41494 and part 5 of IEC60297–3. The rack is 3U high (132,5 mm), 84HP wide (427,58 mm) and 240 mm deep (without handles). For large systems, a rack of height 6U might be used.

2.1.4.2 Mass

The configuration shown in Figure 17 represents the setup of a typical power supply used in a small IR or CCD system composed of, e.g., one Basic Board and one AQ 32 Board. The mass of this specific power supply is 12.5kg and is given for crude reference only.

The exact values of the mass of power supplies for other NGC configurations need to be taken from the corresponding system documentation.

2.1.4.3 Voltages and currents

The power supply modules are commercial units by Kniel.

CDÜ 15.1,5	+/-15 Volt 2 x 1,5A
CLDC 5.5	5 Volt 2A
CDÜ 6.1,5	+/- 6 Volt 2 x 1,5A
CLDC 5.5	5 Volt 2A
CÜ 30.0,5	30 Volt 0,5A
CÜ 5.5	5 Volt 5A

Note that this configuration is representative of typical small to medium-sized CCD systems. Future detectors may require different or additional power supplies.

2.1.4.4 Connectors

The power input of the power supply rack is a standard IEC 3-pin C13 power lead. The output connector of the power supply is a 19-pin MIL-C-5015 connector from Amphenol (Part.-No.: 97B-3100A-22-14S).

2.1.4.5 Power Supply Cable

The power supply will be remotely located from the instrument and should be installed in a cooled cabinet. The maximum cable length between power supply and detector front end is 12 m (the shorter the better). Weight of cable is ~ 1Kg/m.

Figure 18 Power Supply Cable

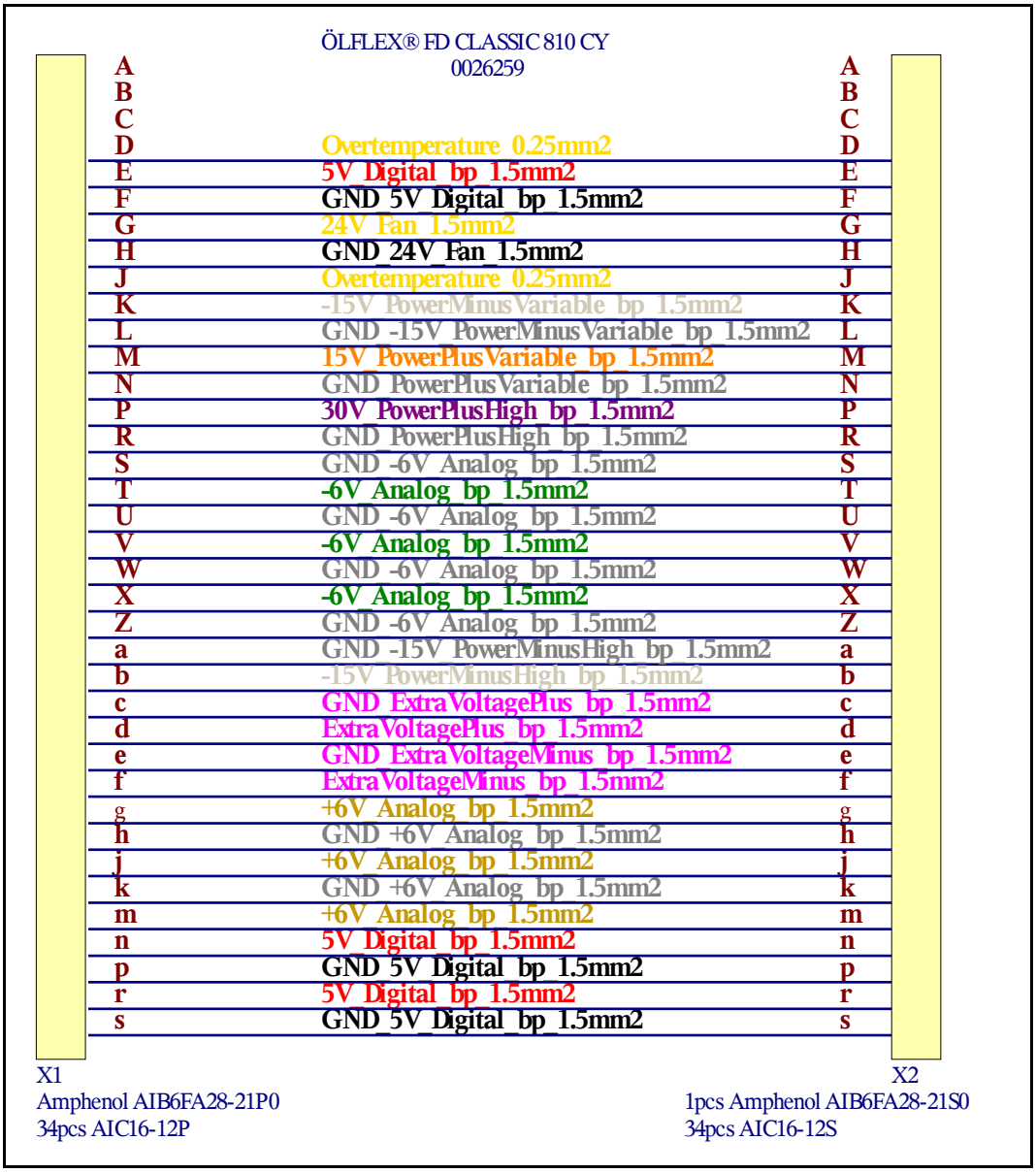

Figure 19 Power Supply Cable Pin-out

2.1.5 Detector Cryostat Cables

2.1.5.1 Infrared Systems

The present IR detector cryostat cable is shown in Figure 20.

Future cable systems will replace the three cryostat connectors with a single HIREL 128 pin connector (HIREL 74000Y-25E-35PN-565 N/R)

NGC System Cable Connectors:

CLOCK/BIAS - HD 62
VIDEO 4 - DB 25
VIDEO 32 - 2 x HD 44

IR Cryostat Cable Connectors:

BIAS - MS27467T15F35SA (66pin)
CLOCK- MS27467T19F35SN (66pin)
VIDEO - MS27467T21F35S (79pin)

Figure 20 IR detector cryostat cable

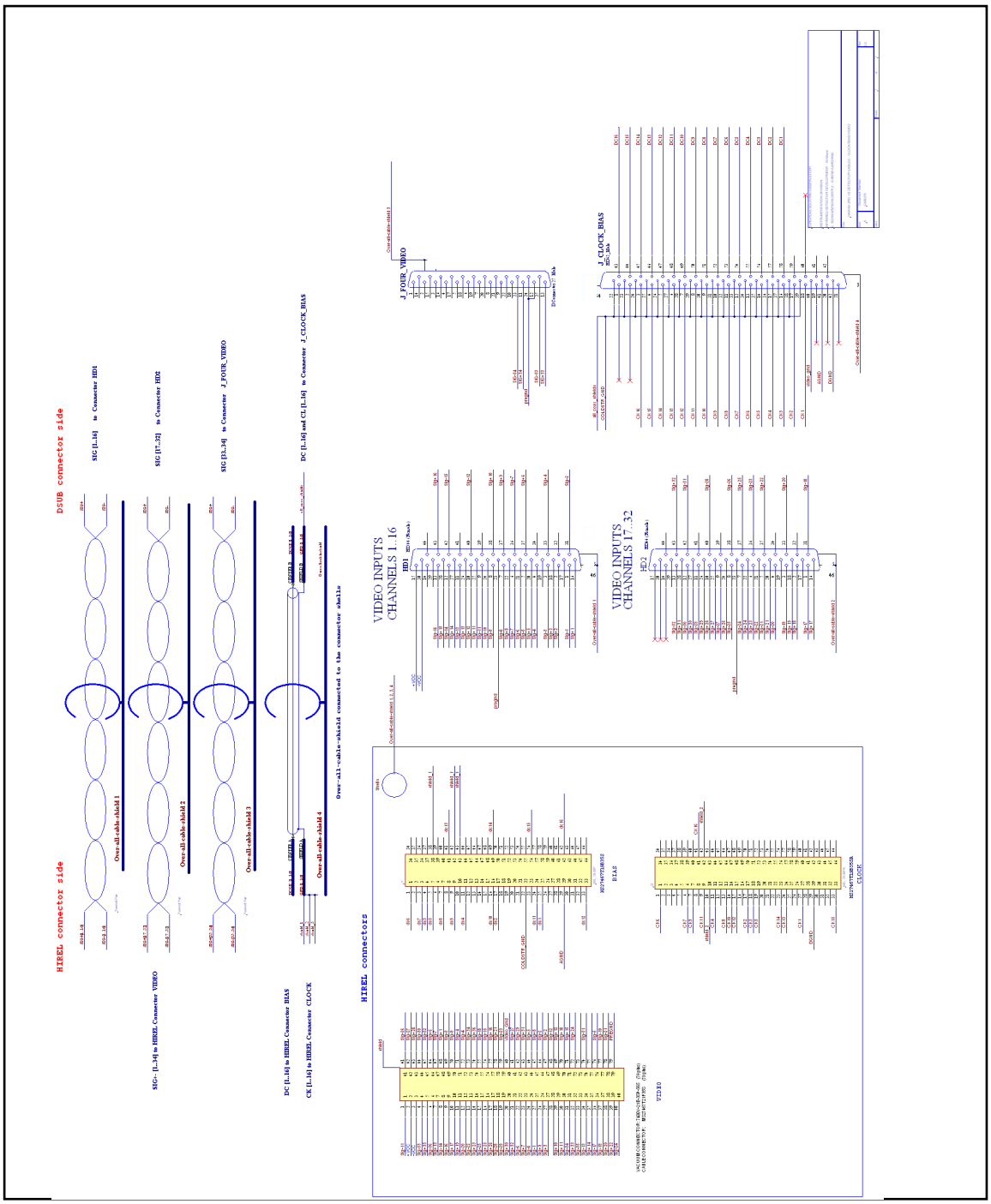

Figure 21 Triple-connector cryostat cable for 32 channel system

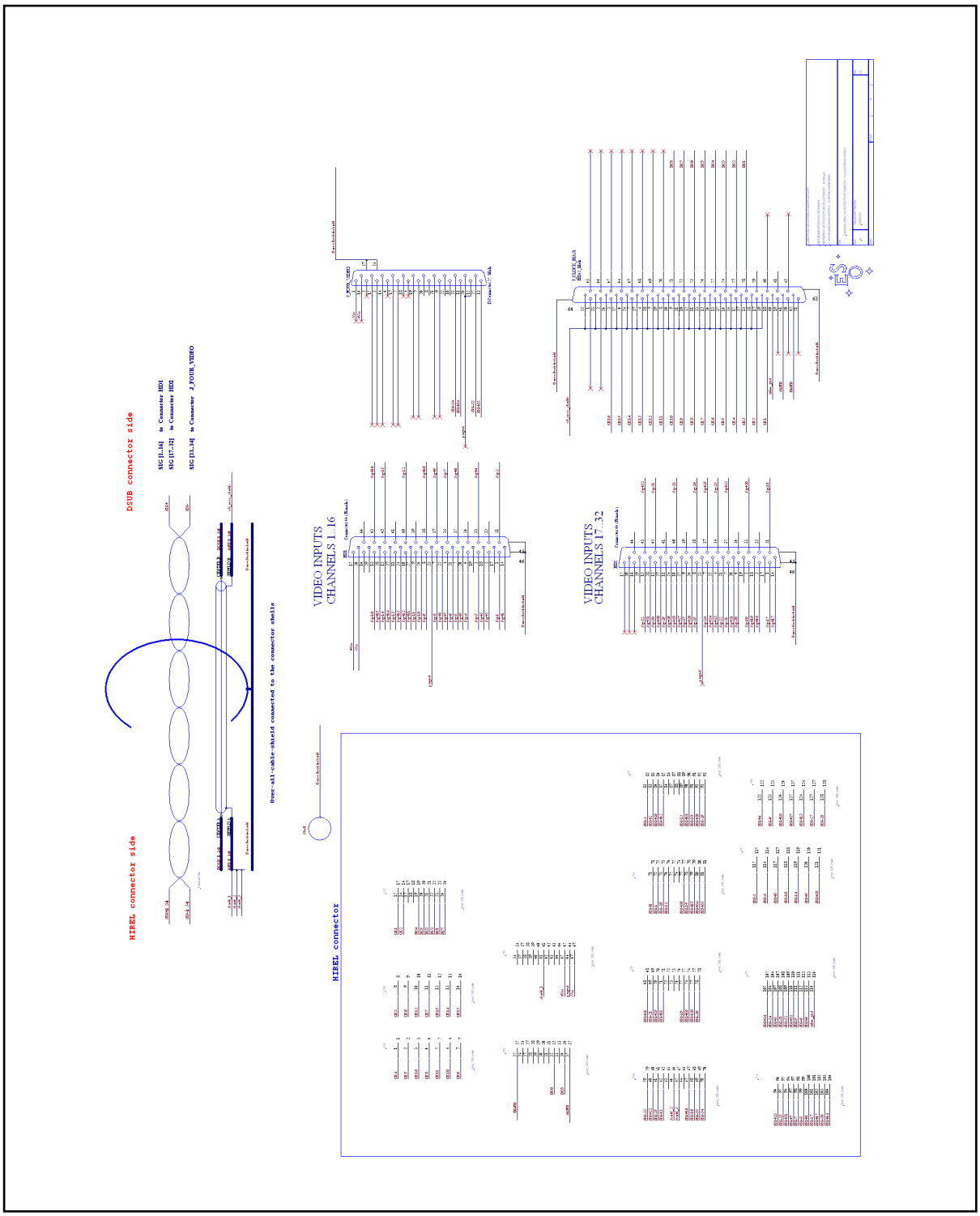

Figure 22 Single-connector cryostat cable for 32 channel system

2.1.5.2 Optical Systems

2.1.5.2.1 Video cable from cryostat to preamp

This is a 10 to 15cm cable connecting the cryostat to the preamp. This is cable and its layout are shown in Figure 23 and Figure 24, respectively.

Figure 23. CCD cryostat video cable

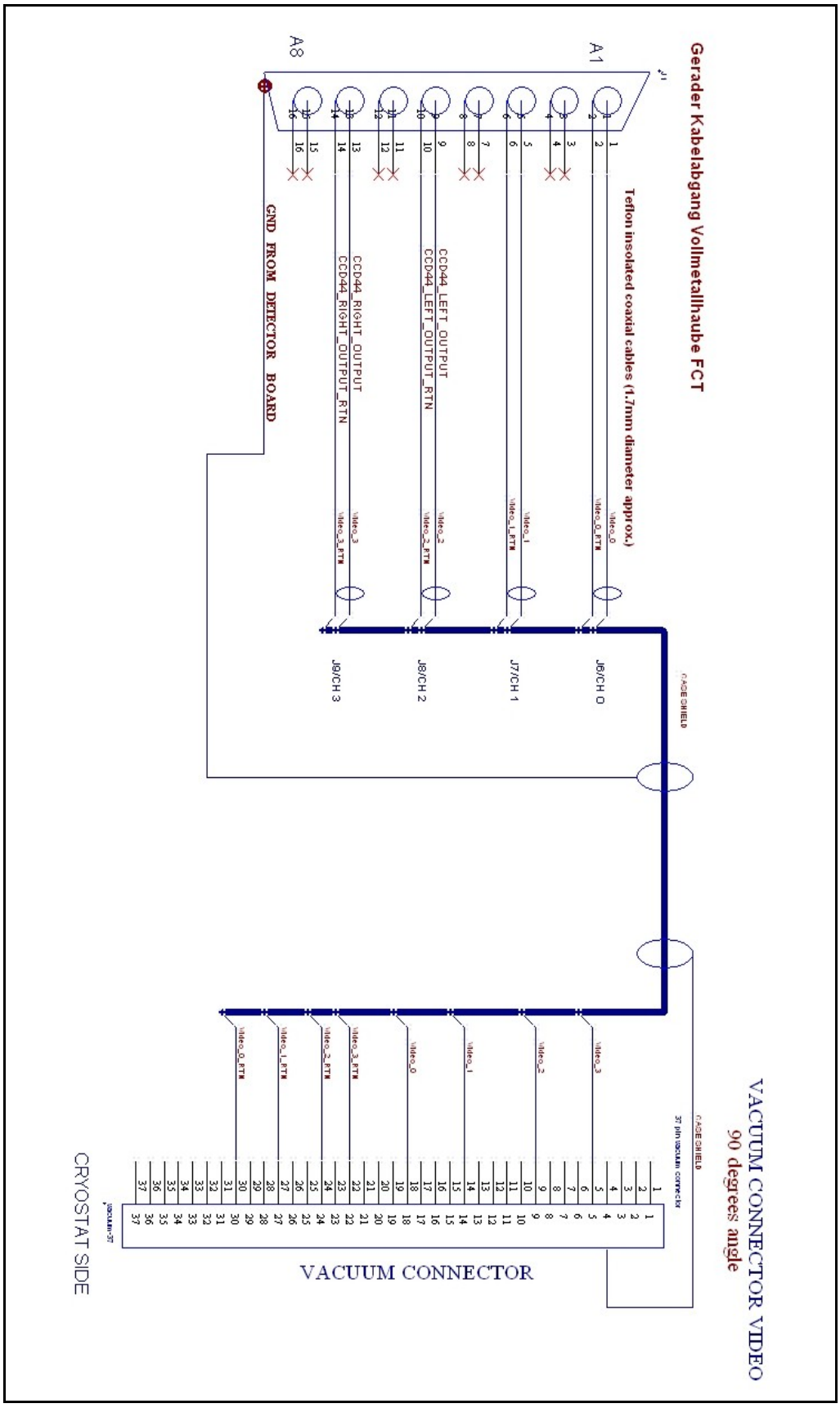

Figure 24. CCD cryostat cable layout.

2.1.5.2.2 Cable from DFE to CCD preamp

This is the cable connecting the preamp to the DFE. Its maximum length should be around 1m and it has a Sub-D25 connector at both ends. Its layout is shown in Figure 25.

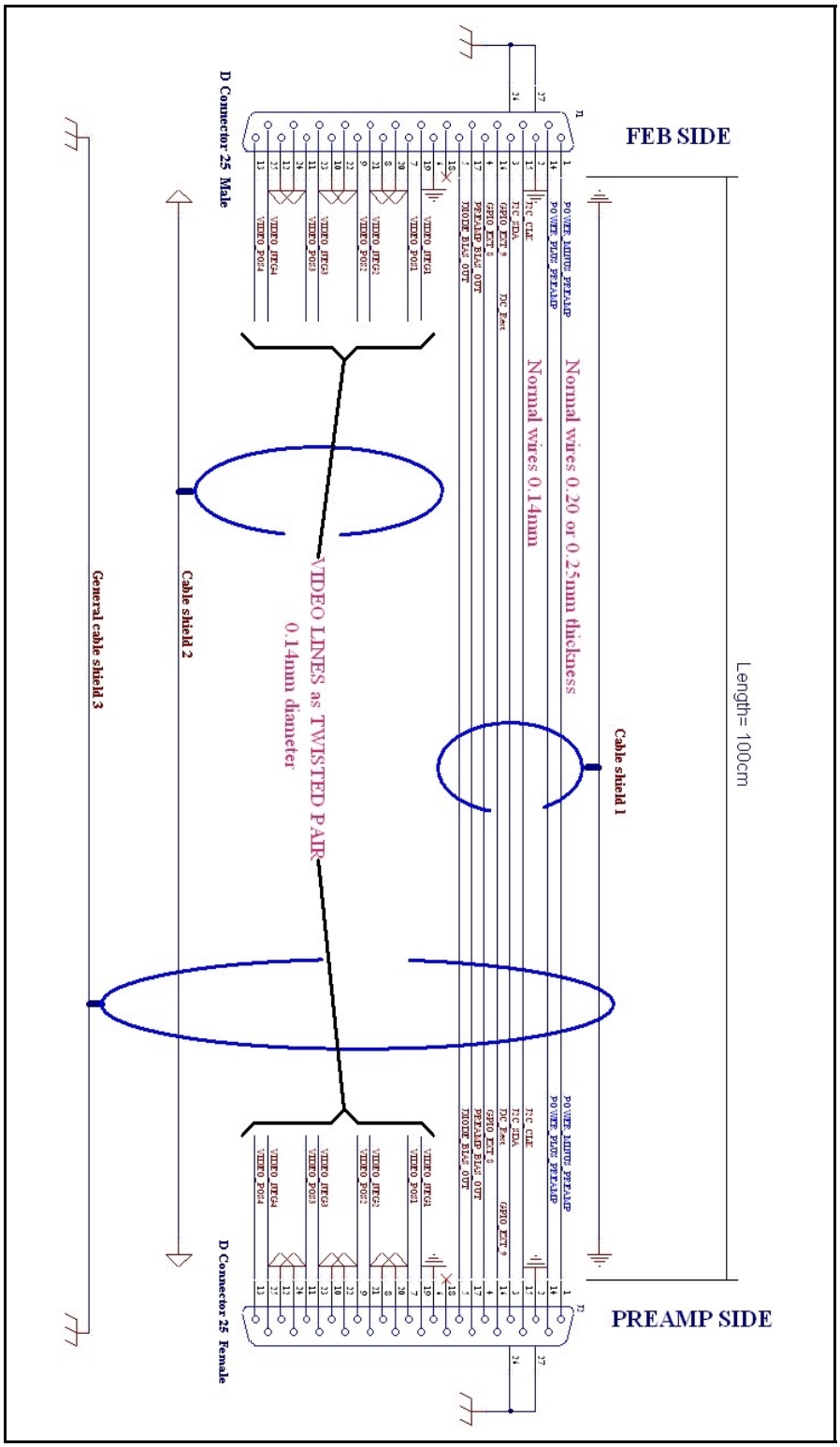

Figure 25. CCD preamp cable.

2.1.5.2.3 CCD clock and bias cable

This is a less than 2m cable going from the DFE to the cryostat. Its thickness is approximately 16mm diameter. This cable splits in one cable for the clock and for the bias, each of 10mm diameter. The clock and bias cable layouts are shown in Figure 26 and Figure 27, the cable itself in Figure 28.

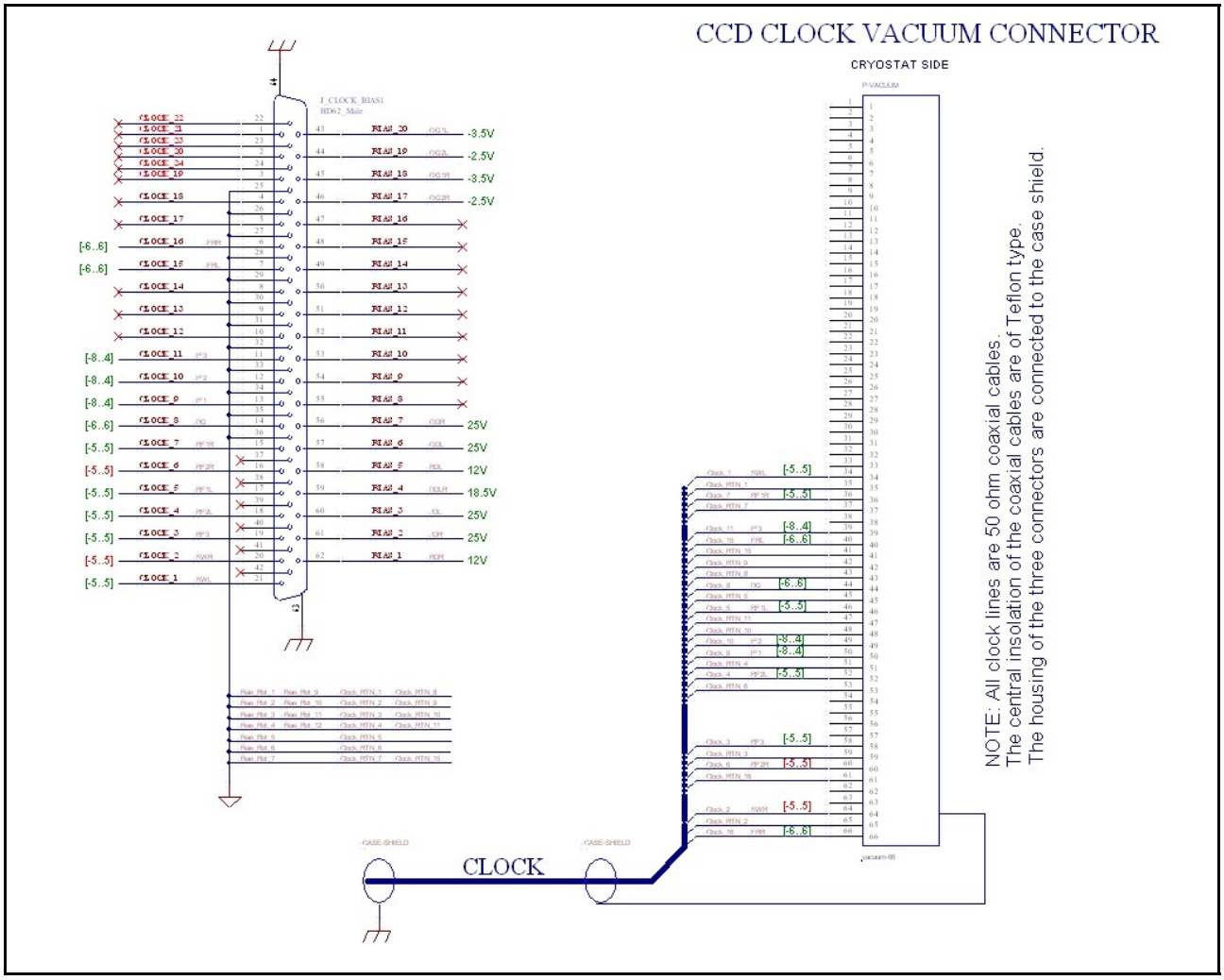

Figure 26. CCD clock cable.

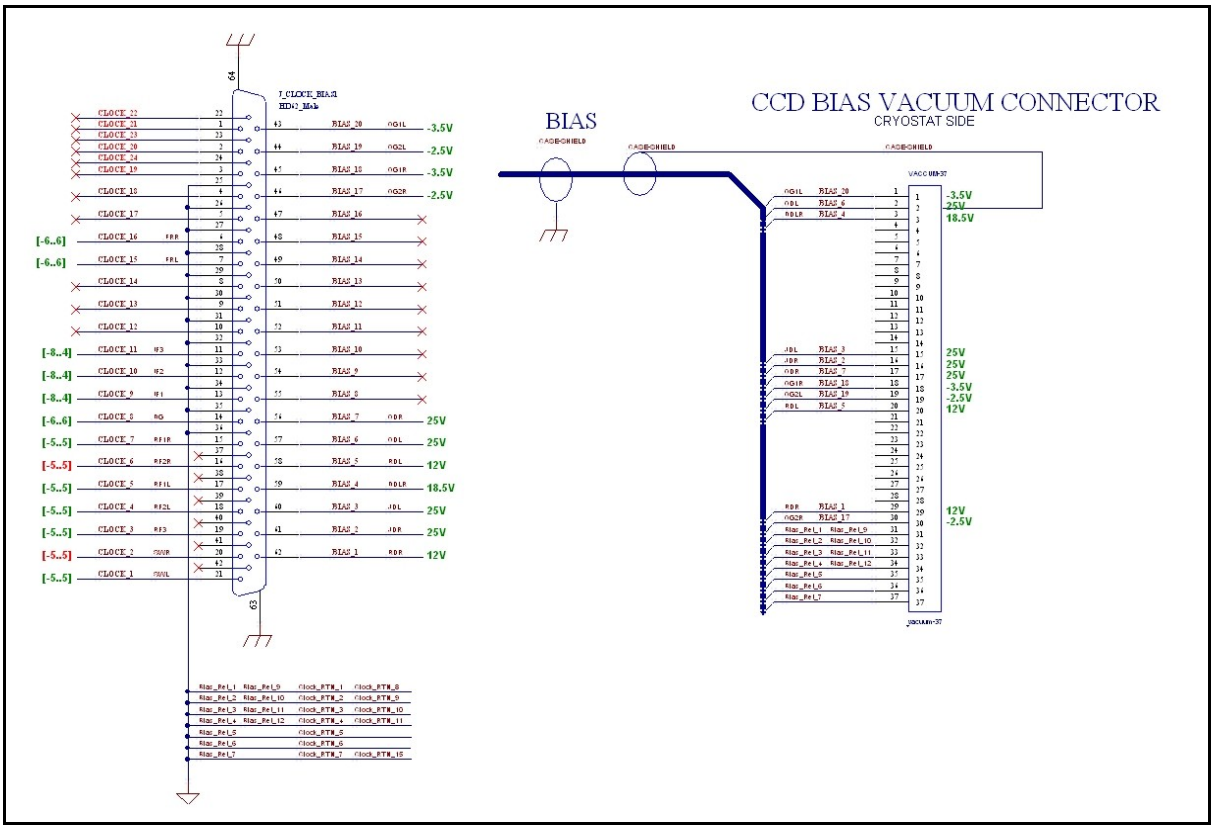

Figure 27. CCD bias cable to the cryostat.

Figure 28. Clock and bias cable for CCDs.

2.1.5.2.4 Shutter cable

This cable connects the HD15 connector on the FEB transition to the shutter and is a standard VGA cable. Its thickness is 9mm diameter approximately.

2.1.6 Detector Preamplifier

2.1.6.1 Infrared Systems

Preamplifier located inside cryostat.

2.1.6.2 Optical Systems

The preamp for CCD is located between the cryostat and the DFE. It features 4 video channels with16 software selectable gains and 8 software selectable bandwidths per channel. Its outer dimensions are 100 x 120 x 40 mm. The preamp is show in Figure 29.

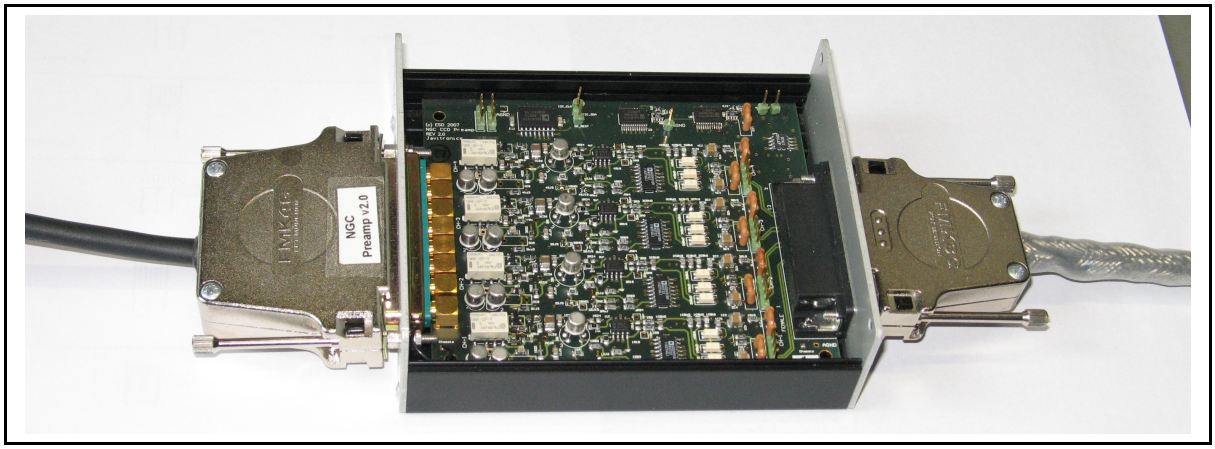

Figure 29. CCD preamp.