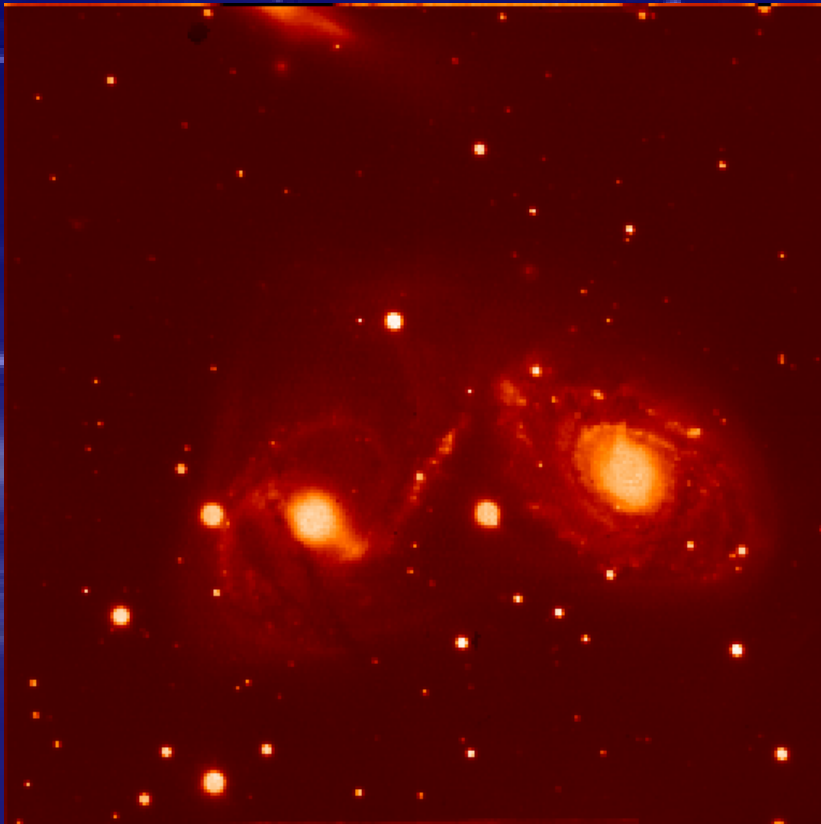


NGC

Detector Array Controller Based on High Speed Serial Link Technology

[IRDT and ODT]



First Light

PICNIC Array Mux

Image of ESO
Messenger Front Page

Conventional Approach : Acquisition System (IRACE)

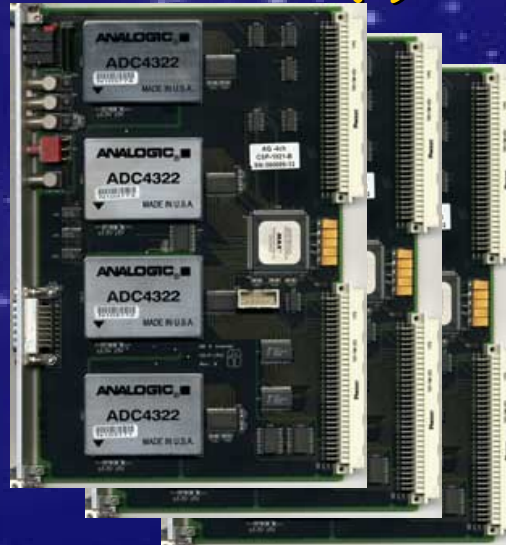


*PCI
Interface*

*Communication
and Data Transfer*



*Acquisition
Module(s)*



Sequencer

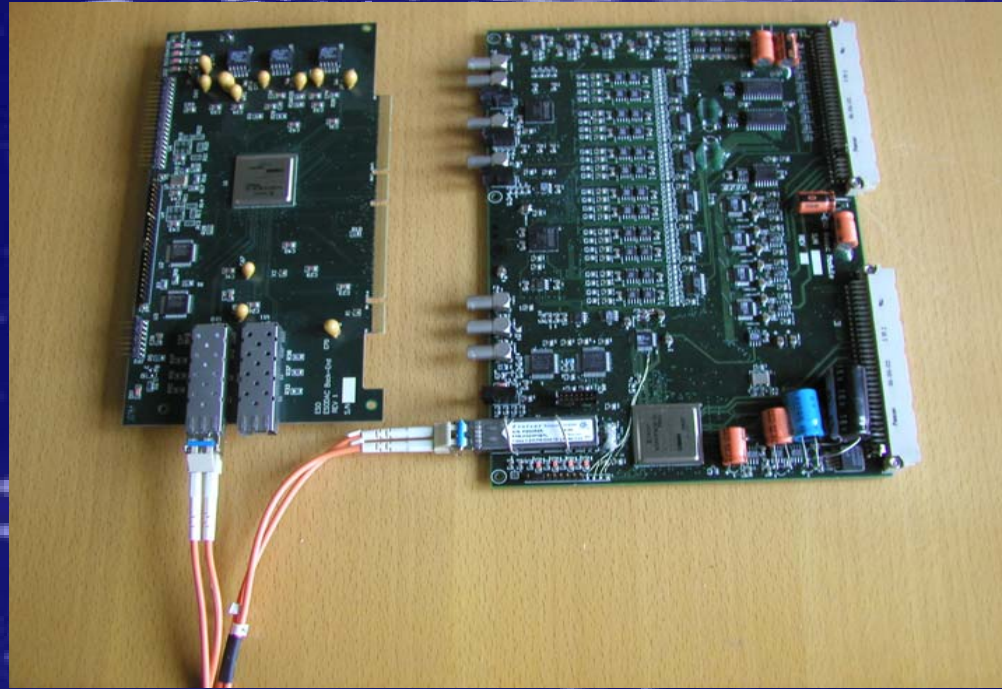


Clock and Bias



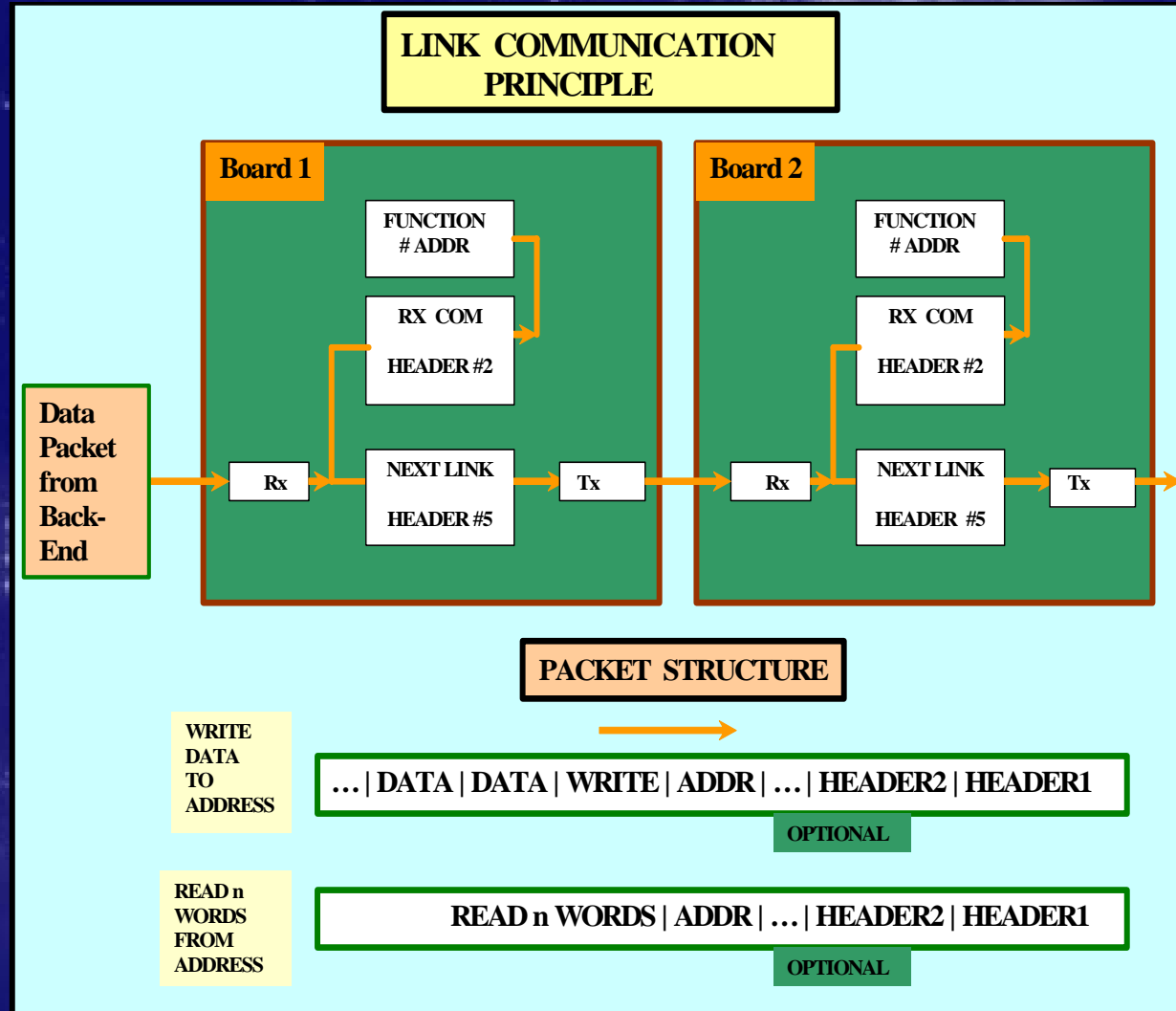
NGC Prototype - Minimum System Back-End and Front-End (Four Channels)

- NGC is a modular system for IR detector and CCD readout with a Back-end, a basic Front-end unit containing a complete four channel system on one card and additional boards like multi channel ADC units and more...
- There is no processor, no parallel inter-module data bus on the front-end side. Advanced FPGA link technology is used to replace conventional logic
- Connection between Back and Front-end with high speed fiber links at 2.5GBit/s
- Connection between Front-end modules with high speed copper links at 2.5GBit/s.
- Power Consumption on this Front-end is less than 10 Watts
(Excluding power supply)
- This Front-End system does not require big cooling boxes



Communication and Data Transfer

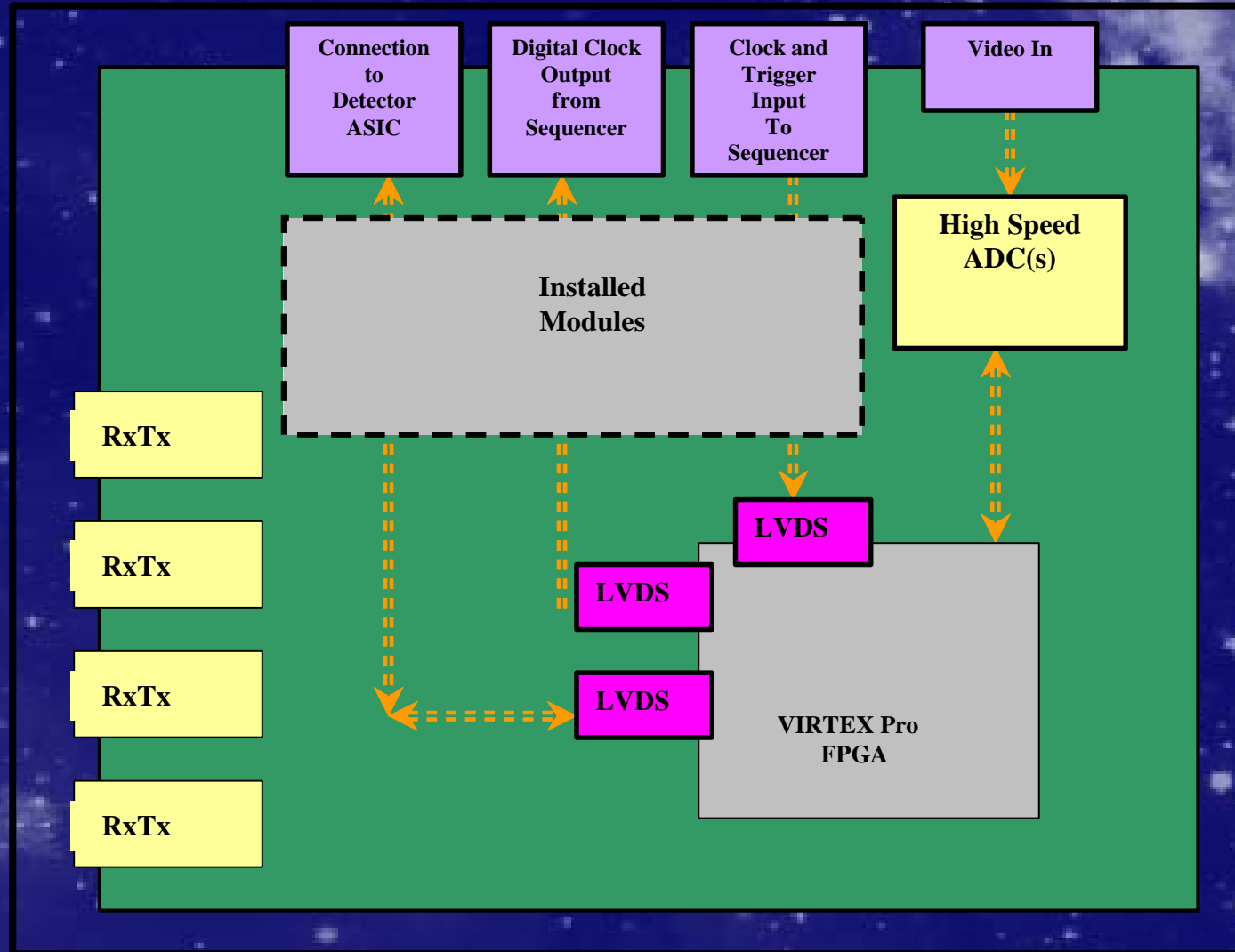
- Communication and data transfer is handled with the Virtex Pro FPGA's Gigabit transceivers
- The communication between all system modules is based on packet transmission over serial links
- A packet structure is defined to address a function (e.g. a register or memory in a front-end module) for read or write
- From the Back-End (PCI board) the packets can be routed to and through each board in the Front-End
- Data are routed with the same structure from the acquisition modules to the Back-End



Platform Design

- The Front-End System consists of a set of hardware modules like clock module, video data acquisition, telemetry, monitoring ...and VHDL modules for communication, data transfer, data capture and system functions like sequencer, telemetry, voltage set-up ...
- Different modules can replace presently installed modules without change in system connectivity and philosophy
- This makes it possible to buildt in a short time a new system for completely different applications

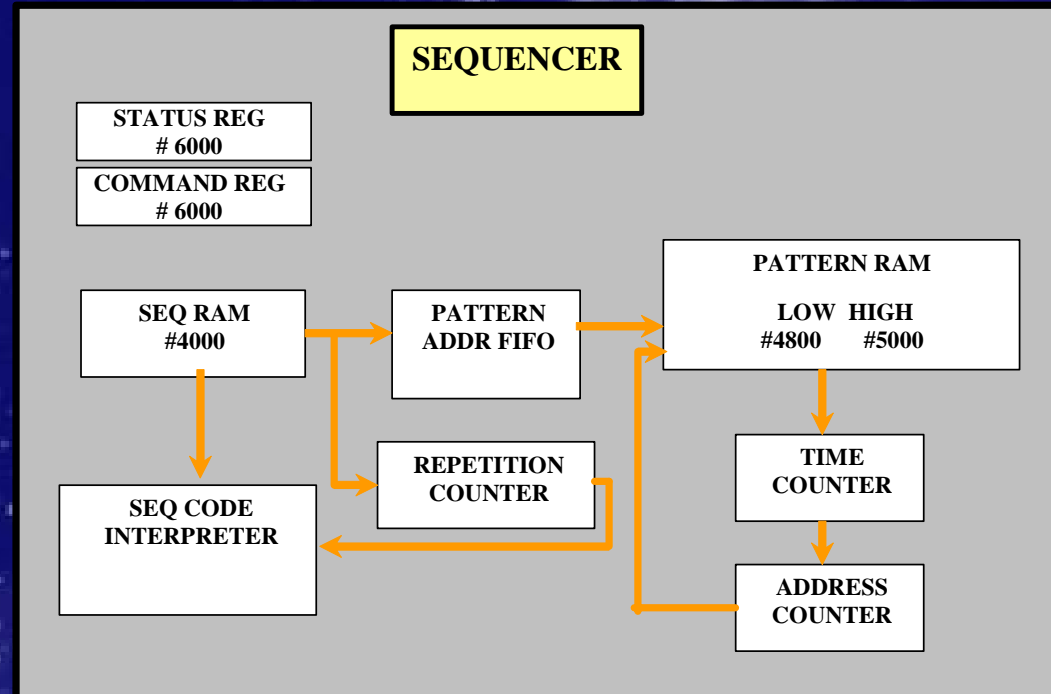
Platform for Acquisition Modules



Front-End Basic Board Sequencer Module



- Sequencer is completely contained within the FPGA
- 100MHz design = 10ns resolution
- Firmware interpreter for Sequencer Codes within the FPGA
- Galvanic isolated high speed trigger input and control outputs



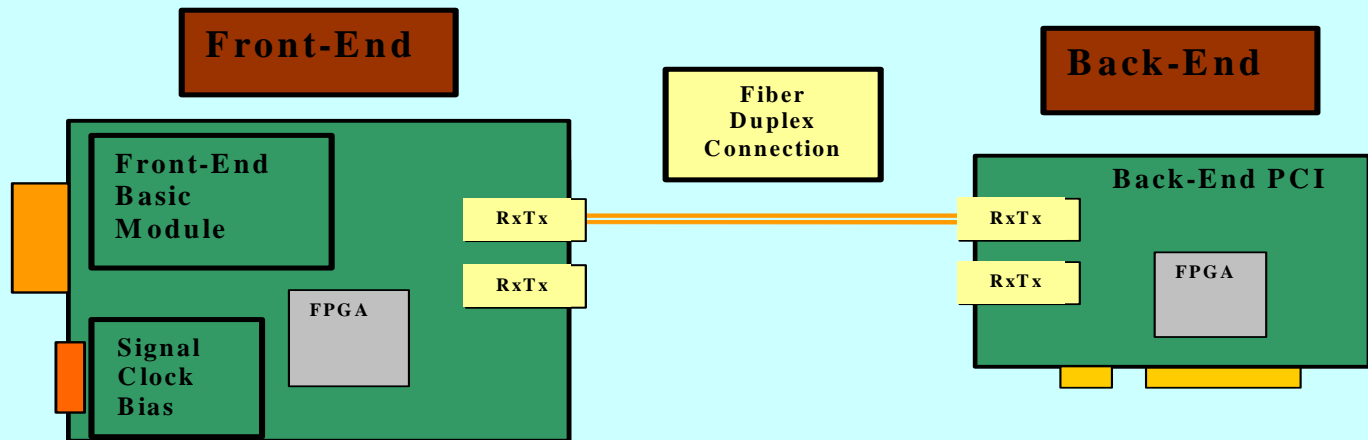
Sequencer Codes

- 000 Stop Interpreter → Stops Pattern Interpretation
- 001 EXEC Pattern < Number of Pattern, Number of Repetitions >
- 010 LOOP < Number of Repetitions >
- 011 LOOP END
- 100 LOOP INFINITE
- 101 JUMP SUBROUTINE < Address >
- 110 RETURN SUBROUTINE
- 111 Reserved

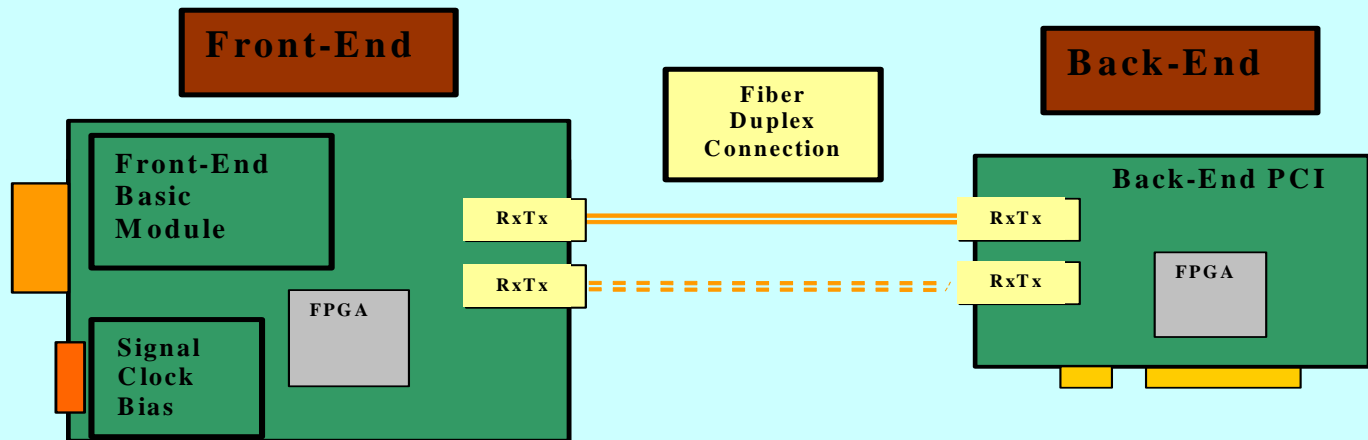
The background of the slide is a deep blue, starry night sky. It features numerous bright stars of varying sizes and colors, some appearing as soft, glowing clouds or nebulae. The overall effect is a rich, multi-colored field of stars, typical of a starry night sky.

Applications and Architectures

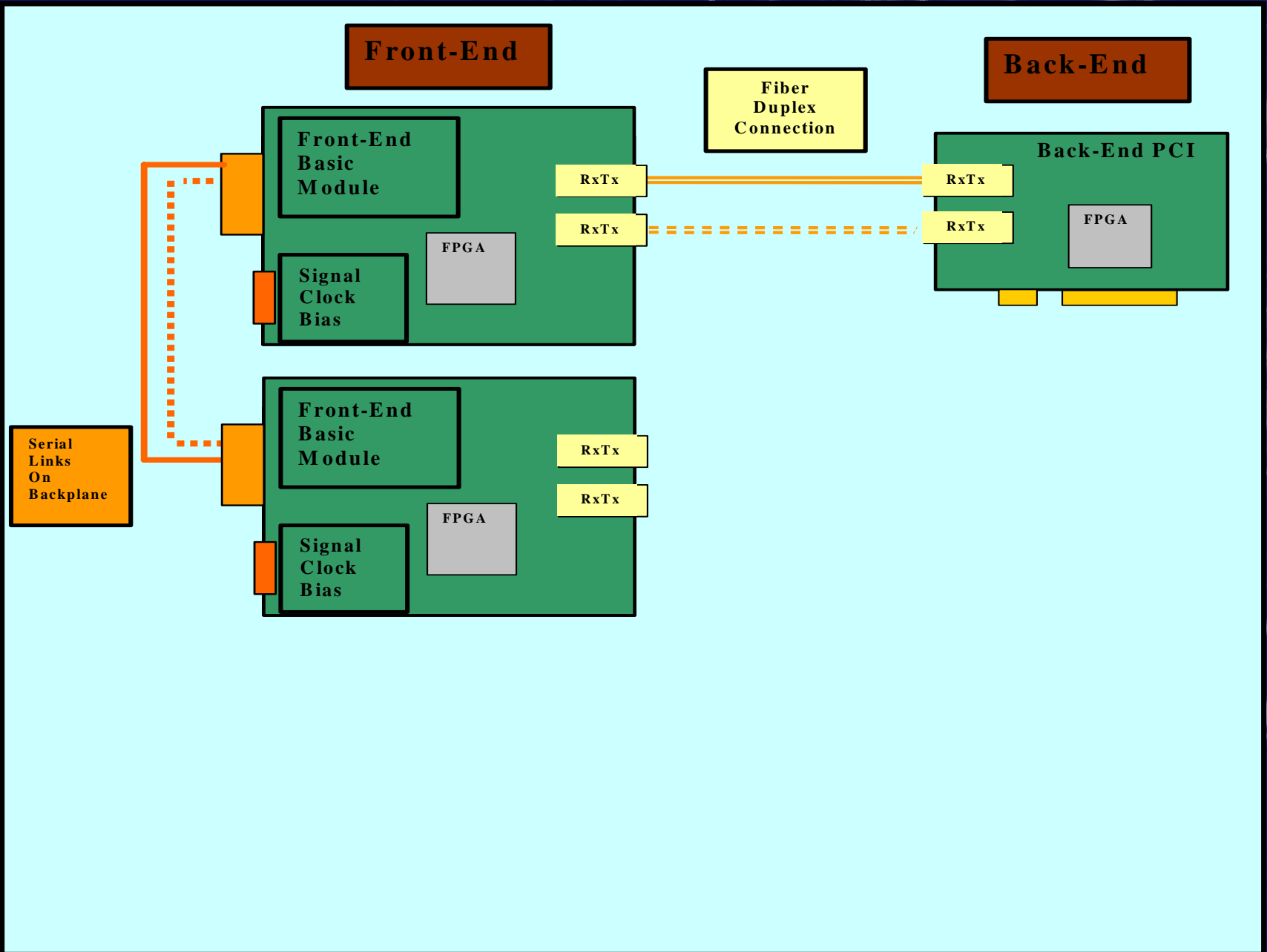
Basic System



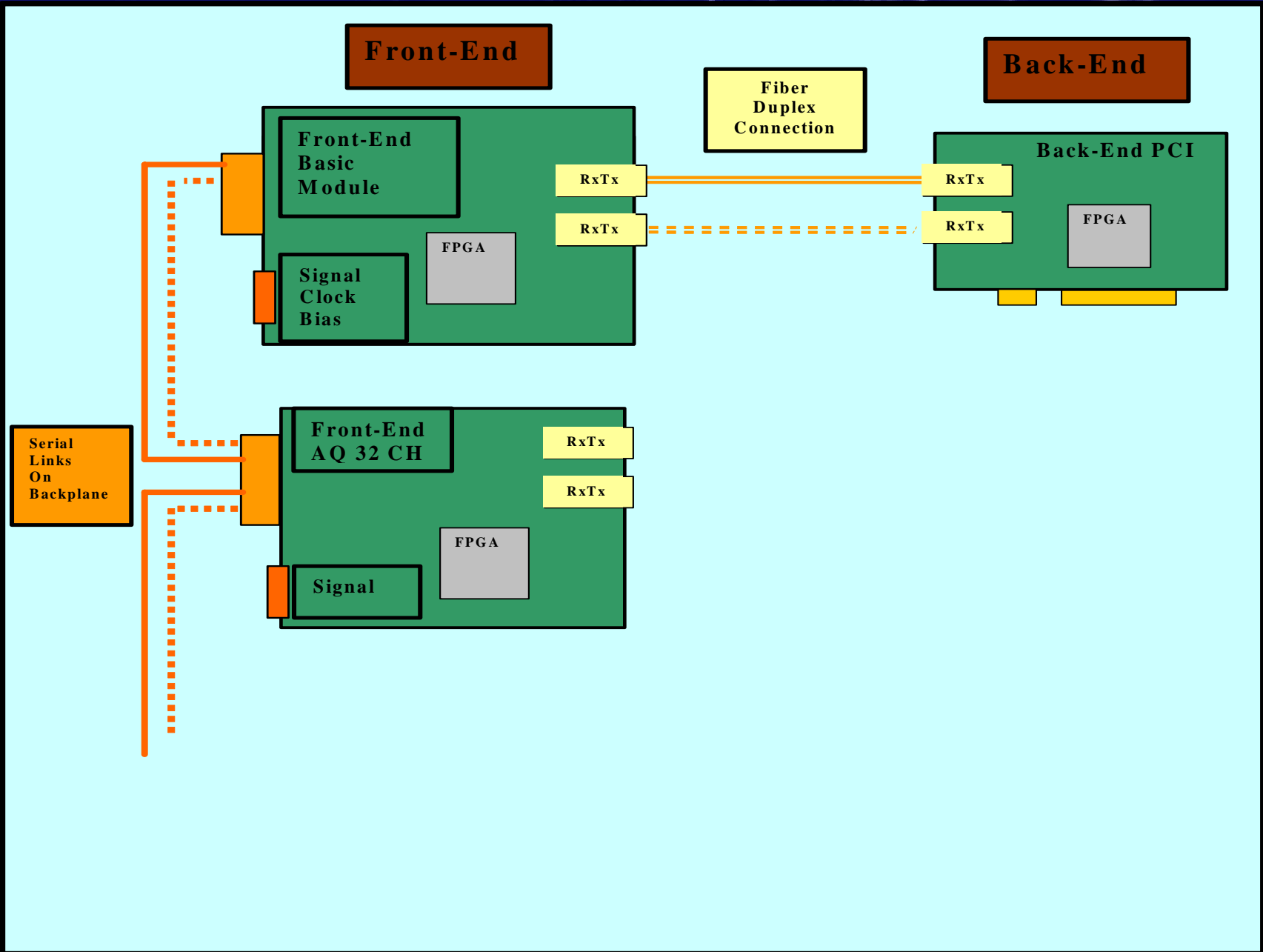
More Bandwidth



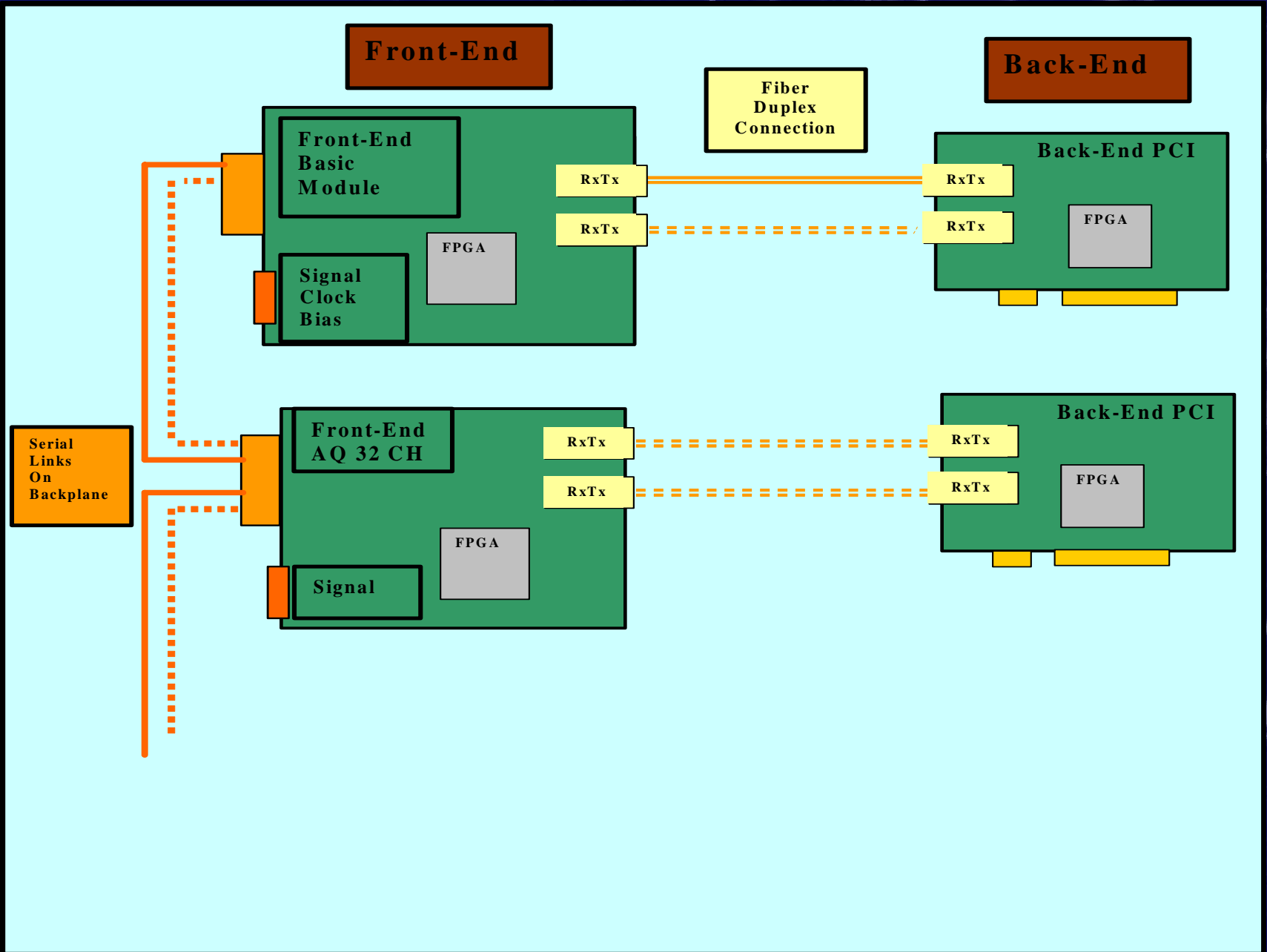
More Clocks, Biases / Two Detectors synchronized ...



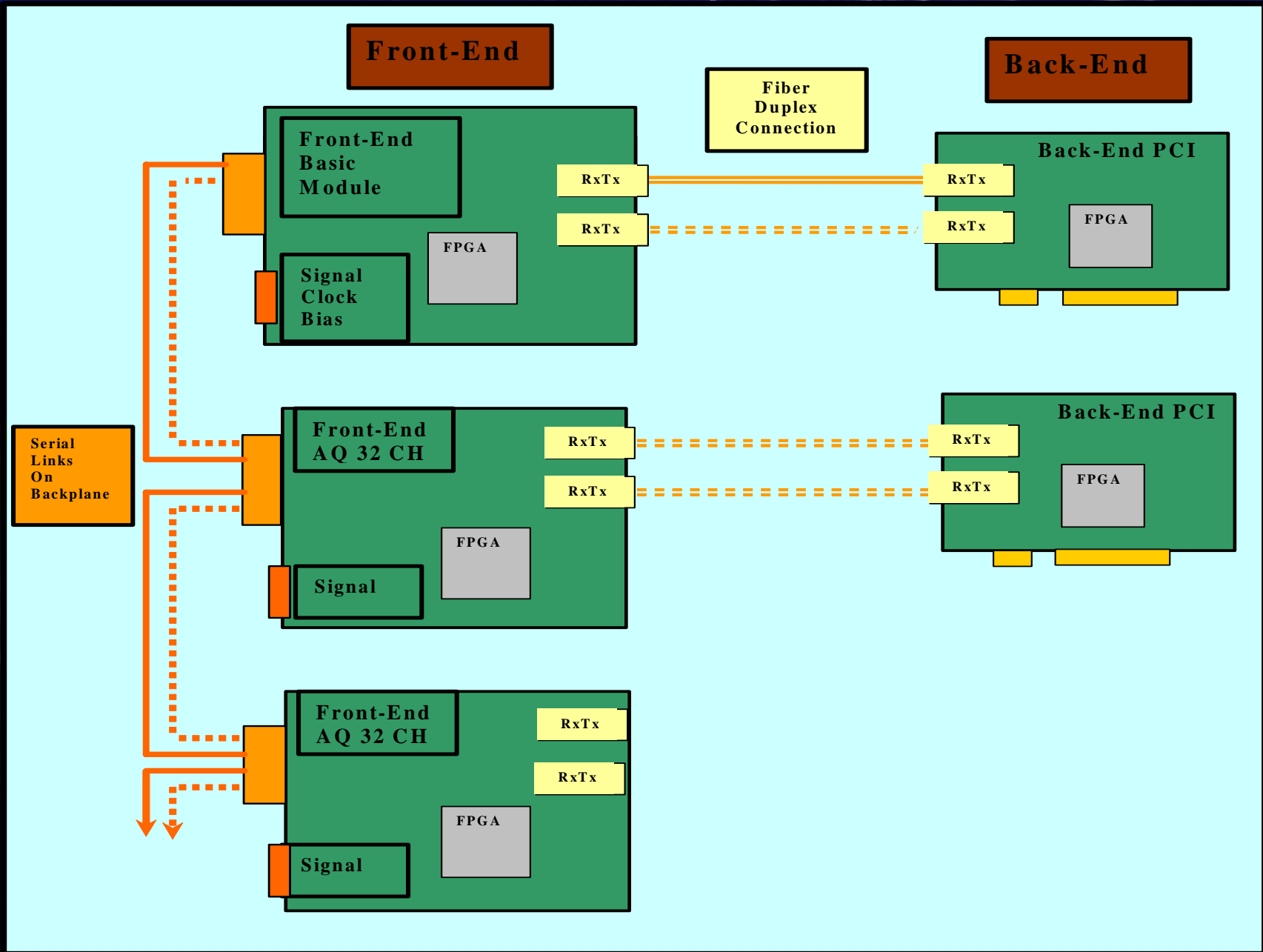
More AQ Channels



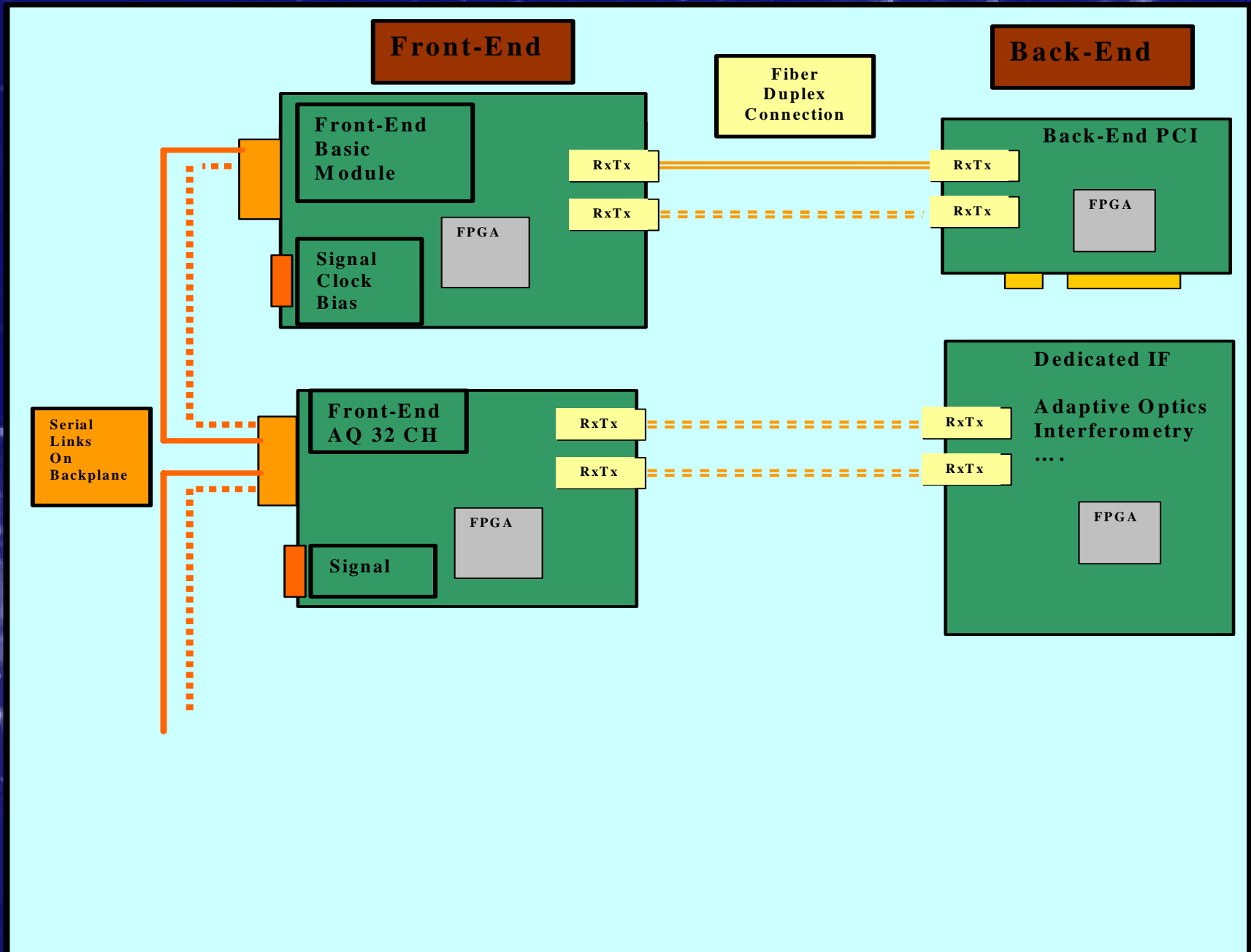
More Bandwidth and Different Routing



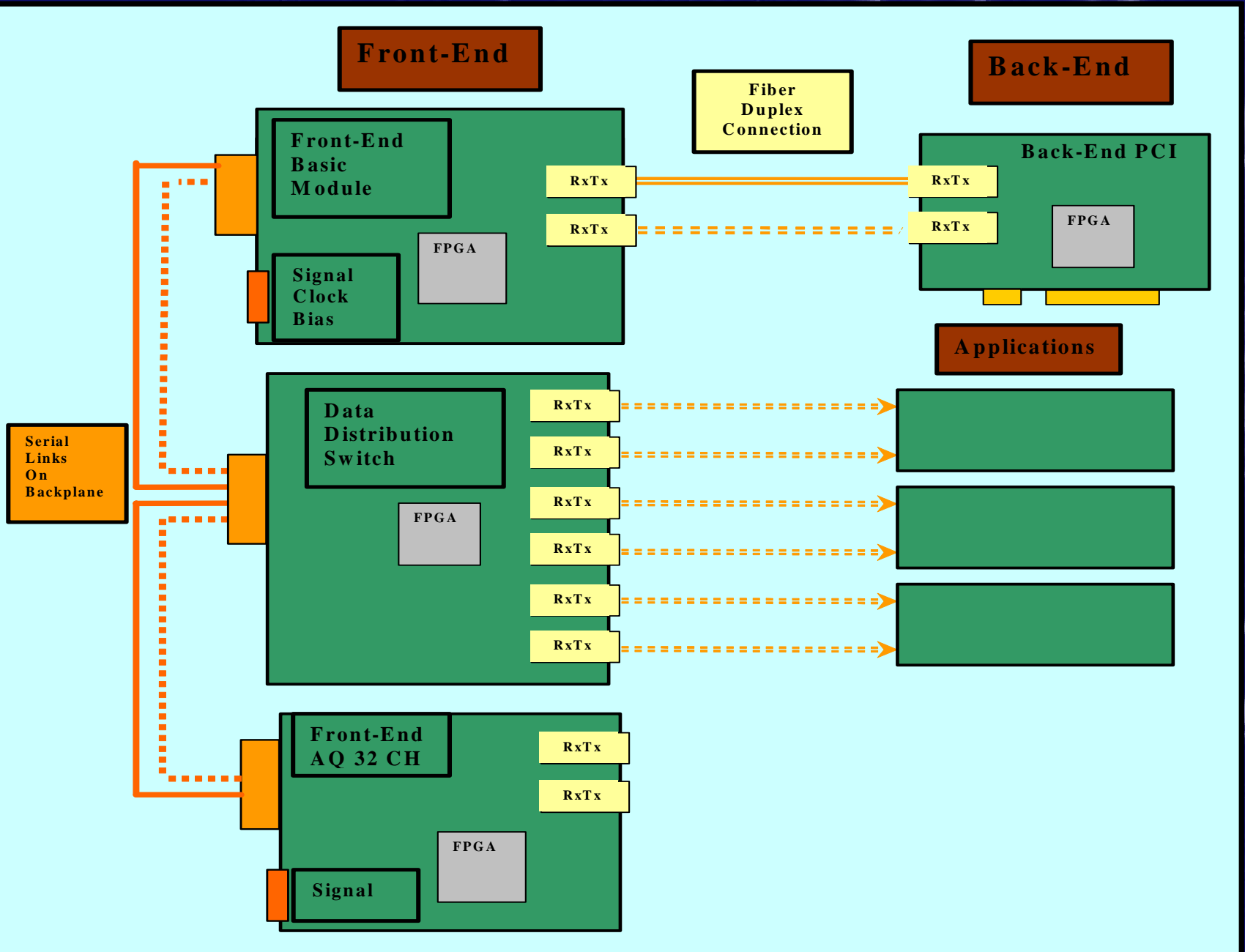
Even more channels



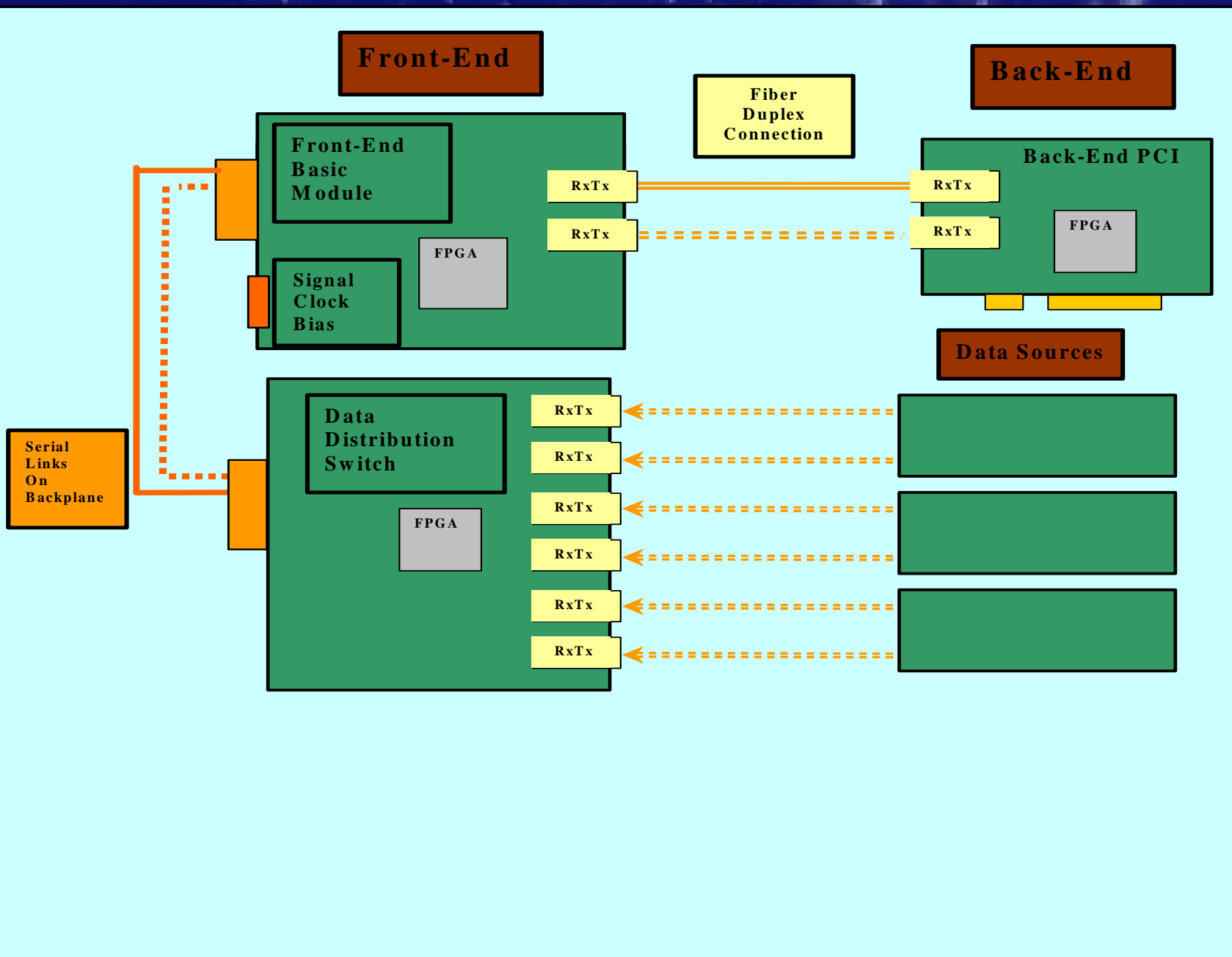
Route to Dedicated Interfaces



Distribute/Copy Data



Collecting / Routing / Preprocessing

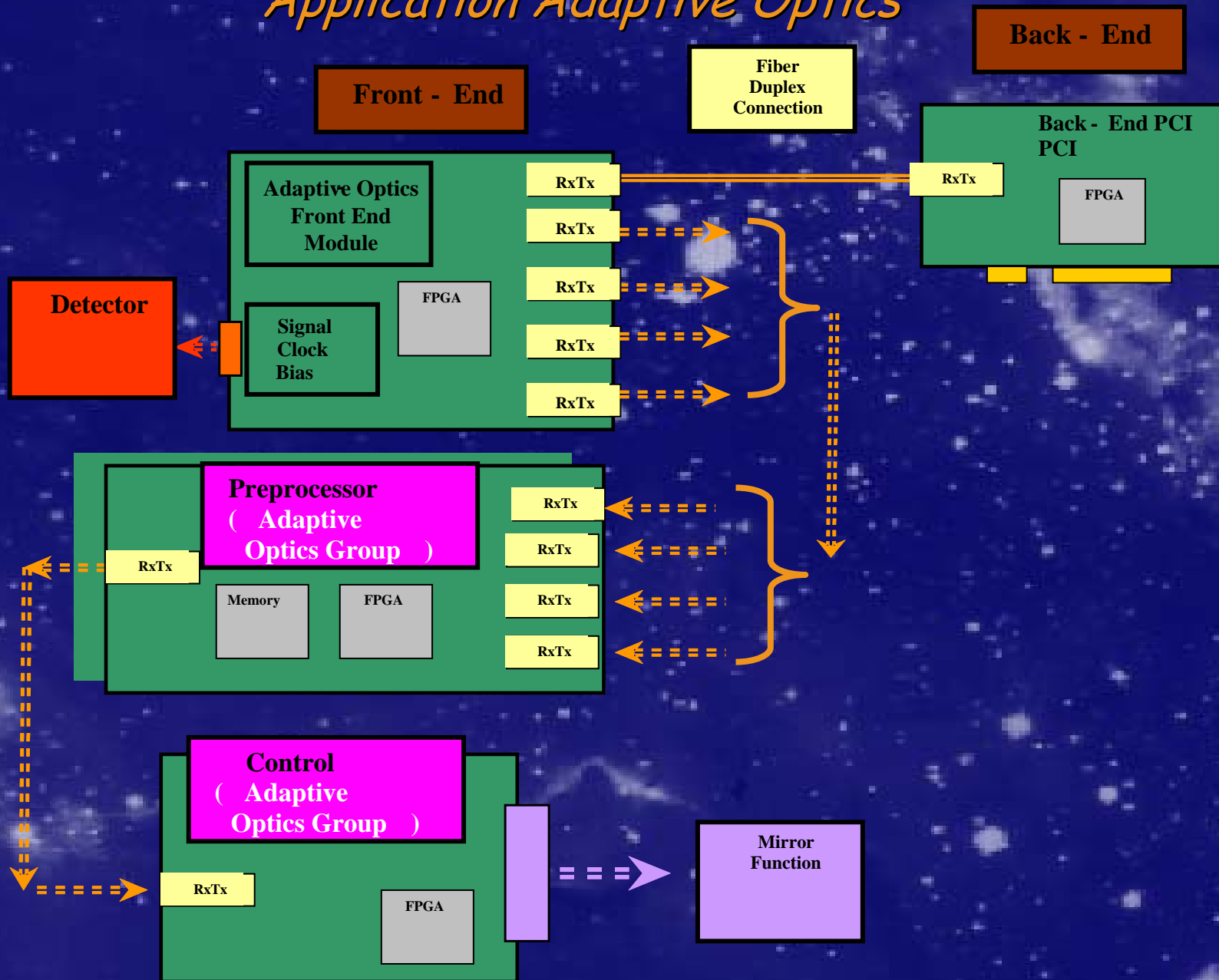


Outlook

Interface to Real Time Processor for Adaptive Optics and Interferometry ?

- Rocket I/O high speed (2.5 GBit/s) data links from acquisition modules can feed a fast preprocessor with data required for interferometry or adaptive optics
- The installed Virtex Pro contains already one Power PC on chip, multiple DSP's can be implemented for data preprocessing
- The most recent XILINX chips (V4) have even higher density and higher speed (400MHz). Links are compatible with links of Virtex Pro
<http://www.xilinx.com/products/virtex4/capabilities.htm>
- Data from link enter directly into FPGA memory, ready for processing
- Because the only input to the board is the data fiber, the board(s) can be installed close to the function
- Routing of acquisition data can easily be accomplished
- VME is no more needed !

Application Adaptive Optics



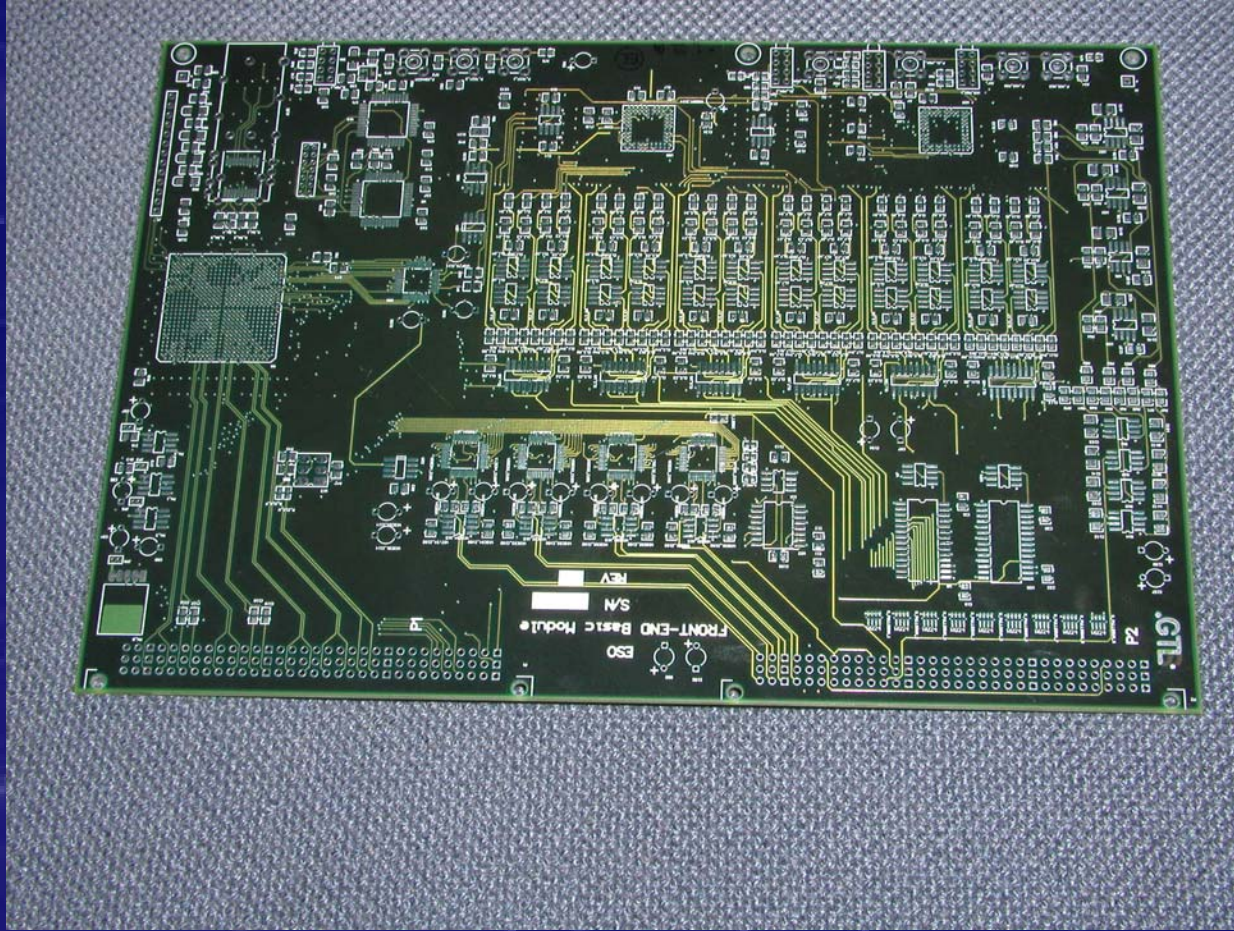
*Engineers
Bad Days*

or

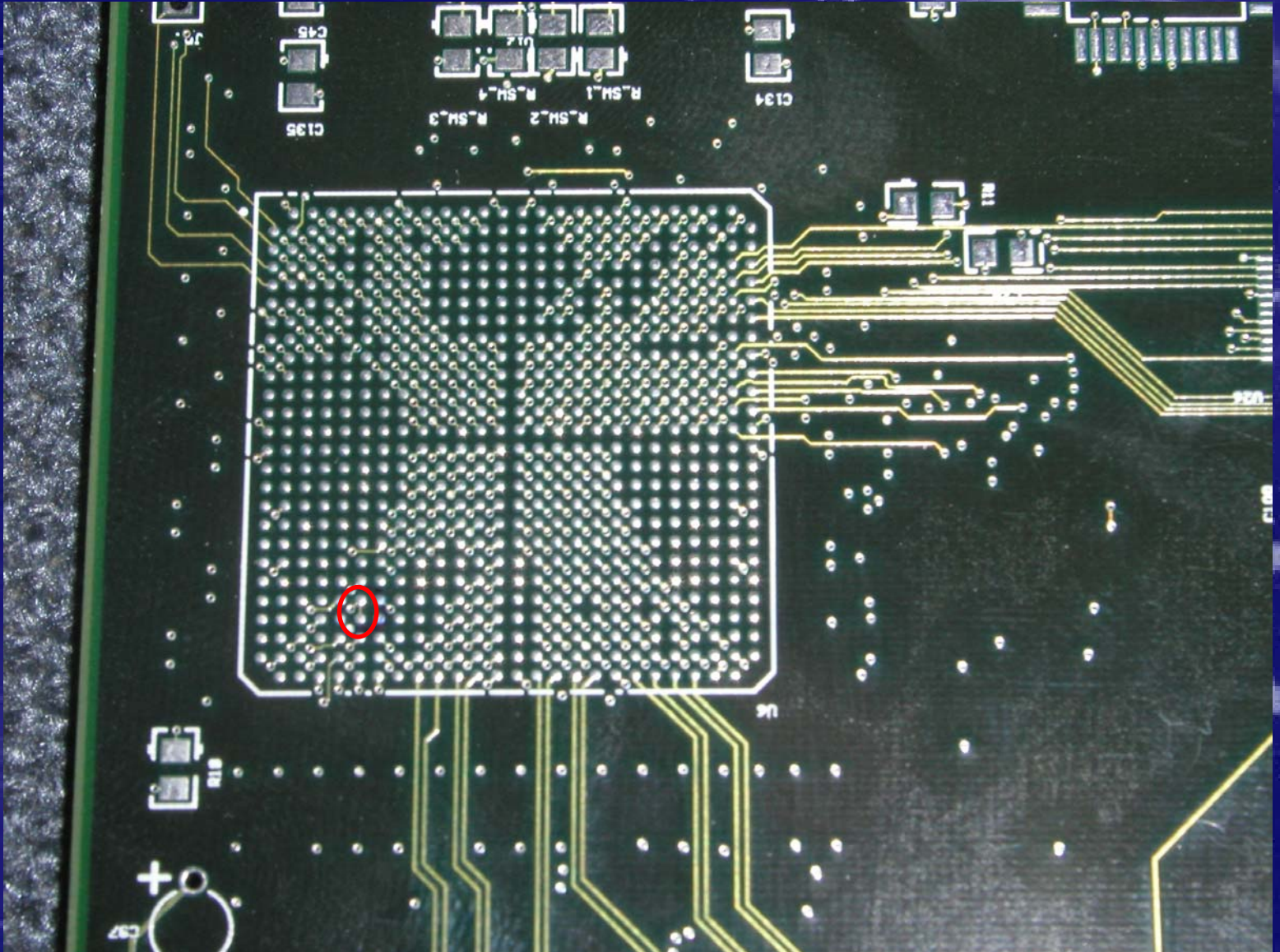
*The Real
World*



*How many Errors will be on ?
It's a 10 Layer board with BGA's !*



Virtex BGA - One Connection too much



Virtex BGA - Missing Connection

