NGC
DETECTOR ARRAY CONTROLLER BASED ON HIGH SPEED SERIAL LINK TECHNOLOGY

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Abstract: Progress in FPGA technology made it possible to build a very compact, versatile, low power detector array controller based on high speed serial link technology. All data and communication transfer between back-end and front-end and within the front-end run over high speed serial links with transmission rates of 2.5 GBit/s. The serial-bus architecture offers high performance and system scalability for modular controller set-up.

Key words: detector readout electronics, data acquisition system, focal plane arrays

1. INTRODUCTION

The conventional approach to build data acquisition systems is based on parallel bus architectures. A parallel bus in the front-end to connects the

different detector video data digitizing modules to a communication module for further transfer to the back-end. This bus already poses serious design challenges especially when the number of modules varies from system to system especially if the bus clock frequency is high. In addition for large systems the bus busy time may determine the maximum sample rate because during bus transfer conversion accuracy may be affected by coupling digital artifacts into the analog chain. For system setup and communication an additional structure is needed that adds complexity to the system. On NGC the parallel busses are replaced with high speed point to point serial links carrying data and communication transfers.

2. PROTOTYPE OF NGC

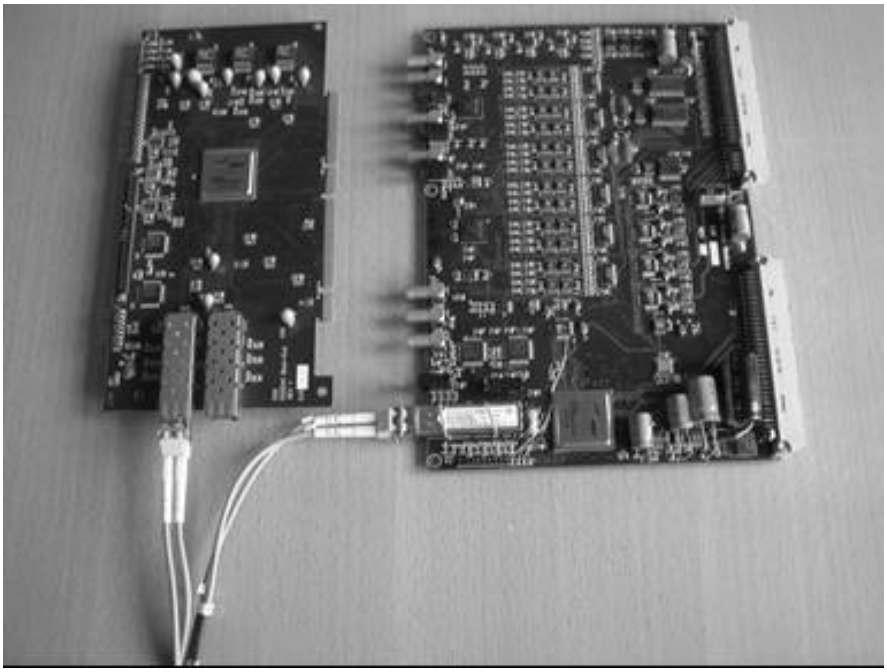

Figure 1. Prototype NGC

NGC is a modular system for IR detector and CCD readout with a Back-end ,a basic Front-end containing a complete four channel system on one card and in future additional boards like multi channel ADC units, routers and interfaces to applications like interferometry, adaptive optics and more.

There is no processor, no parallel inter-module data bus on the front-end side. Advanced FPGA (VirtexPro 2VP7) link technology is used to replace conventional logic. Connection between Back and Front-end is done only by fibers with high speed links (2.5 GBit/s). The modules inside the front-end are connected with high speed copper links (2.5 GBit/s). The links are derived from the Rocket I/O transceivers of the VirtexPro chip. The data rate on one channel between front and back-end is about 200MByte/s.The module functions on the boards are addressed directly from the FPGA without glue logic. Result is minimum disturbance for the anticipated low noise operation on the low level detector signals, small size and low power consumption. The power consumption of the basic front-end is less than 10 Watts (excluding power supply) so that this Front-End system does not require big cooling boxes.

3. BACK-END

All functions are based on the XILINX Virtex Pro FPGA XC2VP7 FF 672 .The back-end is a 64 Bit PCI board. The FPGA contains the PCI interface for Communication functions, the video data DMA channel and the RocketIO transceivers for link transfer. The interface from PCI to FPGA is without glue logic. PCI master (data) and PCI slave (communication)

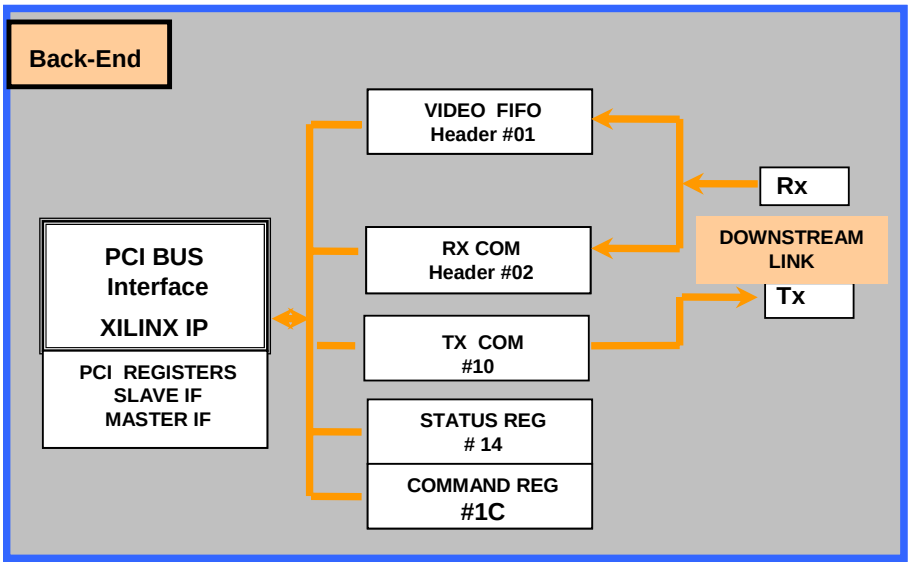

Figure 2. Back-End Block

interfaces are independent and can work concurrently. All communication and data transfers are on the serial links. Scatter /Gather DMA is used for data taking, all communication runs with a handshake protocol.

4. FRONT-END BASIC MODULE

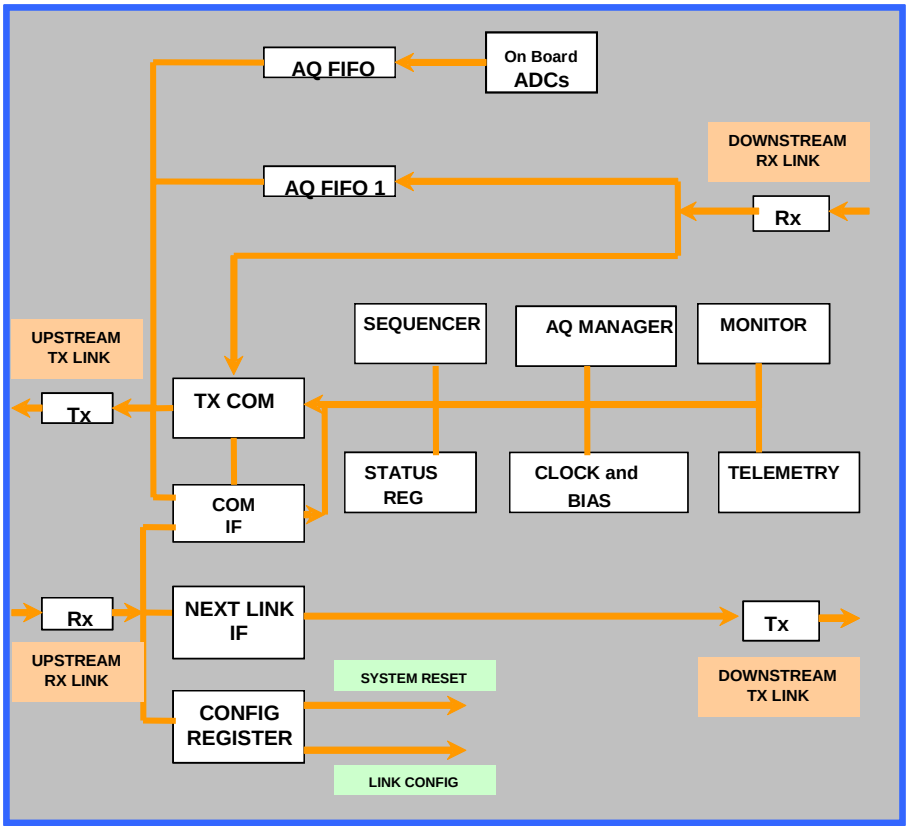

Figure 3 Front-End Basic Block

All functions are based on the XILINX Virtex Pro FPGA XC2VP7 FF 672 .The FPGA contains the link interface for communication and data transfer with RocketIO transceivers, sequencer, system administration, interface to acquisition, clock and bias, telemetry and monitoring. The board contains four ADC channels (16 or 18Bit with Analog Devices Pulsar ADCs), 16 clocks and 20 biases all remotely programmable, Telemetry with 16Bit accuracy, monitor outputs of video input, ADC input, clock signals, convert strobe and digital marker signals.

There are galvanic isolated trigger input and control output signals.
LVDS signals are provided for connection to detector ASIC's - all communication and data transfer to the back-end is handled with the same firmware used for conventional detector read-out.

5. PROTOTYPE SYSTEM NOISE

The Measurement on system noise looks promising. A double correlated readout with 100 Ohm terminated inputs shows 0.7 ADU RMS (readout noise * SQRT 2). The noise on a channel with 10KOhm termination (left upper quadrant) differs as expected (Figure 4).

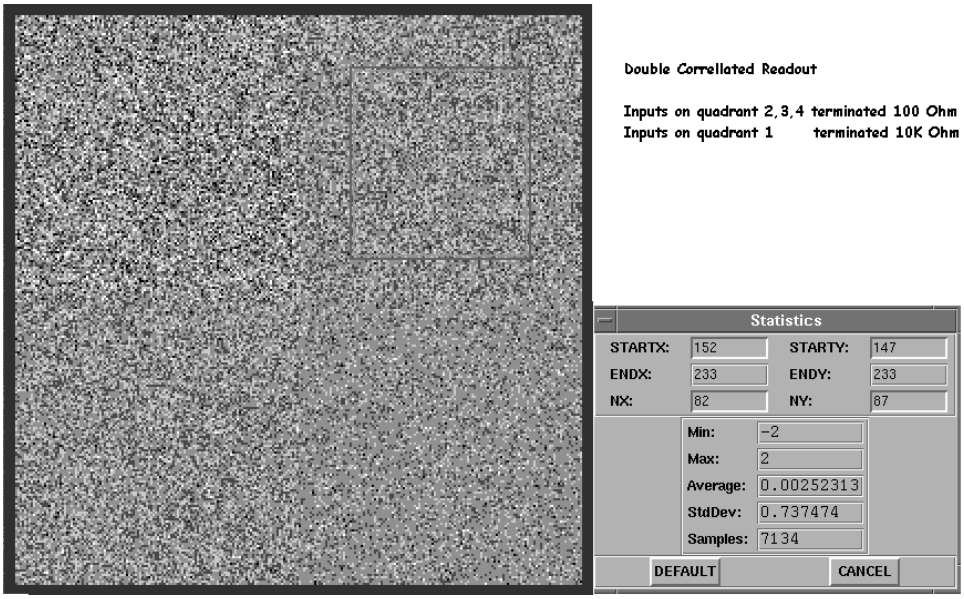

Figure 4. System Noise

6. APPLICATIONS AND ARCHITECTURES

The minimum system (Fig. 5) consists of back-end and front-end ready to read out a four channel IR detector or a CCD.

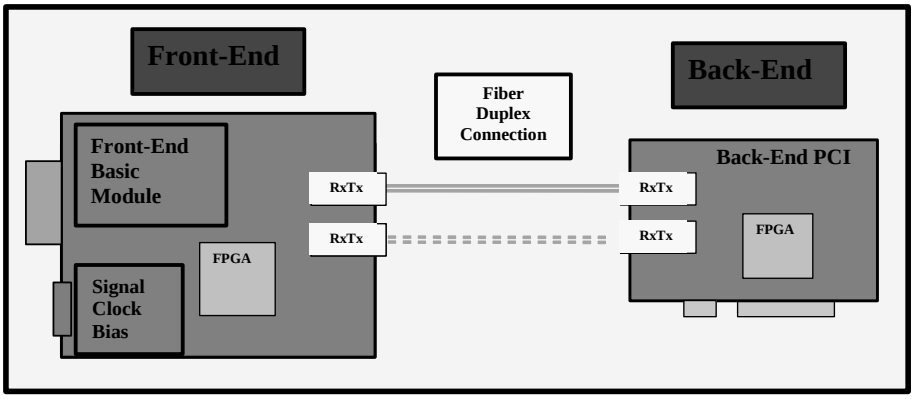

Figure 5. Minimum System

If more bandwidth is required an additional link can be added (Fig. 5). If more clocks/biases are needed or a synchronized read-out should be done of more than one or an additional/ different detector – this can be done by adding additional basic units (Fig. 6).

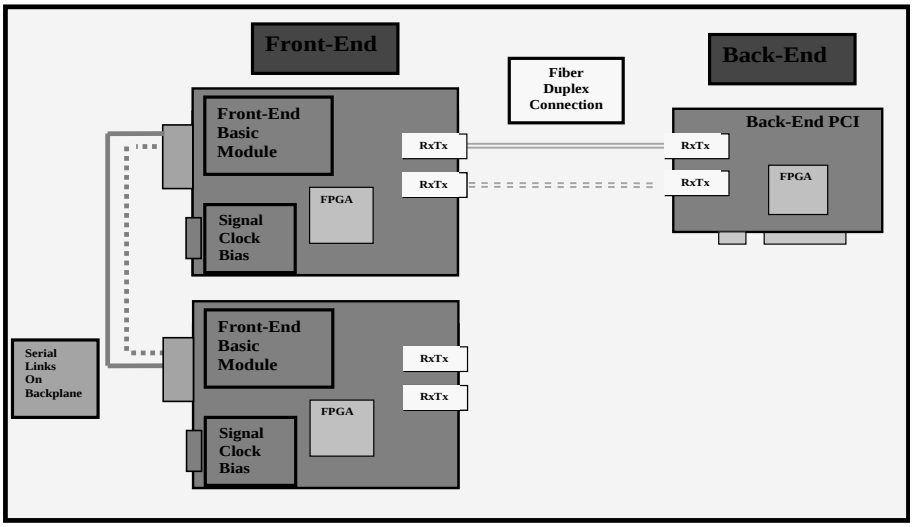

Figure 6. Synchronized Readout of Detectors

Multi channel applications for mosaics of detectors are easy to accomplish just by adding additional multi channel modules with serial links.

Applications like interferometry, adaptive optics or others can be connected with the high speed serial links. The big advantage is, that data

arrive with minimum latency directly at the processing node – the FPGA. There the implemented Power PC's or dedicated DSP's have direct access to the data buffers containing the image data. The processing node can be located remotely and close to functions like deformable mirrors or others (Figure 7).

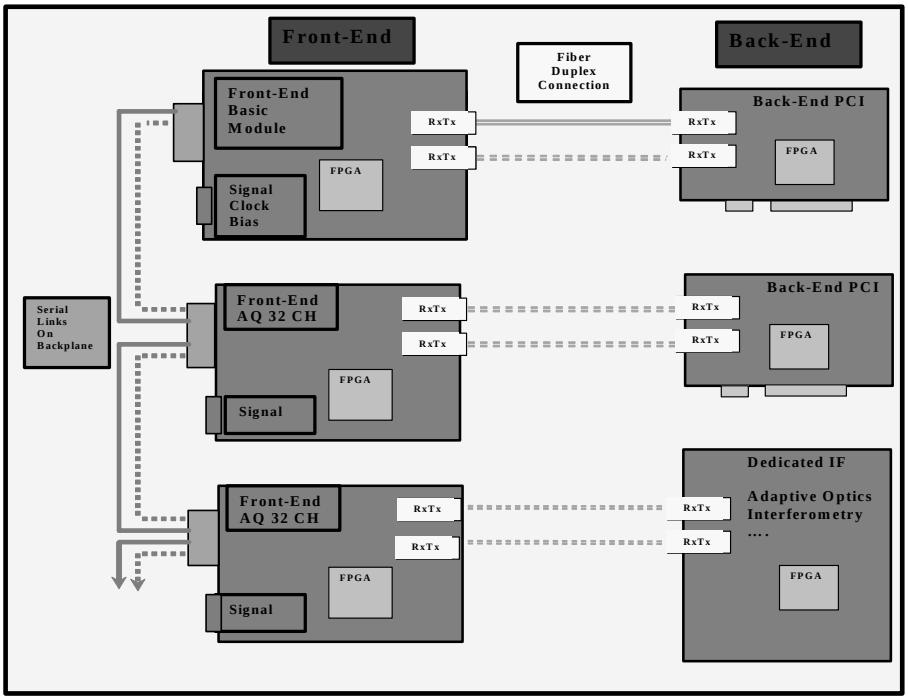

Figure 7. Multi Channel System for Special Applications

7. CONCLUSIONS

Advanced FPGA technology allows building low power and compact data acquisition systems for a high range of applications like single detector or mosaic detector readout with different detectors from visible to mid IR.