Study on the hardware of the ESO Next Generation Detector Controller (ENGDC)

People involved in the discussion:

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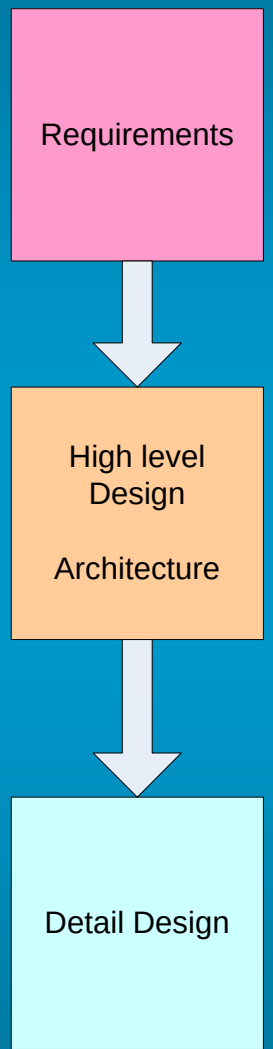
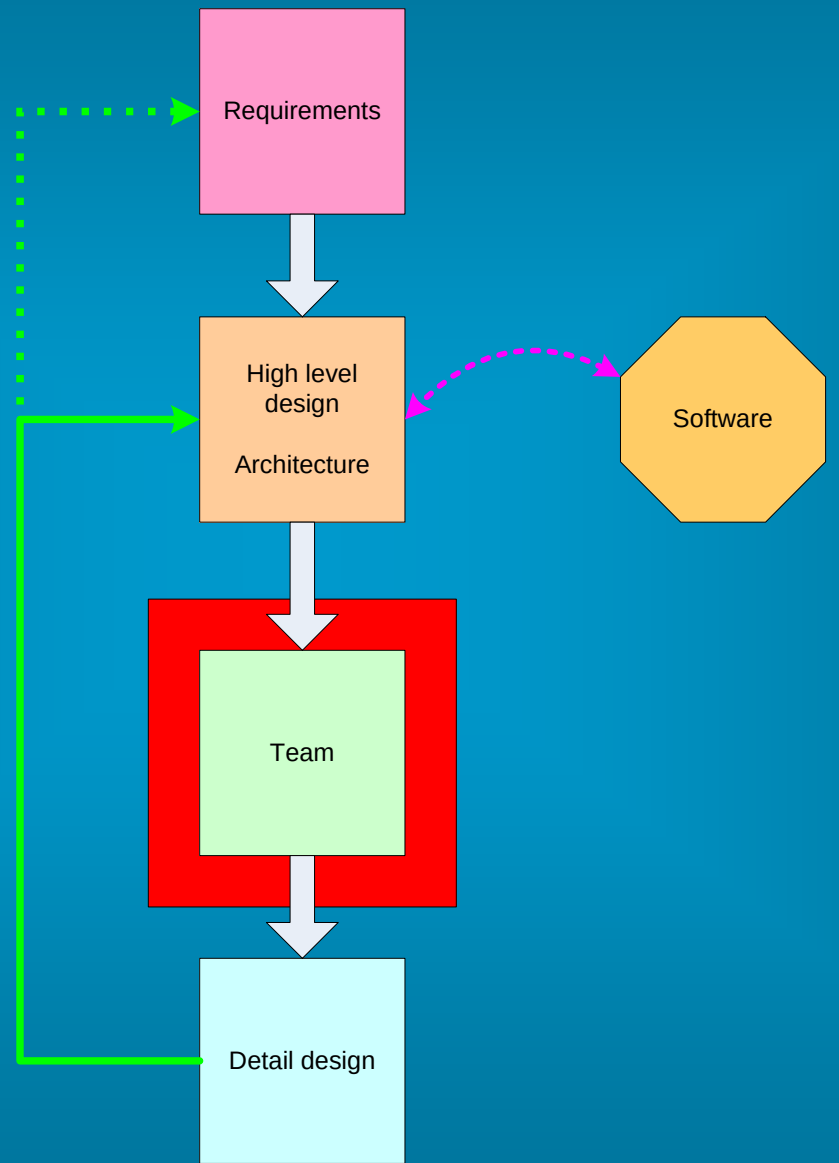
Project electronics design flow



Project electronics design flow (extended)



This presentation is about exploring the possibilities both in architecture and its implementations in order to foster the discussions between the IR and ODT groups to find an optimal implementation.

There are as many questions as answers !!!

Requirements (incomplete and preliminary)

	FIERA	IRACE	Minimum requirements	Goal	Extreme case
Clock voltage range	-14.5V..+14.5V	-10V..+10V			L3CCDs
Number of clock channels per board	14 per board	16 per board (*)	???		
Maximum number of clock boards	4	2			
Clock line maximum current	500mA or higher	30mA	300mA 400mA peak		
Clock voltage accuracy	12-bit	12-bit	12-bit ???		
Clock multilevel support	YES	NO	NO???		YES
Bias voltage range	-15V..+30V	???..???	-15V..+30V		
Number of bias voltages	32 per board	16 per board (*)	???		
Preamp noise	Not measured	???	Limited by forthcoming CCDs???		
Preamp gain adjustable	YES	NO	NO???		
Preamp gain range	1.5 to 3 (adjustable)	3.5 to 8 (Fixed)	???		

(*) IRACE shares clock and bias in one single board. A CLDC board has 16 clock and 16 bias channels.

Requirements (contd.)

	FIERA	IRACE	Minimum requirements	Goal	Extreme case
Video sampling frequency (2)	**2MS/s (limited by the ADC)**	**2MS/s (limited by the ADC)**	**5MS/s???**		
Number of video channels	**4 per board**	**16 per board**	**???**		
Video chain noise (referred to the preamp input)	**Not available**	**???**	**???**		
Embedded video processing	**YES**	**NO**	**YES???**		**HAWAII-2RG ???**
Seamless running sequencer	**YES**	**YES**	**YES**		
Sequencer granularity	**20ns or 25ns**	**50ns**	**???**		
DMA transfer	**PCI 33MHz/32-bit**	**PCI 33MHz/32-bit**	**PCI 66/64???**		
Non-linearity					
Shutter interface	**YES**	**NO**	**YES**		
Need of cooling	**YES**	**NO**		**NO**	
Size				**6U/3U???**	
Power consumption	**Huge in fully populated systems**				
Weight					

Requirements for future detector and instrument systems

MUSE

- Controller maximum allowable weight: TBD.
- Number of channels per head: 4
- Pixel rate per detector/per controller: 625kpx/s.

Future AO systems

- Number of video channels: 256/512
- Maximum frame rate: 1..3kHz
- Read-out noise requirement:
  - 1 e- at 700 frame/s
  - 3 e- at 1.5 kframe/s
  - Epitaxially grown JFET: <2e- at 500kHz
  - MIT/LL: 3-4 e- at 2MHz.

Requirements for OWL

- Not known yet

X-Shooter

- To be bulletized

CCD detectors

- L3Vision clock voltages up to +40V.
- L3Vision clock shape: sine waveform.
- OTCCD/OTA: digital interface (ASIC would cover it)

HAWK-I

- 4 x HAWAII-2RG
- 4 x 36 video outputs

KMOS-I/KMOS-II

- 4 x HAWAII-2RG
- 4 x 36 video outputs

IR detectors

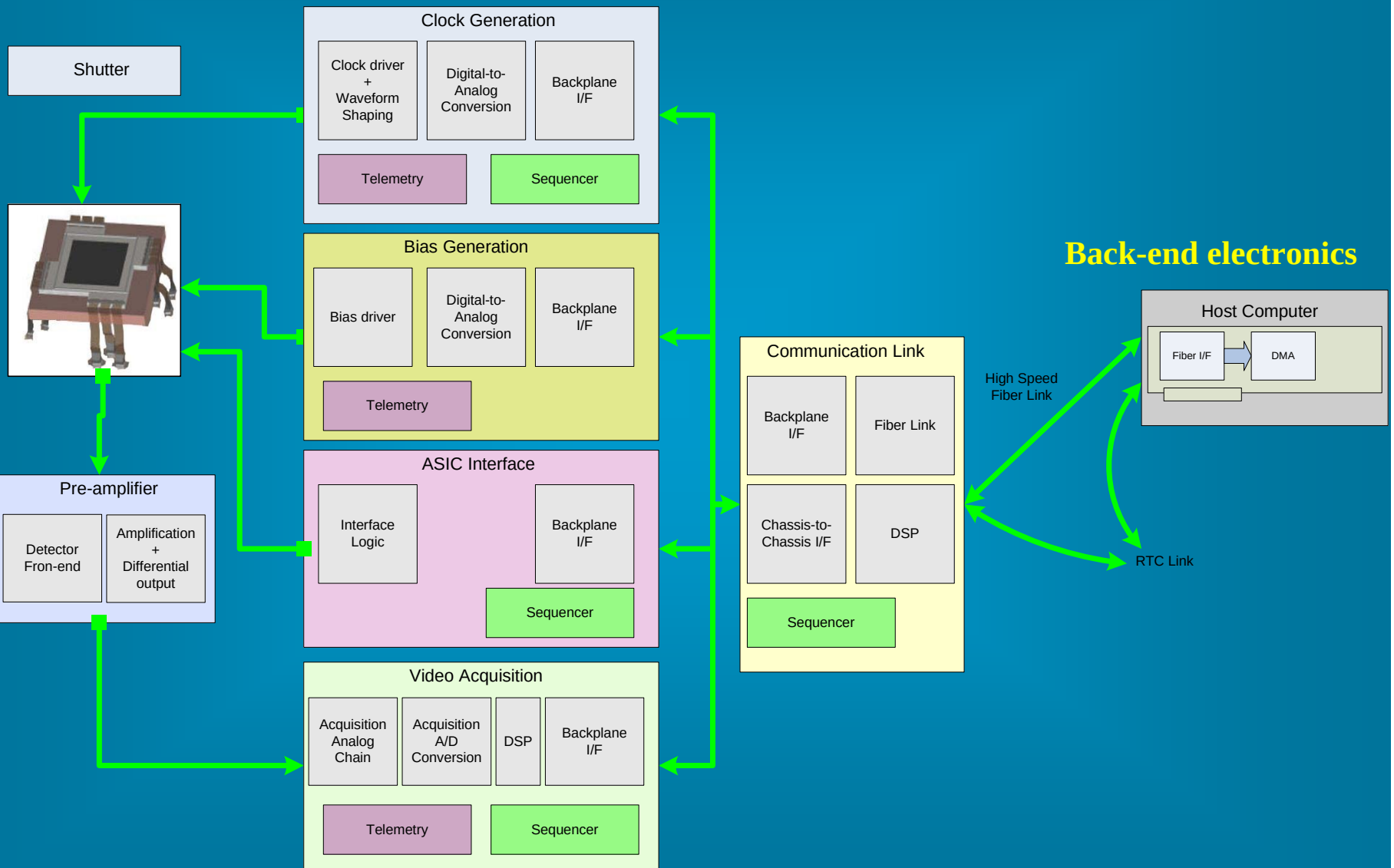
- HAWAII-2RG
  - 2kx2k read every 26ms
  - 2.46Gb/s link
- 5MHz 16-bit ADCs
- (Embedded) real-time processing in high level language (cosmic ray rejection).
- Subpixel sampling by digital filter
- Guiding on science frame

GENERAL

- ASIC support
- Flexible modularity able to be scaled up or shrunk down to our needs
- Multi giga bit optical link
- Fully-fledged embedded video processing
- Conformable form factor, big and with many channels or small with a few channels and lightweight

Architecture
General block diagram

Front-end electronics



Architecture

Breakdown of functionalities. Many partitioning possibilities.

FIERA

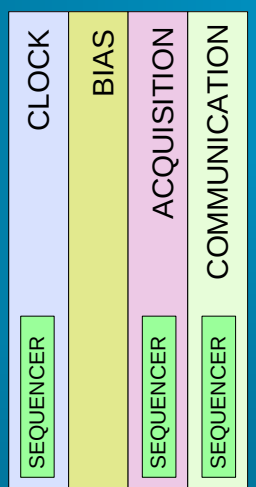
- Clock board with on-board sequencer
- Bias board
- Video board with on-board sequencer
- Communication board with on-board sequencer

IRACE

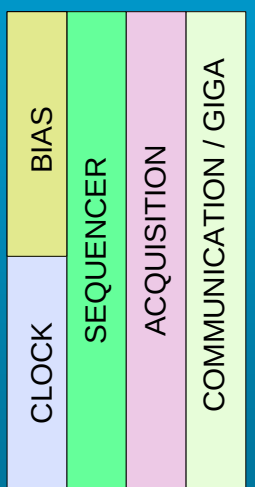
- Clock and bias with no sequencer
- Acquisition board with no sequencer
- Communication board with no sequencer
- A dedicated board for the sequencer

Monsoon

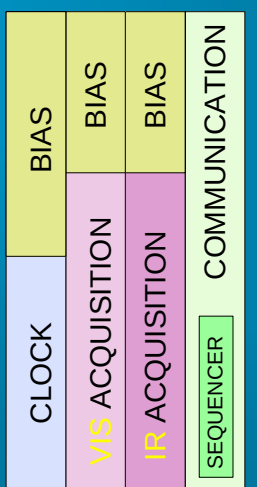
- Clock and bias board with no sequencer
- Bias and acquisition board for IR with no sequencer
- Bias and acquisition board for optical detectors with no sequencer
- Communication and main sequencer



FIERA



IRACE



Monsoon

Architecture

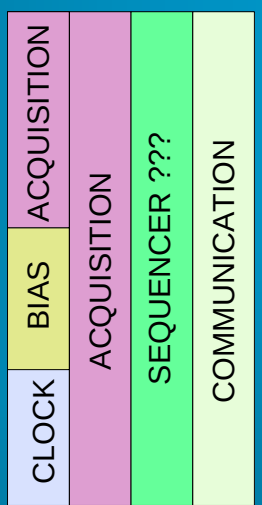
Breakdown of functionalities. Many partitioning possibilities (contd.)

ESODAC

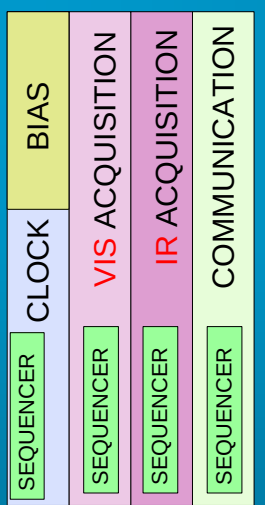
- **Clock, bias and acquisition board**
- **Additional multi-channel acquisition board**
- **Communication and main sequencer board**

ENGDC (a random example of functionality breakdown)

- **Clock and bias with built-in sequencer**
- **Acquisition board for IR with sequencer**
- **Acquisition board for optical detectors with sequencer**
- **Communication board with sequencer**



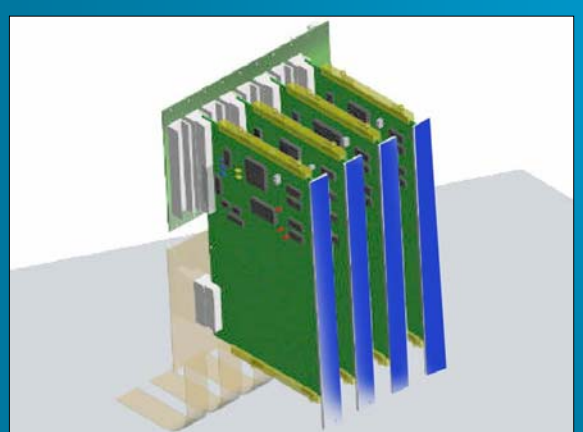
ESODAC

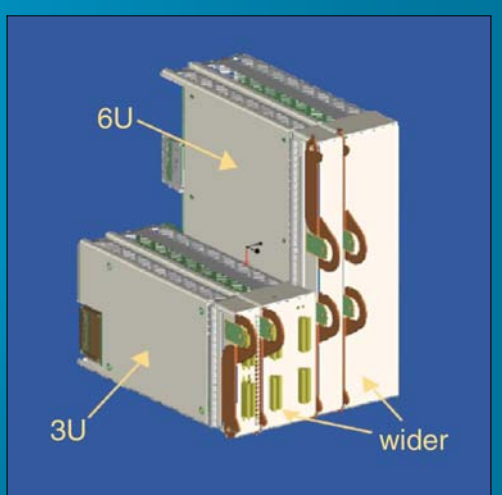


ENGDC (an almost random example)

Architecture
Some ideas to be discussed

- Connection to the detector **through the backplane** or front-panel ?
- Board-to-board connections through **Serial Switched Fabrics** or parallel bus ?
- **Chassis-to-chassis** interconnection through Serial Switched Fabrics ?
- **CompactPCI**, VME or other backplane mechanical standard ?
- Do we want a single board system for simple instruments ?
- Would it be advantageous to have an architecture allowing **6U and 3U front-end form factor** ?

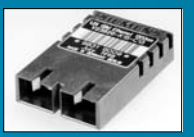




Architecture
Optical Link. PMC/CMC alternative

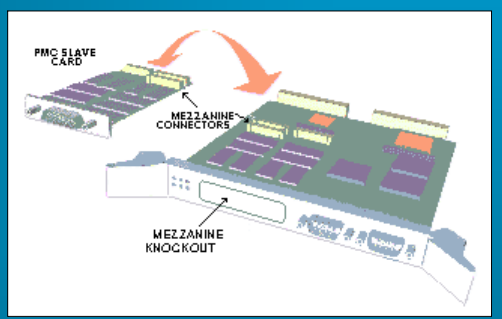
- New generation of IR systems seems to be more bandwidth demanding than their forthcoming optical counterparts
- If no reduction of raw data by pre-processing they require a 2.46Gbps optical link:
  - HAWAII-2RG: 2k x 2k x 16 bits/pixel x 1/26ms
- FIERA and IRACE use a point-to-point fiber link running at 1.25Gbps:

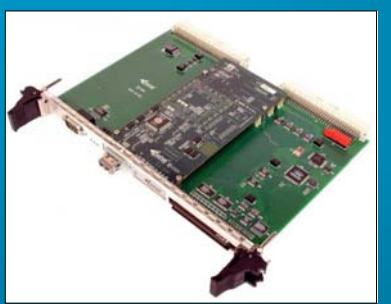

FIERA


IRACE

- 3.125Gbps are possible at > 40km and 10Gbps at > 10km

- COT (Commercial Off The shelf) units are available
- A mature technology is the PMC/CMC standard:



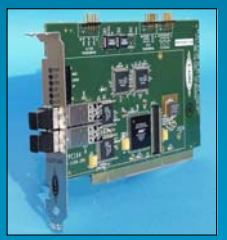


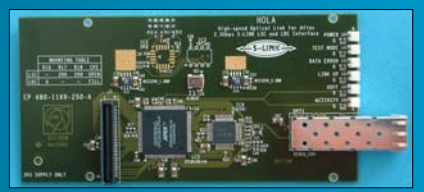
Architecture

Point-to-point optical link. Some COT alternatives

S-LINK HOLA card

- 2.5Gbps
- Open standard by CERN
- Duplex
- 32-bit data width
- Linux, VxWorks.





Multi-point FILAR card

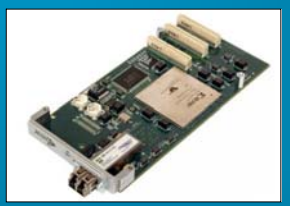
- Four HOLA S-Link card
- 33/66 and 32/64 PCI interface
- CERN open standard
- Able to communicate to HOLA S-Link board
- Linux, VxWorks

FiberXtreme SL240

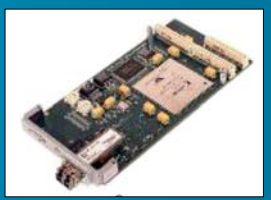
- 2.5Gbps available now
- 10Gbps available in one year
- 64-bit PCI
- Support HPUX, Solaris, Linux, VxWorks and Windows
- PMC and CMC standards

64-bit PCI

CMC



PMC



Architecture

COT point-to-point optical link. Discussion

PROS:

- Fulfill requirements
- No need to in-house development
- Cheaper than in-house design in low quantities (and some in high quantities too)
- Software support. No in-house development
- 10Gbps in one year

CONS:

- Expensive in high volumes
- Only one functionality
- Long-term availability ?

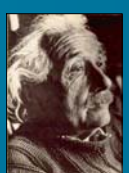
Discussion:

- **COT satisfy the requirements of the ENGDC: 2.5Gbps**
- **CMC/PMC add-in card can be both on front-end and host-computer**
- **CMC/PMC standard does not increase the board width**
- **They support Solaris, Linux, VxWorks, HP-UX, IRIX and Windows**
- **No need to design in house for such a standard functional block**

They want us to save time and money !

Sometimes one pays most for the things one gets for nothing.

Albert Einstein



Architecture
Preamplifier

Requirements for CCD systems:

- AC-coupled
- Outside cryostat ➔ preferably for contamination
- No need to have adjustable gain (FIERA)
- Differential output

Requirements for IR systems:

- DC-coupled
- Inside cryostat
- Differential output

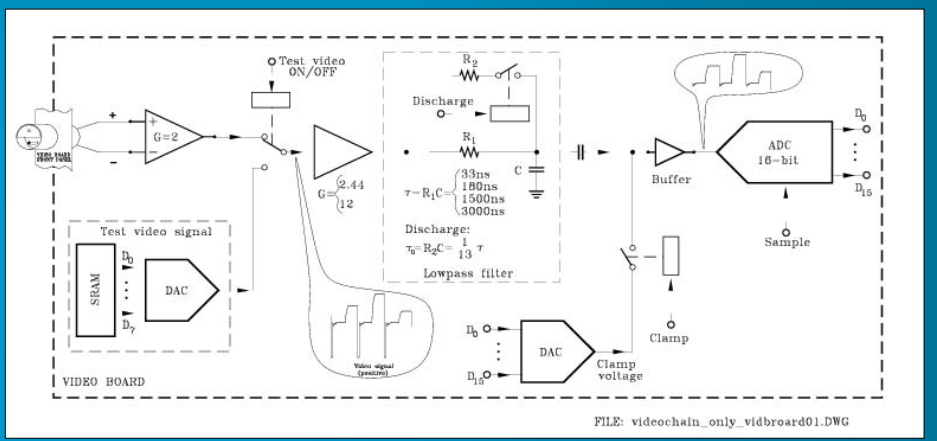
Discussion:

- **Is there enough commonality for single design ?**
- **Should the architecture permit the connection without preamp ?** 

Architecture
Acquisition module

FIERA video chain:

- **Three stages needed before the analog to digital conversion**
  - **Differential to single-ended**
  - **Adjustable gain**
  - **Adjustable low pass filter**
  - **Analog clamp-and-sample**

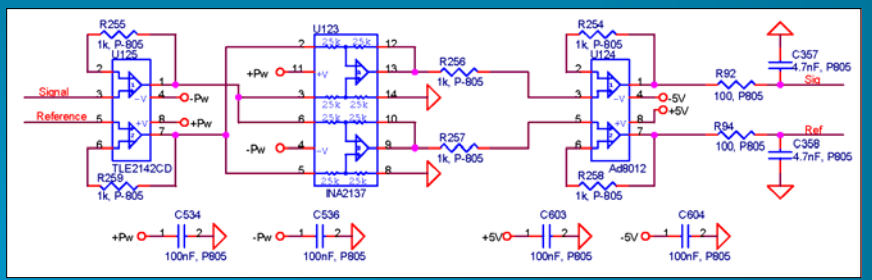


Estimated maximum number of channels: 8

Architecture
Acquisition module (contd.)

IRACE video chain:

- **Only one stage before analog to digital conversion:**
  - **Differential to single-ended**
    - ***Mostly Fixed gain ?***
    - ***Fixed low pass filter***
    - ***No clamp and sample***



Estimated maximum number of channels: ~ 32 ???

Discussion:

- **Is there enough commonality for single design ?**
- **Study required to determine development direction. Questions:**
  - **analog clamp-and-sample**
  - **dual slope integrator**
  - **digital CDS**
  - **optimum number of channels per board**

Architecture
Clock & Bias generation

Clock

Requirements for CCDs:

- Clock: +/- 14V
- Current for CCD mosaics: 300mA (peak >400mA)

Requirements for IRs:

- Exceeded by the ones for CCDs
- Faster clocks than CCDs ?

Special:

- **AO:** Multilevel support
- **L3Vision:** +40V and sine wave

Discussion:

- **How many clocks per board ?**
- **Channel aggregation for high current requirements ?**

Bias

Requirements for CCDs:

- Bias: -10 to +30V
- Low white noise
- Low 1/f noise
- Temperature stability

Requirements for IRs

- Bias: ???
- Low white noise
- Extremely low 1/f noise
- Very high temperature stability

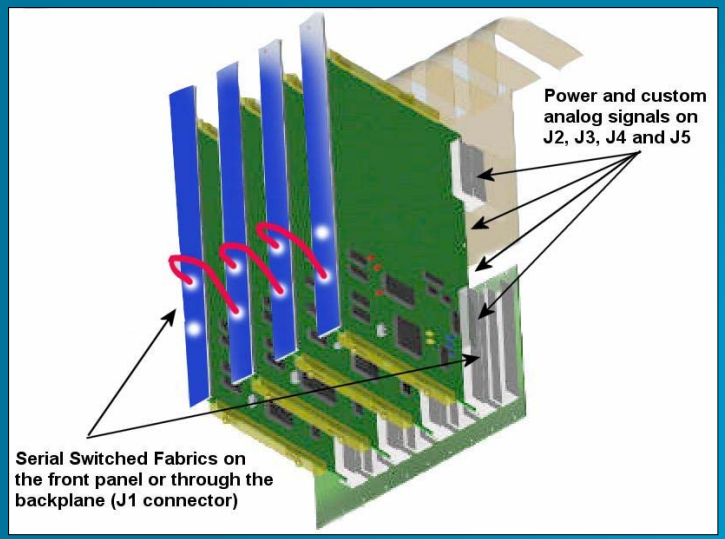
Special:

- **AO HLL CCDs:** -150V

Discussion:

- **How many bias channel per board ?**
- **High voltage as an add-in small module**

Architecture
Backplane & Bus



About CompactPCI mechanical backplane:

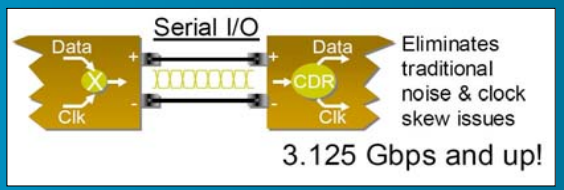
- Much higher pin count than VME: 550 pins against 192
- Connector surround by outside ground blades
- High-quality 2mm pin socket connector that meets industrial requirements
- Success stories about Serial Switched Fabrics on CPCI backplane

About VME:

- VME has evolved over time to support up to 64 bits bus size and is undoubtedly a solid technology… but it has become dated

About Serial Switched Fabrics:

- Xilinx Virtex-II Pro family is an excellent option



Proposal:

- Serial Switched Fabrics for point-to-point, board-to-board communication:
  - It would also allow chassis-to-chassis interconnection to scale up the detector electronics
- Serial links on J1 backplane connector or front-panel (less attractive)
- Power, analog and custom signals on J2
- Additional analog and custom signals on J3, J4 and J5 connectors: 440pins

Discussion:

- Can the architecture be designed in such a way that it allows two type of chassis: 6U and 3U ?
- 6U and 3U chassis: Would it be advantageous for very distributed scientific systems (MUSE) or sensing applications ?

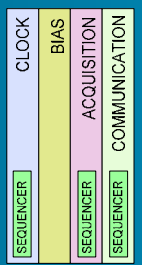
Architecture

Sequencer & Telemetry

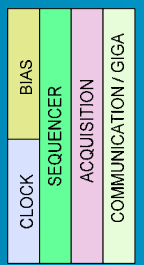
- **Similar requirements for IR and Optical**
- **Sequencer is a mature block and there is no need to be redesigned**
- **Easy to find commonality by using Virtex-II Pro FPGAs and VHDL**

Discussion:

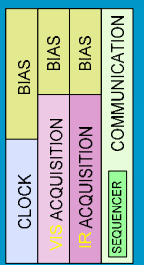
- **Where is the sequencer located ?**
- **Common hardware → Common software ?: Common user interface to program clock timing ?**



FIERA



IRACE



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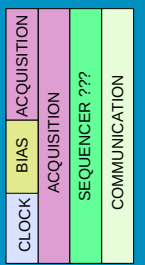
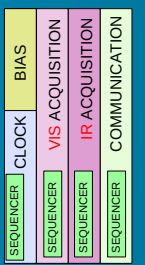


ESODAC



ENGDC
(random example)

Telemetry

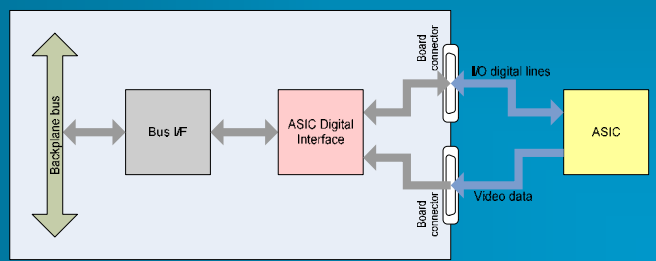
Discussion:

- **Standard to ease the handling of telemetry by the software**

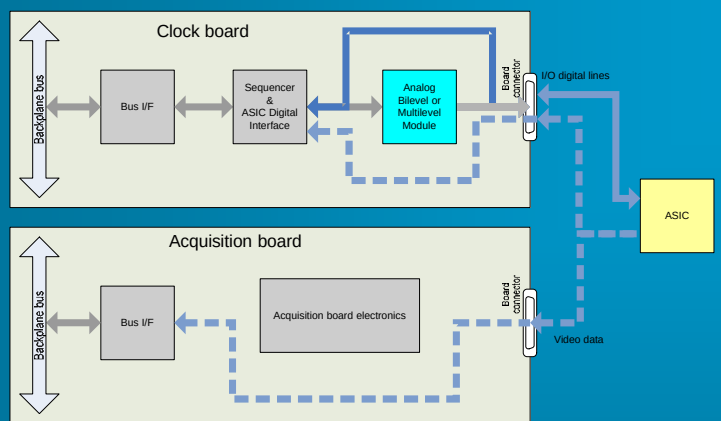
Architecture
ASIC support

• Easy stuff. The question here is whether to make the interface through a separate and dedicated board or through a modular and bidirectional clock board.

• Interface via a dedicated board:



• Interface via the standard clock board or clock board and acquisition board:



Discussion:

- Two architectural options to support ASIC: dedicated board or standard board?
- If standard boards are to be used, two more architectural approaches:
  - Bidirectional clock generation board
  - Bidirectional clock generation board in conjunction with the acquisition board
- ASIC interface still uncertain and many varieties are foreseeable so we are probably better off with a customized board

Architecture (some topologies explored in appendix)

Embedded real-time image processing

Requirements for IR detectors

- Embedded real time image processing in high level language (cosmic ray rejection)
- Subpixel sampling by digital filter
- Guiding on science frame
- Fowler sampling
- Up the ramp
- Intelligent resetting of pixels
- On a Hawaii-2RG, 2kx2k and 26ms frame period ➔ 2.46 Gbps in real-time ???
  - Almost 40% of PCI 64/66 peak bandwidth just to put the image in host-computer memory!!!

Requirements for Optical detectors

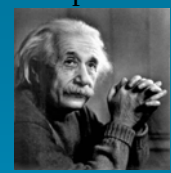
- Digital clamp-and-sample
- Centroiding for AO

Question to answer: Where should real-time processing be done? In controller or back-end ?

Shutter Interface

Just digital outputs for shutter control ???

Everything should be made as simple as possible, but not simpler.
Albert Einstein

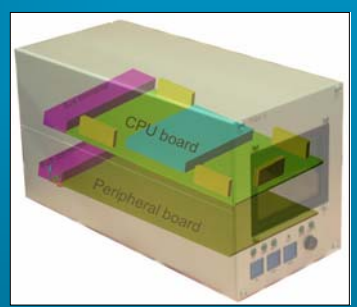


The facts:

- We have to deal with 11 types of shutters
- Out of these 11 types, 7 shutters are completely different
- Shutters are non-standard subsystem, and unfortunately it will always be so
- Shutter are mechanical parts and actual exposure times have to be measured
- Shutter fails and the error has to be reported to invalidate the exposure
- Unfortunately, to interface to a shutter one needs far more than toggling a digital line

Partial conclusion:

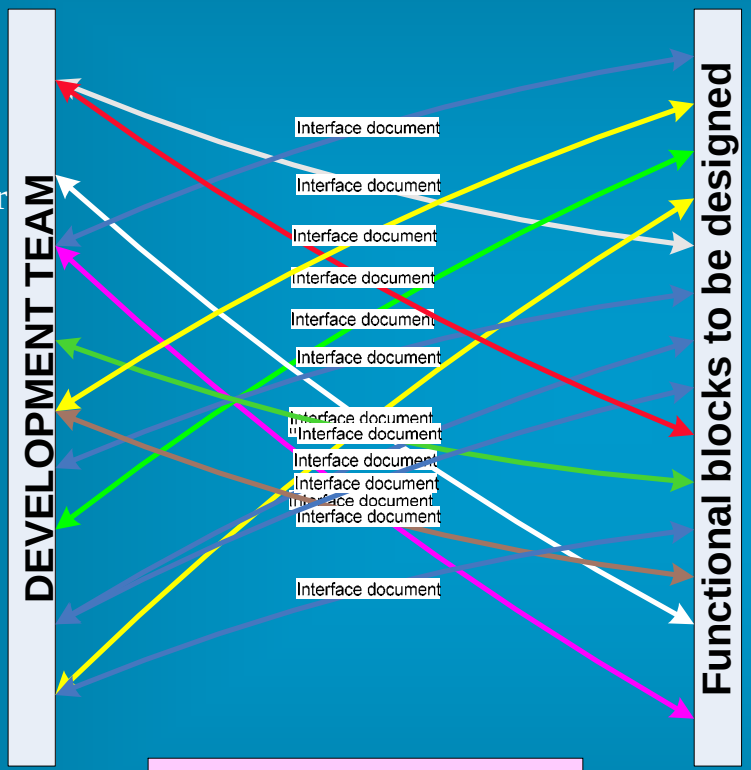
- PULPO-II well serves the purposes of shutter driver and control
- ENGDC only needs to provide a shutter interface



PULPO-II

Development Process

- Reinhold Dorn
- Mark Downing
- Siegfried Eschbaumer
- Christoph Geimer
- Olaf Iwert
- Leander Mehrgan
- Manfred Meyer
- Roland Reiss
- Javier Reyes
- Jesper Thillerup



Common EDA tools

Use the same set of core components

The functional blocks

- **Clock generation**
- **Bias generation**
  - Normal voltage generation
  - High voltage generation
- **Digital interface to the backplane**
- **IR acquisition board**
  - Analog amplification
  - Analog to digital conversion
  - On-board real-time processing
- **Optical acquisition board**
  - Analog amplification
  - Signal filtering
  - Clamp-and-sample circuitry
  - Analog to digital conversion
  - On-board real-time processing
- **Communication board**
  - High-speed optical link
  - On-board digital processing
- **PCI board**
  - High-speed optical link
  - PCI bridge
  - Real-time computer interface
  - On-board real-time processing
  - Shutter interface???
- **Backplane**
- **Backplane interface to the detector**
- **Housing**
- **Cooling**
- **Power supply**

Hardware debugging tools

- **Backplane “snooper”**
- **Fake CCD**
- **Pixel generator**
- **USB/Firewire boards ???**
- **Break-up electronics**
- **Self test ?**
- .
- .
- .

Summary

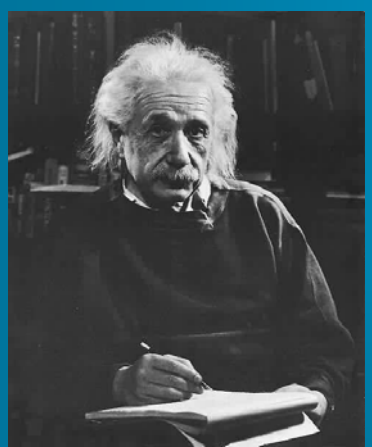
- More work on requirements before start designing
- Detector connected through the backplane or front-panel ?
- COT optical link or in-house design ?
- Serial Switched Fabrics or parallel bus for board-to-board and chassis-to-chassis interconnection ?
- Embedded real time processing: Where ?
- Embedded real-time processing: How ? DSPs or FPGAs.
- CompactPCI, VME or other backplane mechanical standard
- Do we want a single board or multi-board system for simple instruments ?
- Would it be advantageous to have an architecture allowing 6U or 3U form-factor boards ?
- Common or separate preamp design for IR and for optical detectors ?
- Common or separate acquisition board for IR and for optical detectors ?
- ASIC support not to be worried about for the moment. Dedicated board can be a good option
- Shutter is not part of the ENGDC. Only shutter interface required
- Distributed design, development and test among the people: Interface documents

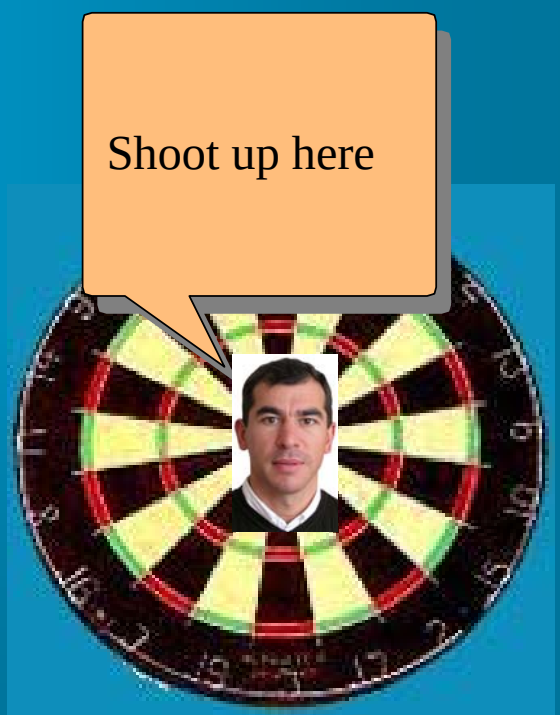
Some other conclusions:

- There are many questions to be discussed and answered
  - More to discuss starting from the requirements and going through the architecture rather than finding the “killer” electronics component
- ESO has many talented and capable people. Focusing these resources on a common controller will deliver a high quality controller in an affordable time

The important thing is not to stop questioning

Albert Einstein





Architecture (appendix)

Embedded real-time image processing. The possible topologies

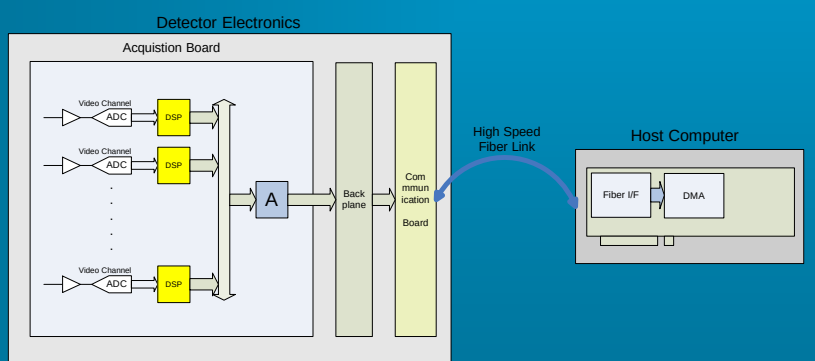
Five topologies/locations:

- On-board and per channel real-time processing
- On-board and per group of channels real-time processing
- On communication board. Data processing previous to downlink to host computer
- Real-time processing located on host computer right after fiber downlink
- Real-time processing always done by a Real Time Computer (RTC)

Two options possible:

- Real-time processing done by FPGAs
- Real-time processing done by DSPs

Option #1: On-board and per channel real-time processing. Idea stimulated by hardwired, small footprint DSPs by Quicklogic.



PROS:

- **Enormous processing power**

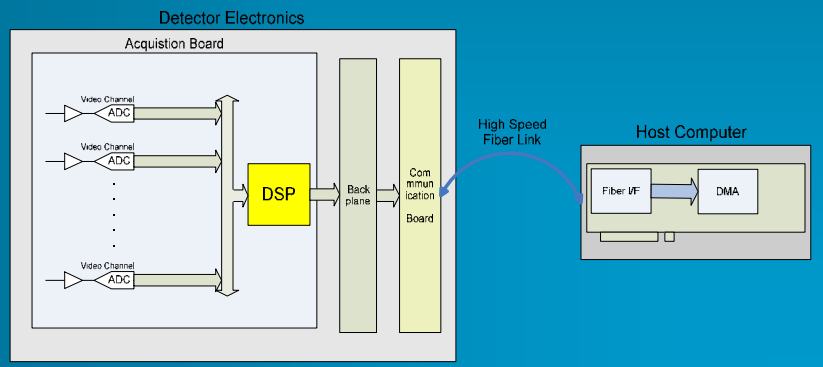
CONS

- **Too much real estate**
- **Most probably an overkill**
- **Power consumption**

Architecture (appendix)

Embedded real-time image processing. The possible topologies

Option #2: On-board and per group of channels real-time processing.



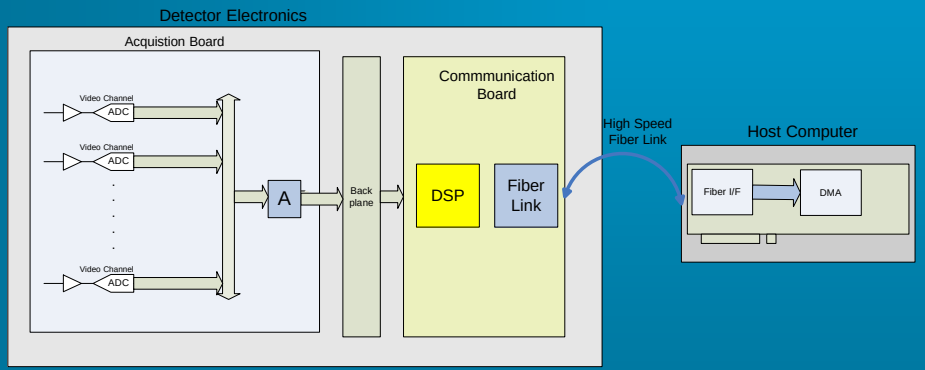
PROS:

- **Reasonable processing capacity**
- **Reasonable real-estate occupation**

CONS

- **Taking real-state where it is more needed ??**

Option #3: On front-end and on giga board. Processing previous to downlink to host computer



PROS:

- **Downlink requirement relaxed**
- **No real-estate required on the acquisition board**

CONS

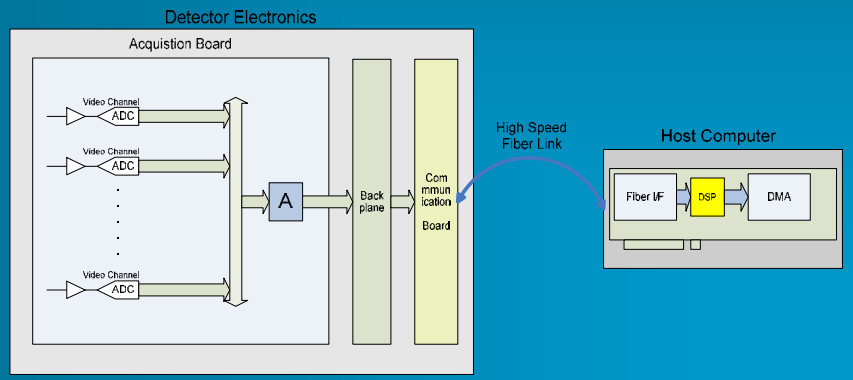
- **Processing required:**

  Number_of_channels x Number_of_Boards

Architecture (appendix)

Embedded real-time image processing. The possible topologies

Option #4: Real-time processing located on host computer right after fiber downlink



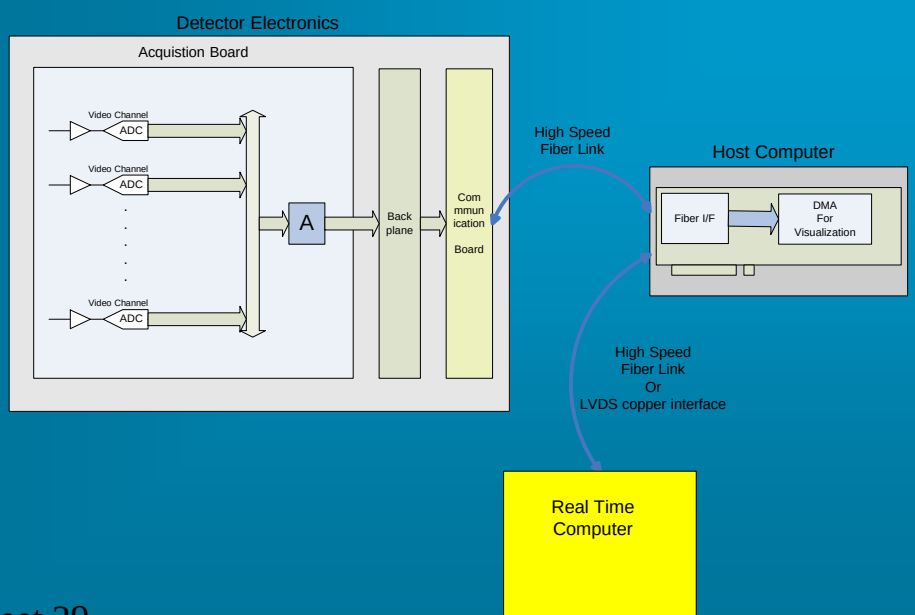
PROS:

- **No real-estate required on front-end**

CONS

- **Processing required:**
  Number_of_channels x Number_of_Boards
- **Downlink requirement not relaxed**

Option #5: No real-time computer as part of the ENGDC. Real-time processing, when needed, handle to an external RTC.



PROS:

- **No real-estate required on front-end**
- **ESO proven solution**

CONS

- **Additional computer**

Architecture (appendix)

Embedded real-time image processing. Two options: FPGAs or DSPs

FPGAs:

PROS

- **FPGAs on-board with DSP capabilities**
- **Less real estate needed than DSPs**
- **Powerful FPGAs with DSP capabilities will be anyway on-board**

CONS

- **Less powerful and less flexible than DSP**
- **Programming tools far more primitive than DSPs ➔ Hardware engineer required in the optimization loop?**
- **Hardcoded algorithm**
- **No floating point (weighted digital clamp-an-sample might require)** ***(might be irrelevant for a decision)***

DSPs:

PROS

- **Flexibility**
- **High-level programming tools for algorithm**
- **Processing power unbeatable**
- **Many off-the-shelf add-in cards for processing purposes**

CONS

- **Higher real estate requirement**
- **They could be an overkill**

Architecture (appendix)

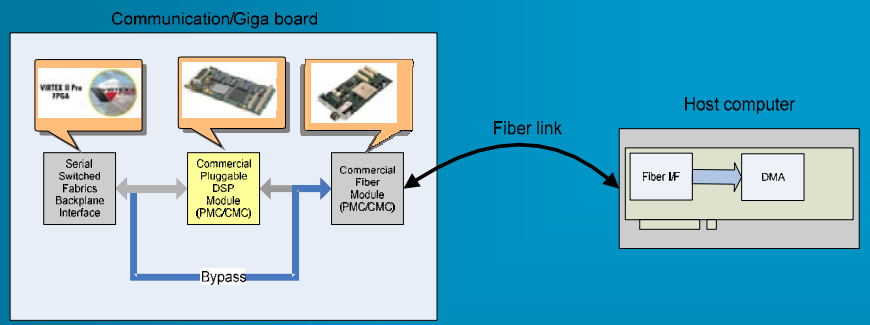
Embedded real-time image processing. A proposal to be discussed.

- DSP based
- Commercial CMC/PMC add-in card on the communication/giga board:

Example:

- Module from Mango with 4 fixed-point DSPs and 5760MIPS each

Communication/Giga board with pluggable DSP module:



The users:

- Gert Finger
- Olaf Iwert
- Mark Downing
- Roland Reiss
- Reinhold Dorn
- Javier Reyes
- Claudio Cumani ???

The "sufferers":

- Andrea Balestra
- Peter Biereichel
- Claudio Cumani
- Joerg Stegmeier

The "doers":

- Christoph Geimer
- Leander Mehrgan
- Manfred Meyer
- Javier Reyes

Discussion on the real-time processing:

- Two possible implementations: FPGAs vs. DSPs
- Need to work on the requirements
- Shouldn't we let the "sufferers" decide, not the designers, what they want to have ?
- Shouldn't we let the users decide, not the designers, what they want to use ?