



PCI interface and backplane of NGC

NGC Backplane

- General purpose
- Board features
- CompactPCI connector
- Ground and Power planes
- Bending of the backplane
- Different backplane size

Backplane

➤ **General purpose**

Designed to achieve requirements and specifications for:

Excellent power distribution

High speed differential pairs

Mechanical specification

➤ Board features

➤ CompactPCI connector

➤ Ground and Power planes

➤ Bending of the backplane

➤ Different backplane size

Backplane

➤ General purpose

➤ **Board features**

Totally 10 layers, 6 ground and power planes and 4 signal layers

Point to point connection of the differential high speed link

Provides system clock of 100 MHz, which is distributed to all slots by using separate buffer

Power up reset component used for global reset for all slots

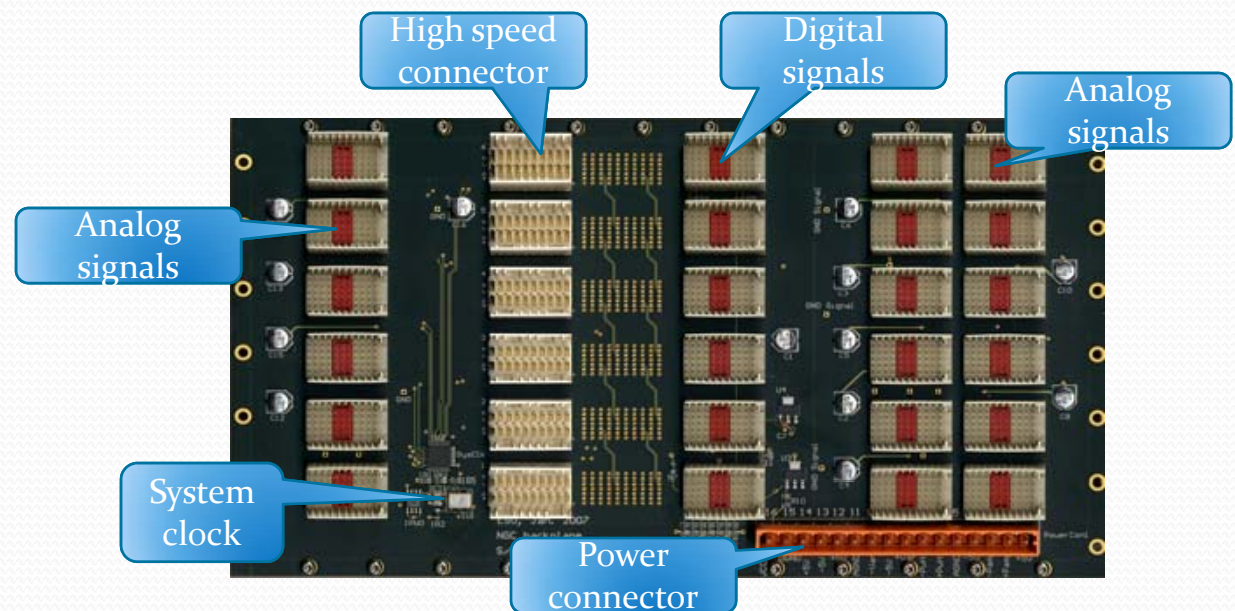
Bypass capacitors for supply voltages

➤ CompactPCI connector

➤ Ground and Power planes

➤ Bending of the backplane

➤ Different backplane size



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Backplane

- General purpose

- Board features

- **CompactPCI connector**

Industrial standard connector, which will on long term displace the VME connectors.

More flexibility due higher number of pins

Boards can be plug on both sides of the backplane

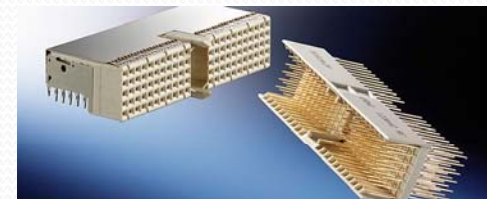
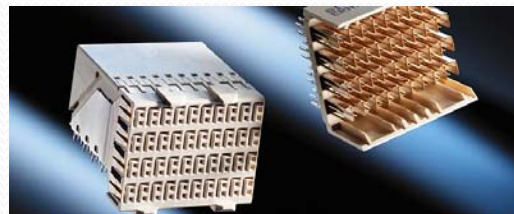
Special connectors (from ERNI) for the high speed differential link

Shielded 2mm pitch, EMI/RFI protection.

- Ground and Power planes

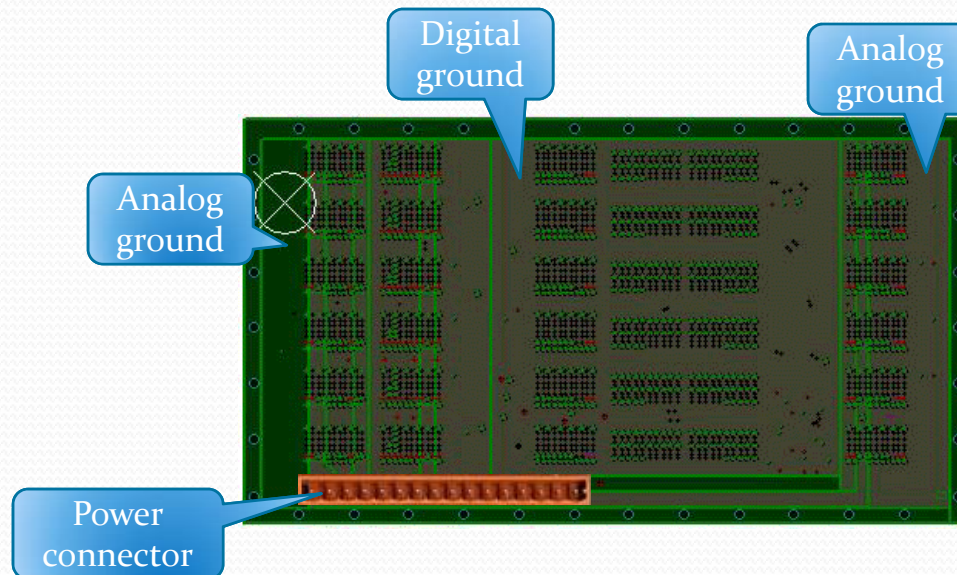
- Bending of the backplane

- Different backplane size



Backplane

- General purpose
- Board features
- CompactPCI connector
- **Ground and Power planes**
 - Divided in digital ground, analog ground and, high speed link area
 - One power entry connector for easy exchange of the backplane board
- Bending of the backplane
- Different backplane size



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Backplane

- General purpose
- Board features
- CompactPCI connector
- Ground and Power planes
- **Bending of the backplane**

To avoid bending the NGC backplanes are equipped with stiffeners, which reduce bending of the backplane while inserting and extracting of the boards cards to a minimum.

- Different backplane size



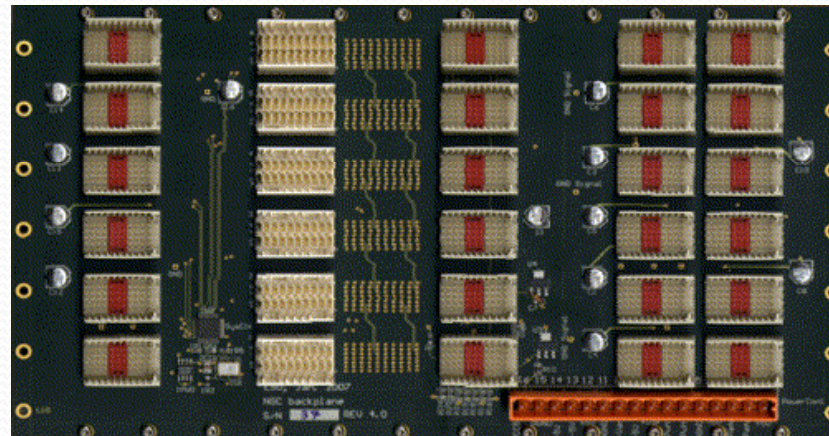
Backplane

- General purpose
- Board features
- CompactPCI connector
- Ground and Power planes
- Bending of the backplane
- **Different backplane size**

For more flexibility two different backplane size created

- Two slot version**
- Six slot version**

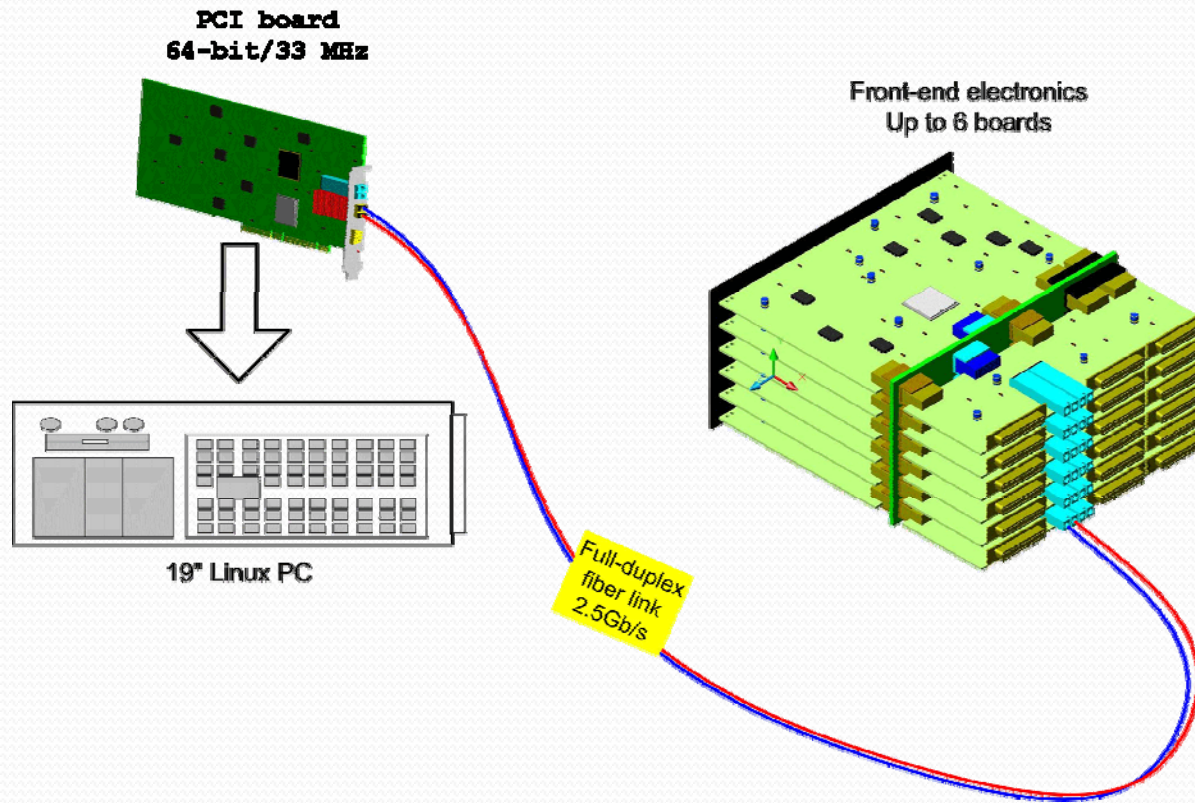
They differ only in the number of slots



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PCI interface

PCI module is the interface between the front-end electronics and the number cruncher (Linux-PC).

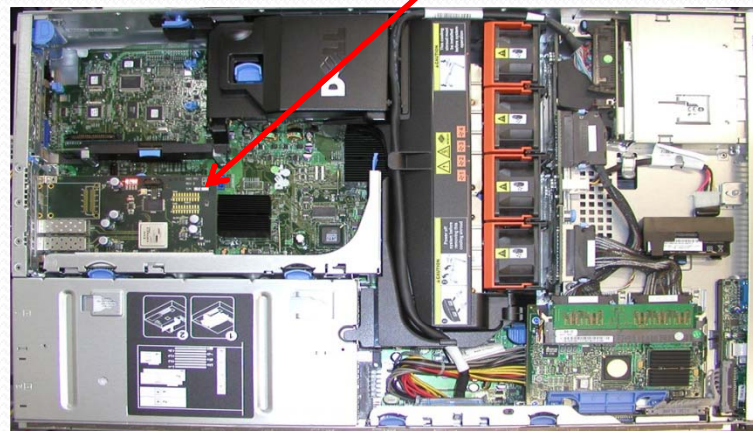
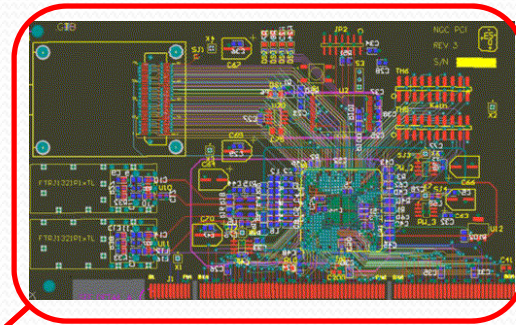


PCI interface

PCI module is the interface between the front-end electronics and the number cruncher (Linux-PC).

With the following features:

- 64 bit data bus with 33 MHz clock
- PCI controller done by the XILINX FPGA (IP core).
- Full/duplex fiber link (2.5 Gb/s)
- USB interface



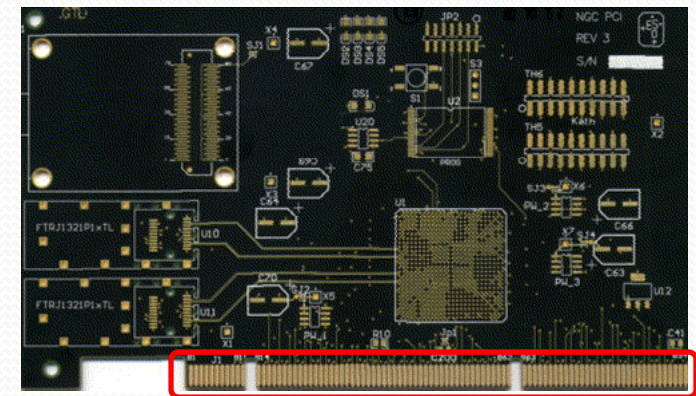
LLCU

PCI interface

PCI module is the interface between the front-end electronics and the number cruncher (Linux-PC).

With the following features:

- **64 bit data bus with 33 MHz clock**
 - Results a bandwidth of 256 MB/s.
 - It matches to the data rate of fiber link (2.5 Gb/s).
 - Optional bus clock of 66 MHz (512 MB/s).
- PCI controller done by the XILINX FPGA (IP core).
- Full/duplex fiber link (2.5 Gb/s)
- USB interface

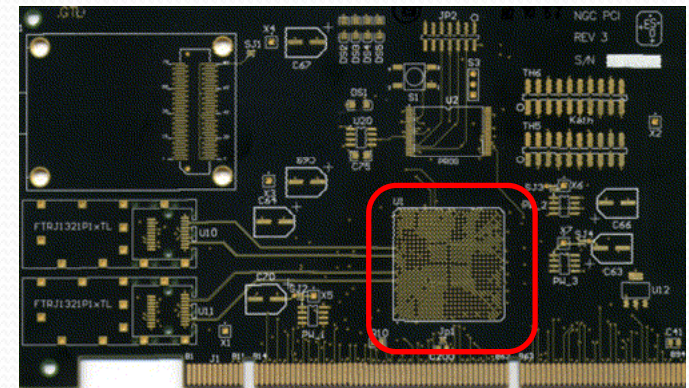


PCI interface

PCI module is the interface between the front-end electronics and the number cruncher (Linux-PC).

With the following features:

- 64 bit data bus with 33 MHz clock
- **PCI controller done by the XILINX FPGA (IP core).**
 - IP core (intellectual property core) is provided by Xilinx doing all the timing needed for the PCI interface.
 - Compliant with PCI v2.3 specification (3.3 V).
 - Local bus interface for user application
 - PCI master/slave interface
- Full/duplex fiber link (2.5 Gb/s)
- USB interface

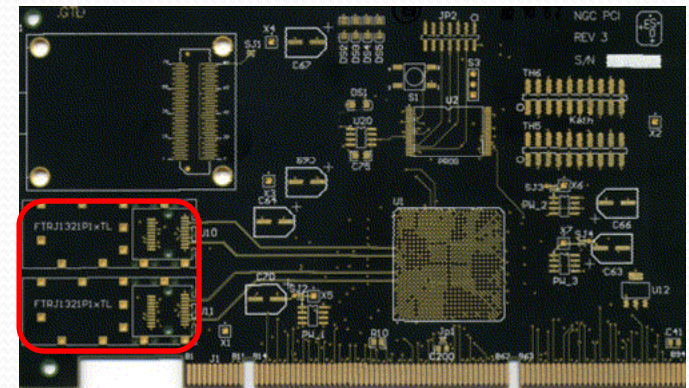


PCI interface

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With the following features:

- 64 bit data bus with 33 MHz clock
- PCI controller done by the XILINX FPGA (IP core).
- **Full/duplex fiber link (2.5 Gb/s)**
 - fiber optic transceiver for RocketIO of the XILINX
 - data and commands time multiplexed transferring
- USB interface



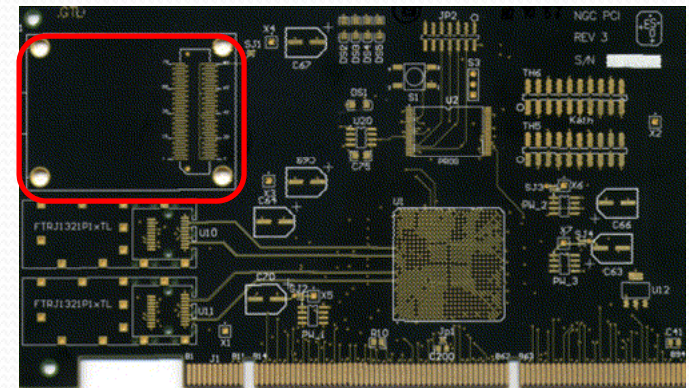
PCI interface

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- 64 bit data bus with 33 MHz clock
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- Full/duplex fiber link (2.5 Gb/s)
- **USB interface**

Provides possibility to operate the controller from a portable PC
For diagnostic and maintenance purpose





Thank you

Leander Mehrgan