# *Report on NGTCCD Integration and Test mission*

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## 1 – Purpose of the mission

The mission was aimed to integrate and test the ARC Controllers together with the TCCD Heads hosting the E2V devices CCD57-10 and CCD47-20 for the future replacement of the actual systems on the telescopes for guiding, image analysis and field viewing.

## 2 – System description

### 2.1 - Hardware

The NGTCCD systems comprise 3 main parts:

- PMC board ARC-65 installed on the PMC Slot of the MVME2604 or MVME2700 CPU board.
- ARC Controller with water cooler
- CCD head

In addition a power supply 24V 3A is required for the controller and a FO pair connects the PMC to the controller.

### 2.2 - Software

The CCD control software has been extended with 2 new modules: the hardware dependent layer 'ccdrdb' providing a hardware independent interface and the VxWorks device driver 'arcdrv'.
The latter module hosts also the PMC and Controller embedded DSP code.
The software interface has not been modified both for command and database.
The MVME167 (68k) version does not include these 2 modules since the system can not be interfaced to this type of CPU.
The latest version can be built using the module 'ccdint' version 7.9.

## 3 – Integration and tests

The two CCD types E2V CCD57-10 (512×512 pixels; size13μm) and CCD47-20 (1024×1024 pixels; size13μm) have been integrated and tested. In particular the clock patterns timings have been measured and the bias voltages tuned. The results are presented in the table below:

## 1 - Configuration

| | CCD47-20 | CCD57-10 | Unit | Signification |
|---|---|---|---|---|
| ISC_DELAY | $1C0000 | $0C0000 | 40ns | IS Parallel clock delay for Wipe |
| IS_DELAY | $1E0000 | $0E0000 | 40ns | IS Parallel clock delay |
| S_DELAY | $7F0000 | $0E0000 | 40ns | S Parallel clock delay |
| R_DELAY | $000000 | $000000 | 40ns | Serial register transfer delay |
| BIAS_OFFSET_L | 2101 | 2197 | | Bias Offset Left |
| BIAS_OFFSET_R | 2019 | 2143 | | Bias Offset Right |
| H_WIPE | 1080 | 566 | | # Serial clocks to clear |
| V_WIPE | 1034 | 528 | | # Parallel clocks to clear |
| H_SIZE | 1072 | 560 | | Horizontal/Serial Chip Physical Size |
| V_SIZE | 1033 | 528 | | Vertical/Parallel Chip Physical Size |
| RG_HI | +6.0 | +6.0 | V | Reset Gate |
| RG_LO | -0.7 | -0.7 | V | |
| R_HI | +2.0 | +2.0 | V | Serial Clocks |
| R_LO | -8.0 | -8.0 | V | |
| SI_HI | +5.0 | +5.0 | V | Parallel Clocks |
| SI_LO | -10.0 | -9.0 | V | |
| DG_HI | +5.0 | +5.0 | V | Dump Gate |
| DG_LO | -8.0 | -8.0 | V | |
| Vmax | 12.4 | 12.4 | V | Maximum clock driver voltage |
| VODL | +26.0 | +26.0 | V | Output Drain Left |
| VODR | +26.0 | +26.0 | V | Output Drain Right |
| VRDL | +11.0 | +13.0 | V | Reset Drain Left |
| VRDR | +11.0 | +13.0 | V | Reset Drain Right |
| VOG | -4.0 | -4.0 | V | Output Gate |
| VABG | -5.0 | -5.0 | V | Anti-blooming gate |

## 2- Noise and Sensitivity

| Performances | CCD47-20 | CCD57-10 | Unit | |
|---|---|---|---|---|
| Gain 4 (i.e. 4.75 fast) at 1MPix/s | | | | |
| ADC | 1.6 | 1.2 | e⁻/ADU | |
| Readout Noise | 12.0 | 11.0 | e⁻ RMS | |
| Full well at | 80.0 | 120.0 | ke⁻/pix | Spec is 100 ke⁻/pix |
| Dark Current | | ≈ 45.0 | e⁻/pix/s | Measured at -20°C |
| | | 9 to 13.0 | e⁻/pix/s | Measured at -30°C |

The following performances could be achieved:

| Full Frame | CCD47-20 | CCD57-10 | Unit | 100 Frames |
|---|---|---|---|---|
| WIPE CHIP | 9.70 | 4.10 | ms | No Wipe between exposures |
| FRAME TRANSFER | | 2.75 | ms | ExpTime=0ms |
| WIPE LINE | 10.00 | 4.20 | μs | Transfer 1 image / 2s asynch |
| WIPE PIXEL | 0.32 | 0.32 | μs | No image processing |
| SKIP LINE | 41.00 | 4.85 | μs | No binning |
| SKIP PIXEL | 0.25 | 0.25 | μs | |
| READ LINE | | 570.00 | μs | |
| READ PIXEL | 1.00 | 1.00 | μs | |
| READOUT FULL FRAME | | 9.00 | ms | |
| TIME to NEXT | 25.00 | 24.00 | ms | Constant? TBV |
| READOUT Left | 1.20 | 0.33 | s | |
| READOUT Right | 1.20 | 0.33 | s | |
| READOUT L+R | 0.64 | 0.18 | s | |
| READOUT L+R Bin 2×2 | | 0.15 | s | |
| Max Frequency | 1.56 | 5.56 | Hz | |

| Window [40x40] | CCD47-20 | CCD57-10 | Unit | 1000 Frames |
|---|---|---|---|---|
| Location | [X=1;Y=1] | [X=1;Y=1] | | No Wipe between exposures |
| READOUT | L=41 ; R=41 | L=50 ; R=49 | ms | ExpTime=0ms |
| Max Frequency | 24.39 | **20.41 (*)** | Hz | Transfer 1 image / 2s async |
| Location | [X=800;Y=1] | [X=400;Y=1] | | No image processing |
| READOUT | L=59 ; R=60 | L=41 ; R=41 | ms | No binning |
| Max Frequency | 16.95 | 24.39 | Hz | |
| Location | [X=1;Y=800] | [X=1;Y=400] | | |
| READOUT | L=74 ; R=75 | L=49 ; R=49 | ms | |
| Max Frequency | 13.51 | 20.41 | Hz | |
| Location | [X=800;Y=800] | [X=400;Y=400] | | |
| READOUT | L=92 ; R=90 | L=44 ; R=44 | ms | |
| Max Frequency | 11.11 | 22.73 | Hz | |
| Location | [X=517;Y=496] | [X=261;Y=244] | | Window centered on chip |
| READOUT | L=70 ; R=71 | L= 43; R=43 | ms | |
| Max Frequency | 14.29 | 23.26 | Hz | |

(*) The measure of this frequency shall be repeated as the value seems too low.

## 4 – Functional differences to the DJO systems

### 4.1 – Additional functionalities

- The NGTCCD controller and detectors support 2 readout ports. The chips can be read from either output Left, Right or using both outputs in parallel.
- Binning has been implemented and is available for any output combination for Full Frame, and only for one output when windowed readout selected. Binning factors are 1, 2 or 4. The latter needs some more testing/tuning.
- The exposure time is handled at DSP level and scales from 0 to $2^{24}$-1 ms (4h 40min).

- The exposure sequence performs optionally a single wipe prior to integration.
- The Peltier cooler is controlled by a PID in closed loop. The temperature can be adjusted by potentiometer.
- The embedded software (PMC and Controller DSP code) is open source and runs on the same DSP Family architecture Motorola DSP 563xx. All necessary compiler and linker tools are available on Windows and Solaris.

## 4.2 – Restrictions and limitations

- Only one window can be readout from one output only.
- Telemetry values (bias and clock voltages) can not be modified by software as they are hard-coded in the clock pattern file.
- Telemetry values can not be monitored as the electronics does not include the necessary ADC circuitry.
- The chip temperature can not be readout as the electronics does not include the necessary circuitry; 2 bits indicate the status of the comparators.

## 5 – Conclusions & Future activities

The 2 chips CCD57-10 and CCD47-20 have been successfully integrated – given the limitations listed above – and are ready to undergo long-term reliability and sky tests. The 4 chips that have been tested show excellent cosmetics.
The CCD software is available on both HP and Linux platforms (APR2004 and JAN2006) and PPC CPU running VxWorks 5.4.

The next activities will aim at:
- Improving the PCI interfacing to the CPU: replace the polled PCI handshake by interrupt driven mechanism.
- Improving the data transfer speed and understand / reduce the observed "dead time" of 25ms between exposures.
- Implementing the 2 windows mode readout.
- Implementing the telemetry setting from the CCD software
- Refining the clock patterns and telemetry values for optimal usage of the chip (especially for CCD47-20 which was not delivered by the manufacturer ARC).
- Defining the operational chip temperature for minimizing the dark current
- Improving full well capacity for CCD47-20 (not yet in spec).

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