22-Nov-2006

CCD57-10
Performance evaluation with CPU VSBC6847

1 - CPU Setup

BSP & Bootrom from module **`vltVXWORKS`** version **`3.17.2.2`**
DMA completion interrupt enabled.
PMC in Slot A - IntVec=20 (`0x14`) - IntLine=1 - PCI Device #11 (`0x0B`)
PMC in Slot B - IntVec=21 (`0x15`) - IntLine=1 - PCI Device #12 (`0x0C`)
BAR0 = **`0x80000000`** – Latency **`0xFF`**

2 - CCD Full Frame Setup

UIT = 10ms
Full Frame [512×512]
1 Wipe between exposures
Display 1 image / second asynchronous
No image processing
Sequences of 1000 or 500 images

2a - Output **`_LR`**

Binning		1×1	2×2	4×4
Cycle	[ms]	163	64	36
Frequency	[Hz]	6.1	15.6	27.8

2b - Output **`__L`**

Binning		1×1	2×2	4×4
Cycle	[ms]	298	108	52
Frequency	[Hz]	3.4	9.2	19.2

2c - Output **`__R`**

Binning		1×1	2×2	4×4
Cycle	[ms]	300	108	50
Frequency	[Hz]	3.3	9.2	20.0

3 - CCD Window Frame Setup

3a - Cycle time as a function of the position of the window in the chip

UIT = 10ms
Window [34×34]
Output **__L**
1 Wipe between exposures
Display 1 image / second asynchronous
No image processing
Sequences of 500 images

Cycle [ms]	X=100	200	300	400
Y=100	26	26	28	28
200	28	28	28	28
300	28	28	28	30
400	30	30	28	28

Frequency ranges between 33.3 and 38.5Hz

3b - Typical FS setup with window in center of chip

Setup idem 3a but
Window Start Position (240;240)
No wipe between exposures

Cycle time = 28ms => 35.7Hz

3c - Idem 3b with Image Processing

Centroid: Threshold -3sigma
Background evaluated from image
Extrema calculation
Offsets IPLLX=2, IPLLY=1, IPURX=0, IPURY=1
=> Calculation on sub-image [32×32]

Cycle time = 28ms => 35.7Hz

3d - Idem 3c without Image Transfer (No display)

Cycle time = 28ms => 35.7Hz

3e - Idem 3d from Output **__R**

Cycle time = 28ms => 35.7Hz

3f - Idem 3d with 1 Wipe between exposures

Cycle time = 28ms => 35.7Hz

3g - Idem 3c with UIT=1ms

Cycle time = 18.5ms => 54.0Hz

3h - Measure `Cycle = f(UIT)`

Setup idem **3c**

UIT	[ms]	1	5	10	15	20	25	50	100
Cycle	[ms]	19	23	28	33	38	43	70	118

Cycle = UIT + 18ms

3i - Idem 3c with Output `_LR` and window split

NB: still this mode shall be properly handled so as to merge the 2 windows halves before performing the image processing. Also it sets hard constraints on the window size and position as it shall be located exactly on the middle of the chip (vertical position is free).

UIT=10ms
1 Window `[17×34]` starting at `(239;239)`
Offsets `IPLLX=2`, `IPLLY=1`, `IPURX=0`, `IPURY=1`

Cycle time = 24ms => 41.7Hz

4 - Conclusions

Tests could not be performed w/o DMA completion interrupts.
This only plays a role for large images when the image data reorganization can be performed in parallel with the readout.

Image processing does not impact on cycle time for UIT ≥ 10ms.

Image transfer shall be done asynchronous and at a frequency of max. 1Hz

Window position in chip does not impact significantly on the performances

(approx. ±8%).

Output selection **__L** or **__R** does not impact on the overall performances.
In Full Frame mode w/ or w/o binning, the Outputs **_LR** are the fastest.

Maximum frequency = 54Hz with UIT=1ms (setup **3g**).

The cycle overhead is 18ms for a [34×34] window (setup **3c**).
The minimum exposure time DIT= 1ms when numWipe=1,
The effective exposure time DIT=18ms when numWipe=0.

___oOo___