26-Nov-2006

CCD57-10
Performance evaluation with CPU MVME2700

1 - CPU Setup

BSP & Bootrom from module **vltVXWORKS** version **3.17.2.2**
DMA completion interrupt enabled.
PMC in Slot A only IntVec=25 (0x19) - IntLine=1 - PCI Device #16 (0x10)
BAR0 = **0xFD040000** – Latency **0xFF**

2 - CCD Full Frame Setup

UIT = 10ms
Full Frame [512×512]
1 Wipe between exposures
Display 1 image / second asynchronous
No image processing
Sequences of 1000 or 500 images

2a - Output _LR

Binning		1×1	2×2	4×4
Cycle	[ms]	166	75	34
Frequency	[Hz]	6.0	13.3	29.4

2b - Output __L

Binning		1×1	2×2	4×4
Cycle	[ms]	302	110	50
Frequency	[Hz]	3.3	9.1	20.0

2c - Output __R

Binning		1×1	2×2	4×4
Cycle	[ms]	302	108	50
Frequency	[Hz]	3.3	9.2	20.0

3 - CCD Window Frame Setup

3a - Cycle time as a function of the position of the window in the chip

UIT = 10ms
Window [34×34]
Output __**L**
1 Wipe between exposures
Display 1 image / second asynchronous
No image processing
Sequences of 1000 images

Cycle [ms]	X=100	200	300	400
Y=100	26			27
200		26		
300			27	
400	27			28

Frequency ranges between 35.7 and 38.4Hz

3b - Typical FS setup with window in center of chip

Setup idem 3a but
Window Start Position (240;240)
No wipe between exposures

Cycle time = 25ms   => 40.0Hz

3c - Idem 3b with Image Processing

Centroid: Threshold -3sigma
Background evaluated from image
Extrema calculation
Offsets IPLLX=2, IPLLY=1, IPURX=0, IPURY=1
=> Calculation on sub-image [32×32]

Cycle time = 25ms   => 40.0Hz

3d - Idem 3c without Image Transfer (No display)

Cycle time = 24ms   => 41.6Hz

3e - Idem 3d from Output __R

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Cycle time = 25ms   => 40.0Hz
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3f - Idem 3d with 1 Wipe between exposures

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Cycle time = 30ms   => 33.3Hz
```

3g - Idem 3c with UIT=1ms

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Cycle time = 17ms   => 58.8Hz
```

3h - Measure `Cycle = f(UIT)`

Setup idem **3c w/o DMA interrupt, no wipe**

UIT	[ms]	1	5	10	15	20	25	50	100
Cycle	[ms]	21	20	30	31	40	41	72	120

```
Cycle = 1.03 × UIT + 18ms
```

Setup idem **3c w/o DMA interrupt, 1 wipe**

UIT	[ms]	1	5	10	15	20	25	50	100
Cycle	[ms]	21	31	30	41	40	61	100	200

```
Cycle = 1.05 × UIT + 25ms
```

3i - Idem 3c with Output _LR and window split

NB: still this mode shall be properly handled so as to merge the 2 windows halves before performing the image processing. Also it sets hard constraints on the window size and position as it shall be located exactly on the middle of the chip (vertical position is free).

UIT=10ms
1 Window [17×34] starting at (239;239)
Offsets IPLLX=2, IPLLY=1, IPURX=0, IPURY=1

```
Cycle time = 23ms   => 43.5Hz
```

3j - Typical FS-Chop setup with 2 windows in center of chip

UIT=10ms
No wipe between exposures
Window #1 [34x34] starting at (280;232)

Window #2 [34x34] starting at (330;250)
Image processing on Window #1 only
Centroid: Threshold -3sigma
Background evaluated from image
Extrema calculation
Offsets `IPLLX=2, IPLLY=1, IPURX=0, IPURY=1`
    ⇨ Calculation on sub-image [32×32]

```
Cycle time = 32ms   => 31.2Hz
```

4 - Conclusions

Tests could be performed with and w/o DMA completion interrupts.
The polling mode only plays a role for large images when the image data reorganization
can be performed in parallel with the readout.

Image processing does not impact on cycle time for UIT ≥ 10ms.

Image transfer shall be done asynchronous and at a frequency of max. 1Hz

Window position in chip does not impact significantly on the performances
(approx. ±5%).

Output selection **__L** or **__R** does not impact on the overall performances.
In Full Frame mode w/ or w/o binning, the Outputs **_LR** are the fastest.

Maximum frequency = 58Hz with UIT=1ms (setup **3g**).

The cycle overhead is approx. 20ms for a [34×34] window (setup **3c**).
The minimum exposure time DIT= 1ms when numWipe=1,
The effective exposure time DIT=20ms when numWipe=0 and UIT≤10ms.

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