INFRARED INSTRUMENTATION

E U R O P E A N S O U T H E R N O B S E R V A T O R Y

Organisation Européenne pour des Recherches Astronomiques dans l'Hemisphère Austral
Europäische Organisation für astronomische Forschung in der südlichen Hemisphäre

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VERY LARGE TELESCOPE

Infrared Array Control Electronics

(IRACE)

Design Description

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1 Introduction

1.1 Scope

This document contains the design and implementation plan for the Infrared Array Control Electronics System (suggested acronym IRACE). Principal purpose of IRACE is to operate the infrared array detectors for ISAAC. The modular design allows use of IRACE for all types of IR arrays independently of the number of output channels.
All design details described in this document are based on the results of extensive analog and digital simulations and the results obtained with prototype functional modules.

1.2 Reference Documents

Applicable Documents

[1] VLT Electronic Design Specification VLT-SPE-ESO-10000-0015
[2] Electromagnetic Compatibility and Power Quality Specifications Part 1 VLT-SPE-ESO-10000-0002.
[3] Electromagnetic Compatibility and Power Quality Specifications Part 2 VLT-SPE-ESO-10000-0003.
[4] VLT Environmental Specification VLT-SPE-ESO-10000-0004.
[5] ISAAC: Thermal Flux and Readout Speed VLT-INS-93/0101
[6] VLT Medium Resolution Infrared Spectrometer Imager (ISAAC) VLT-PLA-ESO-14100-0001
[7] IRACE – Detector control software VLT-SPE-ESO-14100-0843

Additional Documents

[8] The Transputer Databook, Third Edition, Inmos 1992.
[9] ALTERA™ Devices Data Book".
[10] 1 Gbaud Transceiver SIEMENS

2 Design of IRACE

The ESO Infrared Detector High Speed Array Control and Processing Electronic IRACE is designed as a modular system and supports readout and data processing of arrays with four as well as multiple output channels. In addition the system can handle multiple separate arrays and routes the data to multiple processing chains. Detector front-end(s) are galvanically separated from data processing and system administration with fiberoptic links. A Key component of the system is a 1 Gigabit/s fiber optic link. The link not only transmits data, the architecture of the system allows distribution of data to the multiprocessor system(s) in a flexible and simple way.
With the advent of big and multi output IR arrays, requirements for data acquisition systems have increased. The electronic part of a data acquisition system consists of the detector front-end and a data acquisition computer or multiprocessor system for multi output arrays. The low noise detector front-end and the data acquisition computer are galvanically isolated, to avoid ground loops. Galvanic isolation by means of fiber optics is the normal case for detector data acquisition systems used in astronomy. An additional advantage of fiber optics is the ability to go over longer distances at high speed, e.g. between telescope and control room e.t.c..
The ESO IR data acquisition system is primarily build for the VLT instrument ISAAC, which will be equipped with a 4 output channel 256x256 or if available with a 32 output channel 1024x1024 pixel InSb array, in the long wavelength channel from 2.5 to 5um and a MCT 1024x1024 array for the short wavelength channel from 1 to 2.5um. The requirements for data transmission between the detector front-end and the data acquisition computer system are high , e.g. for double correlated sampling at filter L with a scale of 0.2268”/pixel, we expect a flux of 1.84E06 ph/s per pixel (based on measurements with the ESO IRAC1 camera at the 2.2m telescope). That gives a data rate of ~ 4E08 bits/s for 16 bit ADC’s and an array with 32 parallel output channels. But even in the low background bands J,H and K, it is preferable working with multiple, non destructive sampling and linear regression analysis, what gives best results at short readout times per frame, but corresponding high frame and data rates.
To process in real time the continuos stream of data a SUN multiprocessor system based on Sun Ultra Sparc is used. For higher computing power requirements data can be distributed to a net of Ultra Sparc systems.
The system consists of four main groups (see Figure 1 System block diagram) :

- **IR array detector with the differential drivers for the data lines**
- **Data Acquisition Front-end**
- **System Administration**
- **Number Cruncher**

The IR array detector is placed inside the vacuum vessel and the differential data line drivers for the analogue signals are located as close as possible to the detector. There are three terminals on the vessel, the data, the clock and the bias terminal.

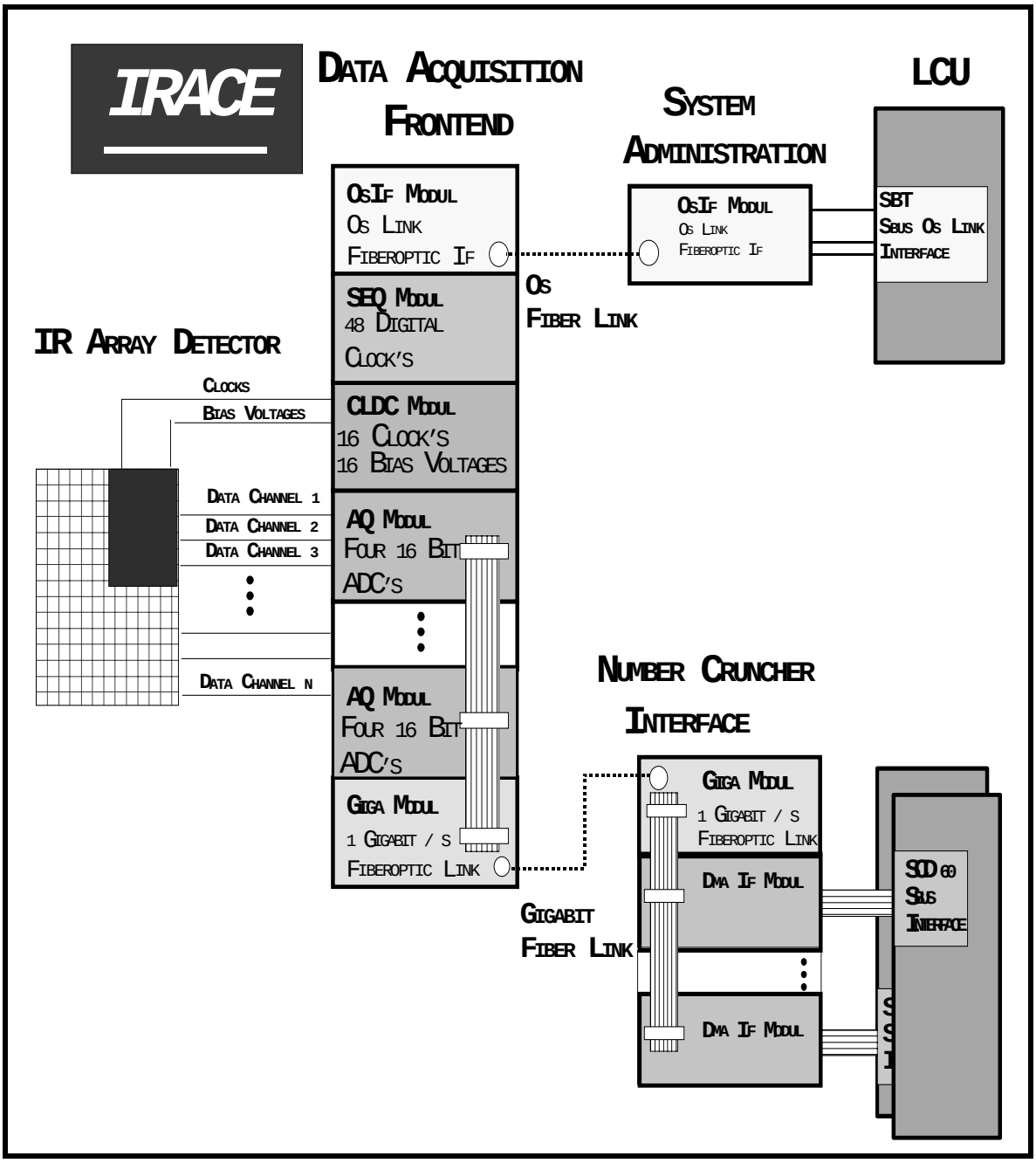


Figure 1 System Block Diagram

3 Detector Front End Electronics (DFE)

DFE consists of at least five boards, standard double Euro card size, placed in a VME size crate.

- **SEQ** **Sequencer**
- **CLDC** **Clock/Bias driver**
- **AQ** **ADC's and Preamplifier's**
- **TIF** **Transputer Fiber optic Link Interface**
- **GIGA** **High Speed Data Link**

Sequencer as well as clock/bias driver and ADC modules can be cascaded, to adapt to individual system requirements.
TRAMs or Transputers [8] are used on every board needing computing power. These are SEQ, CLDC and TIF. They realize (together with the root transputer in the LCU) a distributed multiprocessor system. On AQ and GIGA there are no transputers necessary.

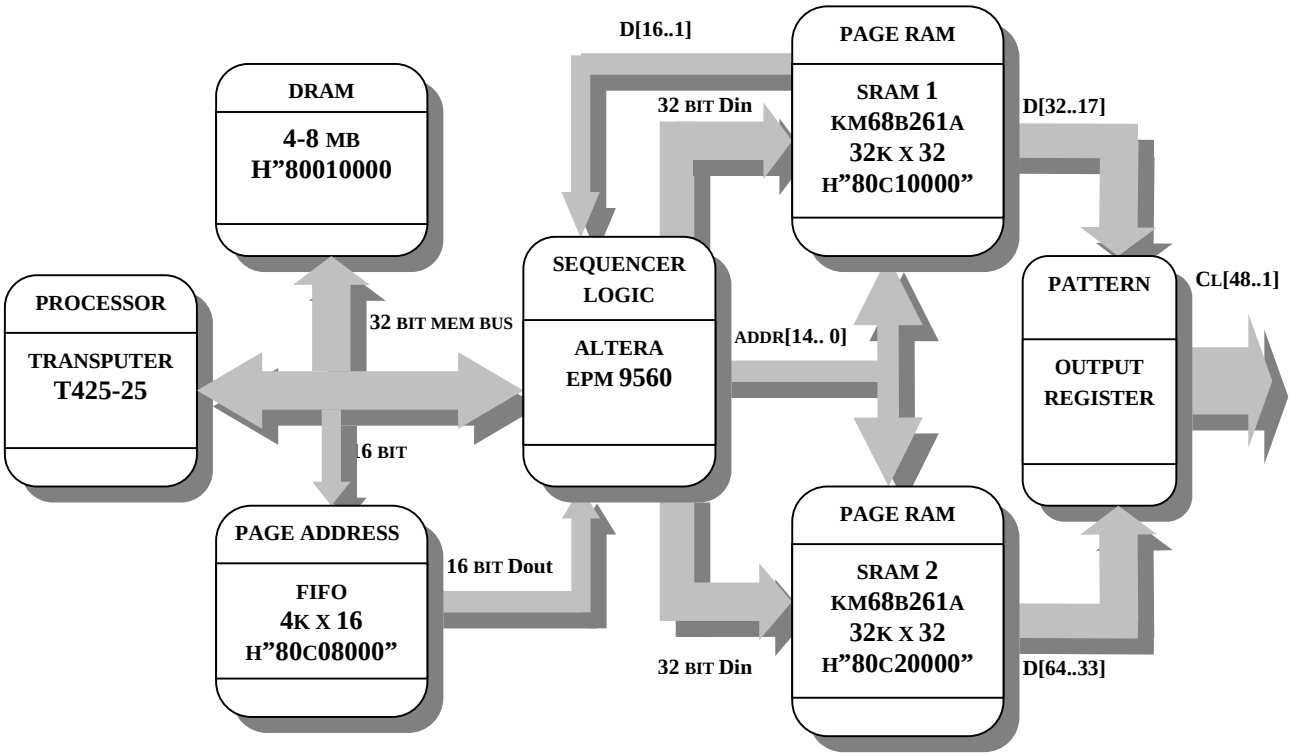
3.1 Sequencer (SEQ)

3.1.1 FEATURES

Double Euro size module
48 digital clocks
Time per word from 50 ns to 6350 ns
Page organized patterns
Page size 128 words of 48 Bits wide - 256 pages
Page repeat from 1 to 63
Quartz time base

3.1.2 GENERAL DESCRIPTION

SEQ is a page oriented clock pattern sequencer with a quartz time base of 50ns. The Sequencer (fig. 2) system processor [9] is a 32-bit transputer (T425) with 8 MBytes DRAM. The words of a page are sequentially output, each word has an individual time count. Pages are held in a SRAM, 32K deep and 64Bits wide. Bit 0 to 6 determine the lifetime of the pattern and Bit 15, if set, states the end of a page. Bit 16 to 63 of a word are output as digital clocks, so there are 48 TTL clocks available.. The maximum page length is 128 words. The time per word is between 50ns and 3.5µs, depending on Bit 0 to 6.
A sequence can run an infinite amount of time by continuously reloading the page address FIFO with new page addresses by the system processor from the DRAM. The system processor gets interrupts when the FIFO is less than half full and the event enable of the control register is set (Control register Bit 7). This enables Block transfers and fast FIFO reloads. The sequence stops, if the FIFO is empty.



FIFO DATA WORD

D15	Disable output reg update[48..33]
D14	Disable output reg update[32..17]
D13-8	Loop count [5..0]
D7-0	Page addr [7..0]

SRAM 1 DATA WORD

D15	End of page
D14	End marker
D13-7	Reserved
D6-0	Time count [6..0]

Status
H"80C06000"

D2	Seq running
D1	/FIFO full
D0	/FIFO empty

SRAM 1_Databit[31..16] = Clcok [16..1]
SRAM 2 Databit[15..0] = Clcok [32..17]
SRAM 2 Databit[31..16] = Clcok [48..33]

Control
H"80C00000"

D7	Event enable
D5	Chopper mode
D4	FIFO clear
D2	Seq start

Figure 2 Sequencer – Simplified block diagram

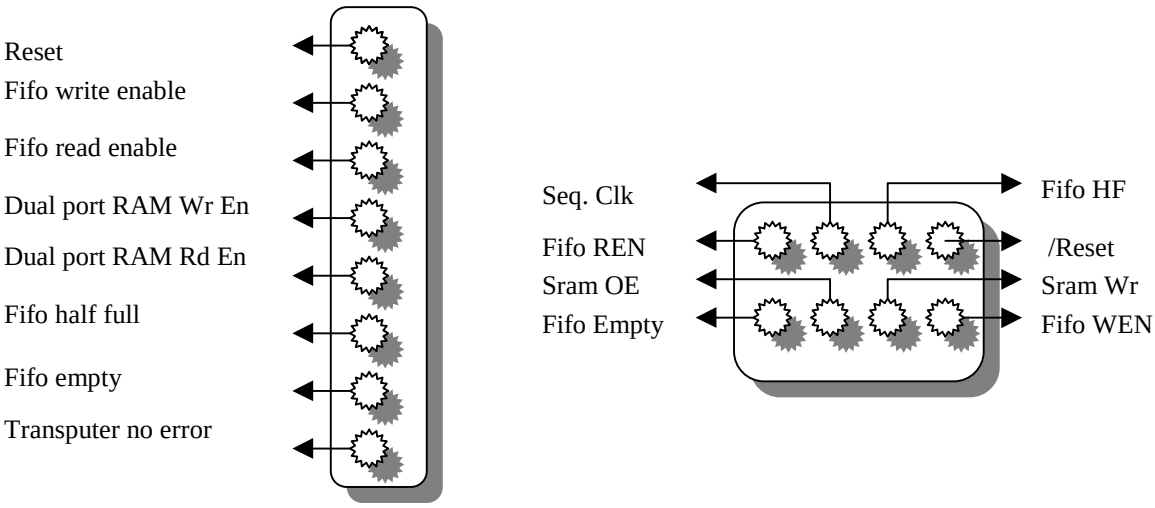


Figure 3 Sequencer – Front Panel LED's

DEFINED AREA	HARDWARE BYTE ADDRESSES FROM	TO
NOT DEFINDED	#80C30000	...
FIFO	#80C08000	#80C10000
SRAM2	#80C20000	#80C21000
SRAM1	#80C10000	#80C11000
SEQUENCER STATUS BITS	#80C06000	#80C06000
SEQUENCER CONTROL BITS	#80C00000	#80C00000
EXTERNAL MEMORY OF TRANSPUTER (4-8 MB)	#80401000	#808010001
INTERNAL MEMORY OF TRANSPUTER		

Figure 4 Transputer addresses for Sequencer module

3.2 DC Bias and Clock Driver (CLDC)

3.2.1 FEATURES

Double Euro size module
16 low noise analogue clocks out of 16 TTL signals
16 low noise bias voltages
Telemetry of clock and bias voltages
Temperature stable precise reference voltage

3.2.2 GENERAL DESCRIPTION

The Module provides 16 clock and 16 bias voltage generators with a maximum continuous output current drive of 36mA and an amplitude range of +/-10V. Clock high / low levels and the bias voltages are generated by 12-bit DAC's and following operational amplifiers. The clocks are produced by fast CMOS multiplexers (HI-201HS) switching between the outputs of the high or the corresponding low level operational amplifiers of a clock driver. Their input switch signal is a TTL signal from the backplane P2 connector. Clocks and Bias voltages are output on the backplane P2 connector. On board telemetry is done with a 12–bit ADC (3.3 μsec conversion time) connected to the input of the analog switches, via analog multiplexers. At power-up, the clock and bias outputs are disabled (10KOhm to GND). The outputs can be enabled through software. A voltage references circuit provides stable voltages for the DAC's . CLDC's system processor is a T225 transputer.

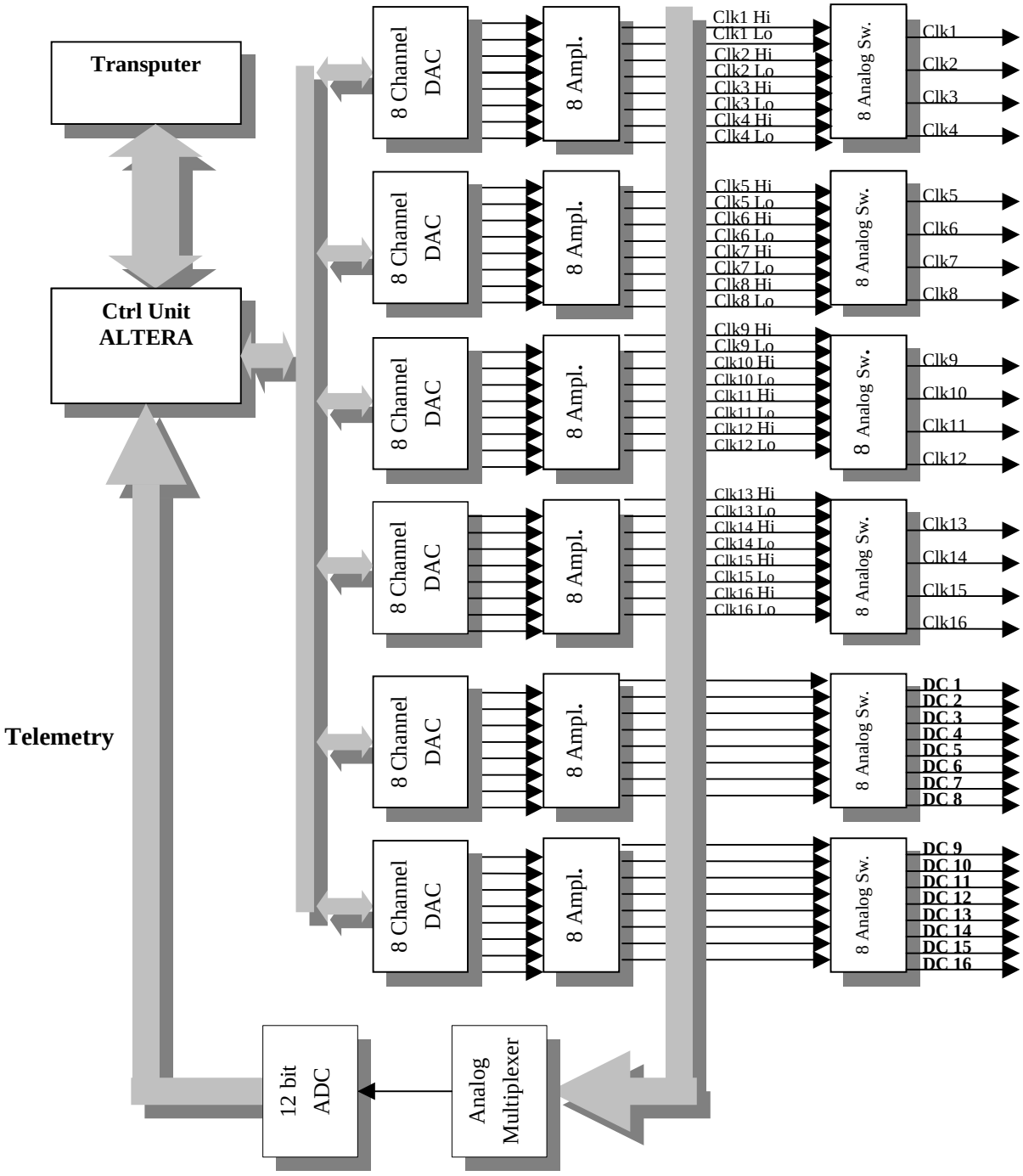


Figure 5 CLDC - Simplified block diagram

DEFINED AREA	HARDWARE BYTE ADDRESSES
RESET	#7FFB
OUTPUT ENABLE	#7FF6
DAC DATA	#7FDC
DAC CLOCK	#7FDE
DAC LOAD	#7FE2
SELECT TELEMETRY CHANEL	#7FF2
ADC CONVERT	#7FFC

Figure 6 Transputer memory addresses for CLDC module

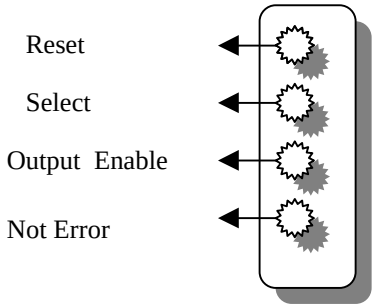


Figure 7 LED's of CLDC module

3.3 Acquisition Module (AQ)

3.3.1 FEATURES

Double Euro size module
True differential analog inputs
Four fast 500 ns ADC's
Low noise design
Delay for ADC convert signal - software/hardware controlled up to 3 us by 200 ns steps
AQ modules can be cascaded
Two different signal gains - selectable by software
Two different signal filters - selectable by software
FIFO buffered ADC data
Monitor of ADC-inputs and the convert signal via front panel LEMO's

3.3.2 GENERAL DESCRIPTION

The acquisition module has four channels and contains minimum digital logic, so that low-level analog signals are not disturbed by digital noise. The differential analogue input signals of each channel are input to an instrumentation amplifier followed by a low pass filters in front of the ADCs. A conversion command triggers the ADCs, the data are immediately transferred to a FIFO and then to the output registers. The convert signal has a programmable delay from 0 to 3 usec in steps of 200 nsec.
Each acquisition module can internally be set to be a master module. It then generates a header code, corresponding to the number selected on a hex switch. It then puts out first a header word followed by the ADC data. If the module is not a master it just puts out the ADC data to the front panel synchronous GIGA bus.

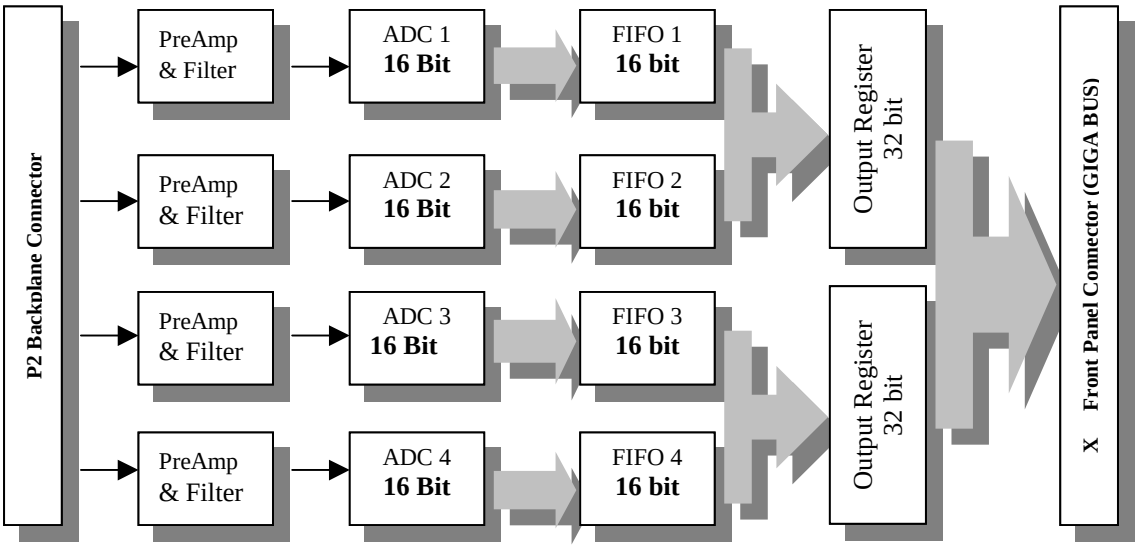


Figure 8 Video Processor - Simplified block diagram

Board Jumpers

JP6	enables the on module quartz to generate the data clock signal (used only for test setup ! normally not set)
JP7	reserved
JP8	Slave module if set otherwise master module
JP54 - JP57	3-pin jumper. configures the ADC input range
SW1	hex switch for setting the board header.
SW2	hex switch for setting the delay factor for the ADC convert signal.
SW3	hex switch for setting the status address of the AQ module.

STATUS INPUT REGISTER (WRITE ONLY)		STATUS OUTPUT REGISTER (READ ONLY)	
Bit7		Bit7	FIFO empty
Bit6		Bit6	FIFO full
Bit5	Gain on / off	Bit5	Gain on / off
Bit4	Filter on / off	Bit4	Filter on / off
Bit3	Soft Delay Factor [3..0]	Bit3	Soft Delay Factor [3..0]
Bit2		Bit2	
Bit1		Bit1	
Bit0		Bit0	

Figure 9 Status register of AQ module

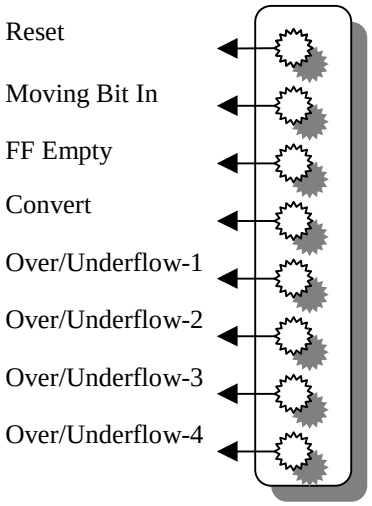


Figure 10 LED's of AQ module

3.4 High Speed Data Link (GIGA)

3.4.1 FEATURES

Double Euro size module
High speed fiber channel transmission of 1062.5 Mbaud (one gigabit / sec)
Up to two kilometers fiber length possible
32 bit wide data input and output
Data input and output FIFO buffered

3.4.2 GENERAL DESCRIPTION

GIGA is a VME 6HE module. It is a fiber optics transceiver with a transmission speed of 1gigabit/s and uses for serial transmission a modified FIBERCHANNEL protocol. Data enter the module on the front panel X connector from the synchronous Giga Bus to the fiber optics transmitter and the serial data from the fiber optics receiver leave the module to the synchronous Giga Bus on the VME P2 connector. The protocol and pin-out of the parallel bus is identical on transmitter and receiver side.
Input and output data are FIFO buffered. The Transceiver hybrid itself (SIEMENS V23806) has a 32 bit wide data input and output and a 4 bit command input and output. The command signals are transmitted like data and are used to form the protocol of the parallel Giga Bus.

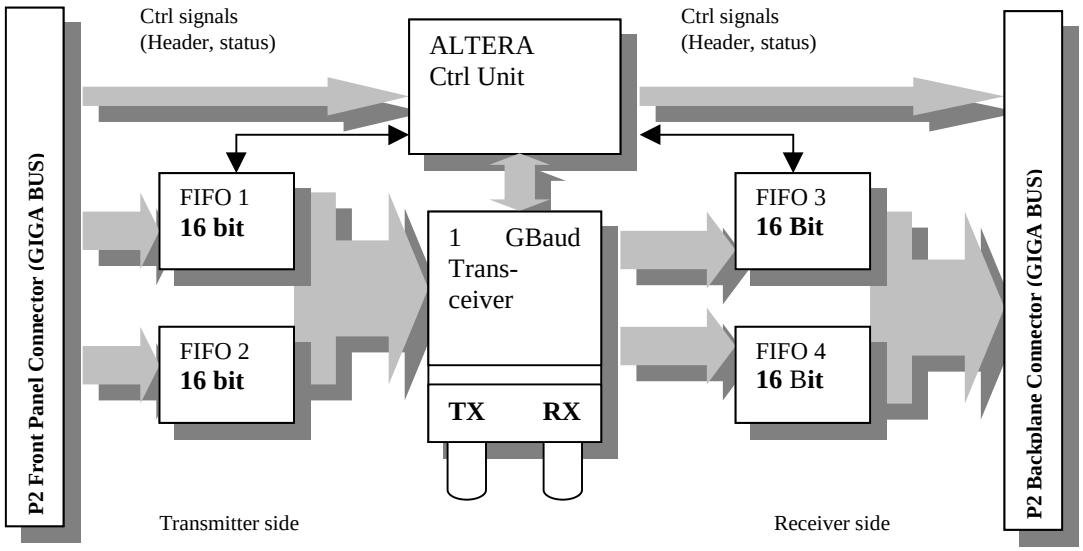


Figure 11 GIGA LINK - Simplified block diagram

3.4.2.1 Giga Bus

Figure.10 shows the layout of the GIGA Bus. A 96-pin DIN 41612C is the physical bus connector . Signal lines are placed between ground lines, to establish a defined impedance when 96pin ribbon cables are used. There are two busses on GIGA bus, a 32 Bit wide parallel bus and a serial bus. The parallel bus has 32 data lines and 6 control lines. Controls are DataClock, /DataEnable and Header 0 to 3. A data transmission always starts with a header word and a header value containing the address of the receiving module. Data are then transmitted with a header value 0. During transmission of data and header the /Data Enable" line is low. The receiver of the data recognizes the incoming Header and if its header code is equal, he clocks the following data with the rising edge of DataClock in. He is receiver till a data sequence with different header code arrives. The serial bus is completely independent from the parallel bus. It is used to pass status and command information to modules on the bus

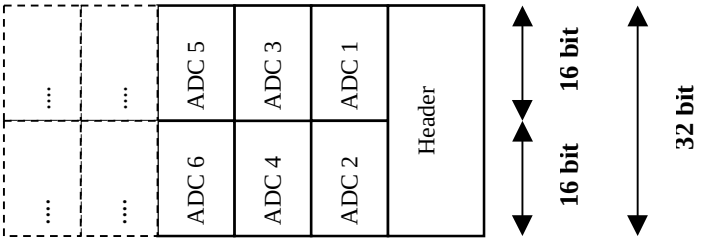


Figure 12 Data packet transmitted over GIGA BUS

Pin No.	Row A	Row B	Row C
1	Data bit 1	GND	Data bit 2
2	GND	Data bit 3	GND
3	Data bit 4	GND	Data bit 5
4	GND	Data bit 6	GND
5	Data bit 7	GND	Data bit 8
6	GND	Data bit 9	GND
7	Data bit 10	GND	Data bit 11
8	GND	Data bit 12	GND
9	Data bit 13	GND	Data bit 14
10	GND	Data bit 15	GND
11	Data bit 16	GND	Data bit 17
12	GND	Data bit 18	GND
13	Data bit 19	GND	Data bit 20
14	GND	Data bit 21	GND
15	Data bit 22	GND	Data bit 23
16	GND	Data bit 24	GND
17	Data bit 25	GND	Data bit 26
18	GND	Data bit 27	GND
19	Data bit 28	GND	Data bit 29
20	GND	Data bit 30	GND
21	Data bit 31	GND	Data bit 32
22	GND		GND
23	Header bit 0	GND	Header bit 1
24	GND	Header bit 2	GND
25	Header bit 3	GND	/Data Enable
26	GND		GND
27	Data Clock	GND	
28	GND	/Reset	GND
29	VCC	GND	VCC
30	GND	Status Line	GND
31	/Status En	GND	Status Clk
32	GND	Status Reply	GND

Figure 13 Pin Out - GIGA BUS

STATUS INPUT REGISTER (WRITE ONLY)		STATUS OUTPUT REGISTER (READ ONLY)	
Bit7		Bit7	Module Error
Bit6		Bit6	FIFO empty
Bit5		Bit5	FIFO full
Bit4		Bit4	Data transmission
Bit3		Bit3	Reserved
Bit2		Bit2	Reserved
Bit1		Bit1	Giga sync
Bit0	Reset Giga	Bit0	Reset state

Figure 14 Status register of GIGA module

3.5 Transputer Fiber Link Interface (TIF)

3.5.1 FEATURES

Double Euro size module
Fiber optic transputer link (Link in and Link out)
LED monitor of Giga Bus data lines
Control unit for status bus

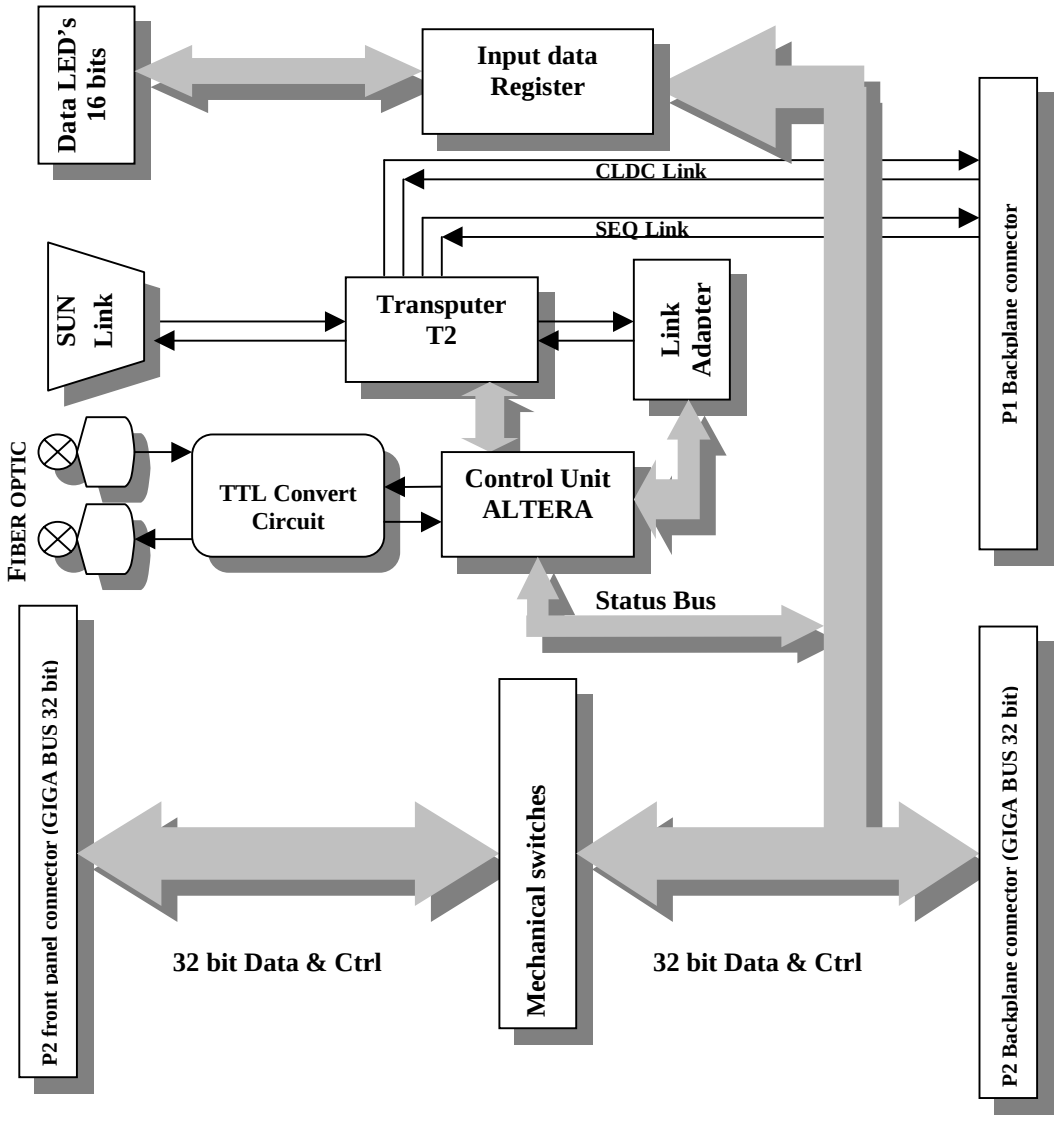


Figure 15 TIF - Simplified block diagram

3.5.2 GENERAL DESCRIPTION

TIF does primarily the conversion of the transputer link to a fiberoptic link between NC side and DFE and the distribution of transputer links in DFE. The TIF module is installed on the detector front end and on the number cruncher side and detects in which part of the system it is (NC or DFE) and configures itself automatically. In NC the transputer link from SUN Link will be routed to the fiber optic, in DFE TIF will convert the incoming fiber optic link to a tranputer link, route it to the transputer and de-multiplex the link signal into two other links. Over backplane the first is connected to the Sequencer (SEQ) link chain and the second to the clock driver (CLDC) link chain. If more than one sequencer is installed, the link is routed down through each sequencer. The same applies for the clock driver.

3.5.2.1 Status Bus

Control I/O to all connected modules without transputer can be done via the status bus, which exists both on the front-end and on the number cruncher side. The STATUS BUS is a part of GIGA BUS as shown in Figure 10
The control unit for the status bus is on the TIF module. Figure 14 shows a simplified block diagram of the status bus on the DFE side. It is produced by the TIF Transputer via link adapter. A unique module number is assigned to each module in the system. Status information can be requested from each module and. some hardware configuration can be done, using the status bus, like setting filter, gain, delay of convert puls on the AQ module and so on.

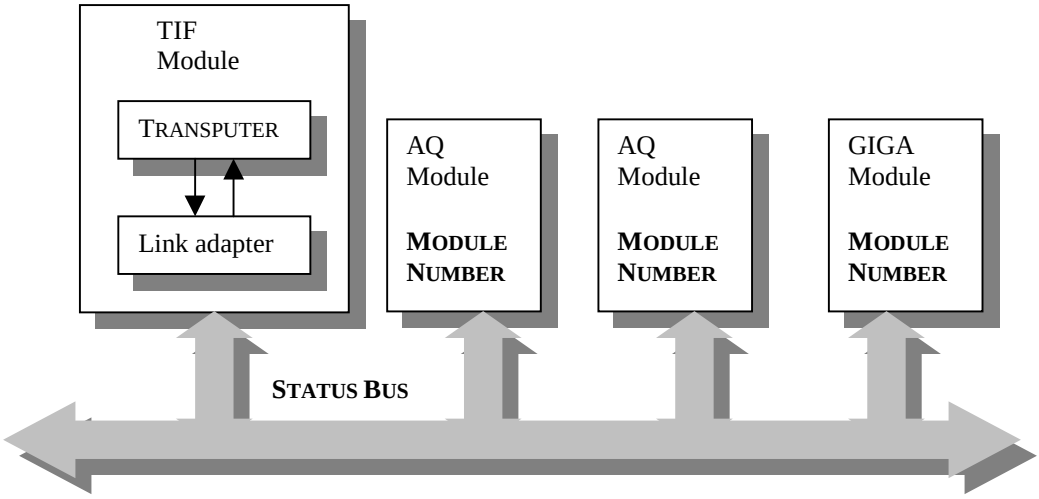


Figure 16 STATUS BUS - Simplified block diagram

The status of a module can be read with the following protocol:
Command : <NC/DFE> , <Module number> , <Address of internal Reg.>
Reply: <Result value>
Each module can be written with the following protocol:
Command : <NC/DFE> , <Module number> , <Address of internal Reg.>
<Set value>
Description:
<NC/DFE>: On which side of the system is the module. Number 0 for NC and 1 for DFE
<Module number> : The address of the accessed module
<Address of internal Reg.>: The address of the register on the accessed module (default value is 0)
<Set value>: The set value for the register of accessed module
<Result value>: the result of the command
Caution: *Each module has a different input and output register structure.*

The set values and the Result value should match individually.
An example:
To send a command to an AQ module on the DFE side with module number 7:
Write command: 1 7 0 6

Interpretation:
1) The module is on DFE side = 1
2) Module number = 7
3) The first output register of module is selected = 0
4) Delay factor = 6 (function only for AQ module)

To read the status of an AQ module on the DFE side with module number 7:
Write command: 1 7 0
Response : 86

Interpretation:
1) The module is on DFE side
2) Module number = 7
3) The first output register of module is selected = 0
4) Delay factor is 6 and FIFO is empty (only valid for AQ module)

3.5.2.2 LED Monitor

Incoming data over the GIGA BUS can be monitored with 16 LED's (16 bit data). There are two switches on the front panel of the TIF module, header and bus switch. They determine the data packet and the data word to be monitored.
If the HEADER SWITCH and the incoming data packet header are identical, the packet is selected. The BUS SWITCH determines which data word in the selected packet is shown by the LED's.
For example, if the bus switch is set to two (beginning with zero) then the high word (16 bits) of the second word will be shown

Jumpers and switches

JP1 Enables front panel LED's
JP3-6 Connect the front panel giga bus with the backplane
JP10 3-pin jumper- selects the link speed of the link adapter
Sw1 Header switch
Sw2 Bus switch

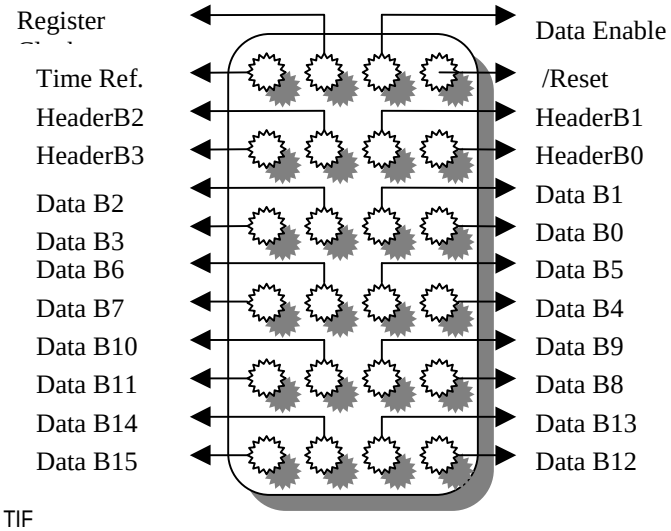


Figure 17 LED's of TIF

4 System Administration and Number Cruncher

The modules on the NC side are installed in a standard VME crate. They have only Sysreset and power connection to the VME bus. The following IRACE modules are installed

- **TIF** **Root Transputer for DFE, Fiber Link Interface**
- **GIGA** **High Speed Fiber Link**
- **DMA-IF** **Interface Gigalink Bus to NC DMA controller**
- **NC** **The number crunching facility.**

4.1 Transputer Fiber Link (TIF)

Identical module as on DFE side. See description above.
It configures in the NC side crate itself automatically, so that the front panel link to the system administration is enabled and the links to the back panel P1 are disconnected.

4.2 High Speed Fiber Link (GIGA)

Identical module as on DFE side. See description above.
The Giga Bus output used to connect to the DMA_IF is on the back panel P2.

4.3 Interface Gigalink Bus to NC DMA controller (DMA-IF)

4.3.1 FEATURES

Double Euro size module
Interface between GIGA BUS and SCD 20(or 60) SUN SBUS DMA interface
20 (60) Mbyte/s Data Rate from GIGA BUS to SUN SBUS DMA interface

4.3.2 GENERAL DESCRIPTION

DMA-IF interfaces the Giga Bus to the SUN Sbus DMA controller SCD 60 (20). The 32Bit Giga Bus enters on P2 the DMA-IF. In an Altera PLD all logic for header recognition is done and the 32Bits of Giga Bus are de-multiplexed to the 16Bit size of the SUN Sbus DMA controller. From Altera the data are feed into a FiFo. The Fifo output runs into a voltage level conversion circuit with the appropriate signals for SCD20 (TTL) or SCD60 (LVTTL). The appropriate driver circuits are installed at module assembly. The module can than only be used either for SCD20 or SCD60 !

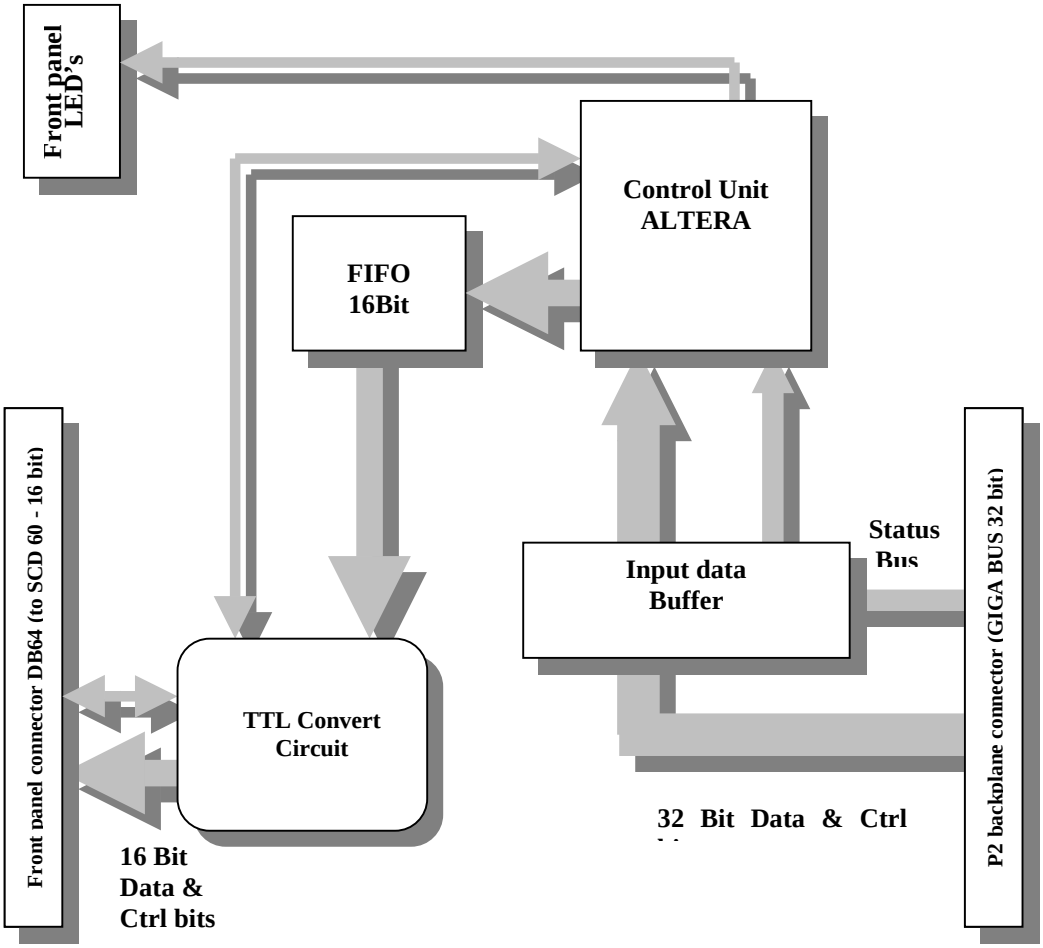


Figure 18 DMA-IF module - Simplified block diagram

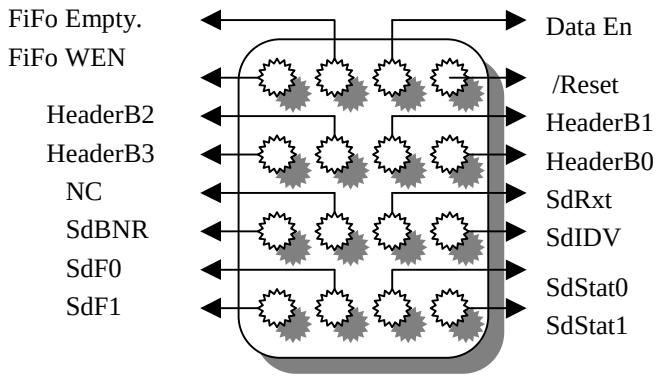


Figure 19 DMA-IF module - Front Panel LED's

4.4 Number Cruncher (NC)

Commercial ULTRA SPARC computer(s) manufactured by SUN Microsystems.

5 DFE Crate and Backplane

The DFE crate is a VME size crate and uses the standard DIN connectors at P1 and P2 position. On P1 are only digital signals, the 5V digital power supply and the digital ground are at the nominal VME location. Digital signals are the transputer links, SysReset and the global 25MHz clock and the derived sequencer clock. . Communication between modules is only done by transputer links over the P1 connectors of the modules On P2 are mainly analogue signals corresponding to the individual modules installed. These are the analogue power supplies and analogue ground, clock driver produced biases and clocks, the differential signals to the ADC boards (AQ) and the convert strobes from the sequencer to the AQ boards.
The location of the modules within DFE is fixed by the back plane layout.

6 NC Crate and Backplane

The NC crate is a VME size crate and uses the standard DIN connectors at P1 and P2 position. The P1 connector is on a standard VME bus, but the IRACE modules use only power and SysReset. On the modules P2 position a small Gigalink back plane is installed.

7 Power Supply

7.1 Power Generation

Creation of all voltages (+5V DIG, +/-5V , +/–15V) of DFE from KNIEL commercial power supplies.

7.2 Power Consumption

The estimated power consumption is 150…300 Watts depending on configuration (1…32 detector outputs).

8 Grounding and Shielding

To avoid ground loops and pickup the telescope/instrument structure is connected to the DFE common ground point like cryostat, detector shield and DFE crate. Shielded cables interconnect cryostat and DFE, where the cable shield is connected to the metallic crate of DFE. All data transmission from and to DFE from the NC side is done by fiber optic links. The crate must be electrically floating in order to avoid multiple earth connections.

9 Cables and Connectors

Connections between DFE and LCU will only be by means of fiber optics. The maximum distance will be 1Km, so that even operation of a detector front-end from the distant locations is possible.

9.1 Host Link (DFE↔NC Side)

Duplex fiber optics transputer link (2 lines) with embedded subsystem control signal RESET. The maximum length of this cable is 2 Km.

9.2 Data Link (DFE ↔ NC Side)

Fiber optics duplex high speed links (one giga baud). The maximum length is 2 Km.

9.3 DFE Internal Wiring (DFE Back Plane ↔ DFE Back Panel)

Connection from back plane 96-pole DIN 41612C connectors at CLDC and AQ to back panel military connectors. Twisted pair cable per detector channel for the detector signals, coax lines for biases and the clocks.

9.4 Cryostat Link (DIB ↔ CRYO)

Military connector cables between DFE back panel and cryostat.
There is one twisted pair cable per detector channel for the detector signals, coax lines for biases and the clocks. The detector signal lines for each detector are in one cable, the same applies for the biases and clocks.

10 Mechanical Dimensions

The standard board size is 230×160 mm² (double Euro Board format). The bus connector is a 96-pole DIN 41612C. The size of the crate may vary with the actual system configuration, number of boards etc. For the single Infrared Array configuration an overall size of 300×150×300 mm³ is anticipated.

11 System Configuration

The system is designed to accomodate all types of infrared arrays. The modular approach allows many different system configurations. The basic configuration is for four quadrant IR arrays. A 32 output IR array does not change the basic sceem, only eight AQ boards have to be installed and connected to a 32 channel backplane.

12 Performance Specifications

Preliminary performance specifications are given in Table 1.

Clock pattern time resolution:	50 ns
Noise @ 20 kpixels/sec .	≤ 20 µV RMS
Gain mismatch between channels:	≤ 2%
Gain drift:	≤ 100 ppm/°C
Max. number of ADCs	No limit-modular system
Dynamic range of video chain:	≥ 50,000
Range of bipolar voltages:	−10.0..+10.0 V
Resolution of output voltage setting:	< 0.1 V
Absolute error of output voltages:	≤ +/– 0.1 V
Telemetry range:	−10.0..+10.0 V
Resolution of telemetry system:	≈ 0.01 V
Relative error of telemetry system:	≤ 0.2 %
Temperature drift of output voltages:	≤ 50 ppm/°C
Max. number of DC output voltages (multiples of 16) :	no limit-modular system
Max. number of independent clocks (multiples of 16) :	no limit-modular system
Clock rise and fall times (10V amplitude):	≤ 100 ns
Power consumption (4 channel system):	≤ 150 Watts
Power consumption (32 channel system):	≤ 300 Watts

Table 1. Performance of system