IRACE
The ESO Controller for Infrared Arrays

(Infrared Array Control Electronics)

European Southern Observatory

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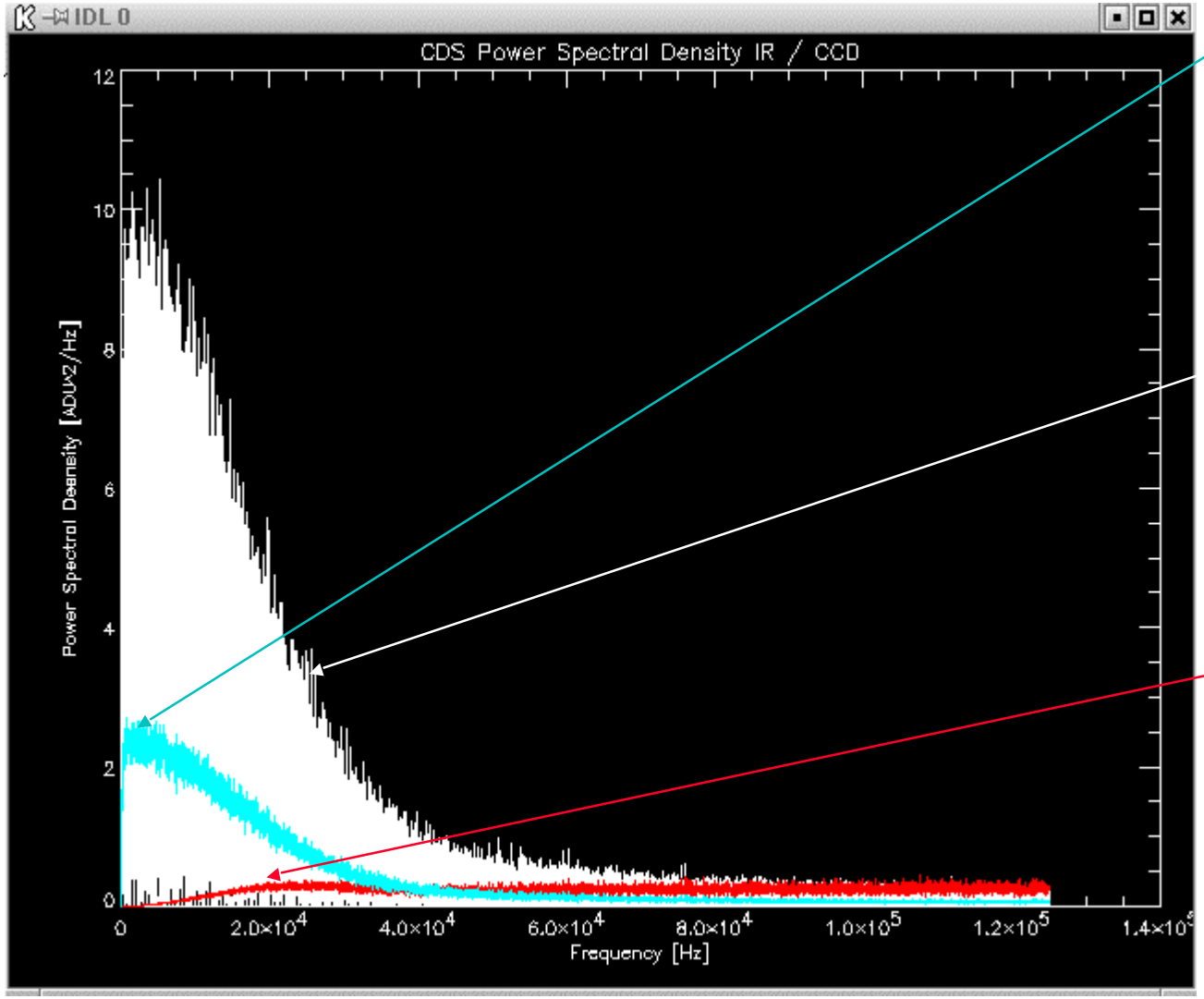
Speaker: Gert Finger

Outline

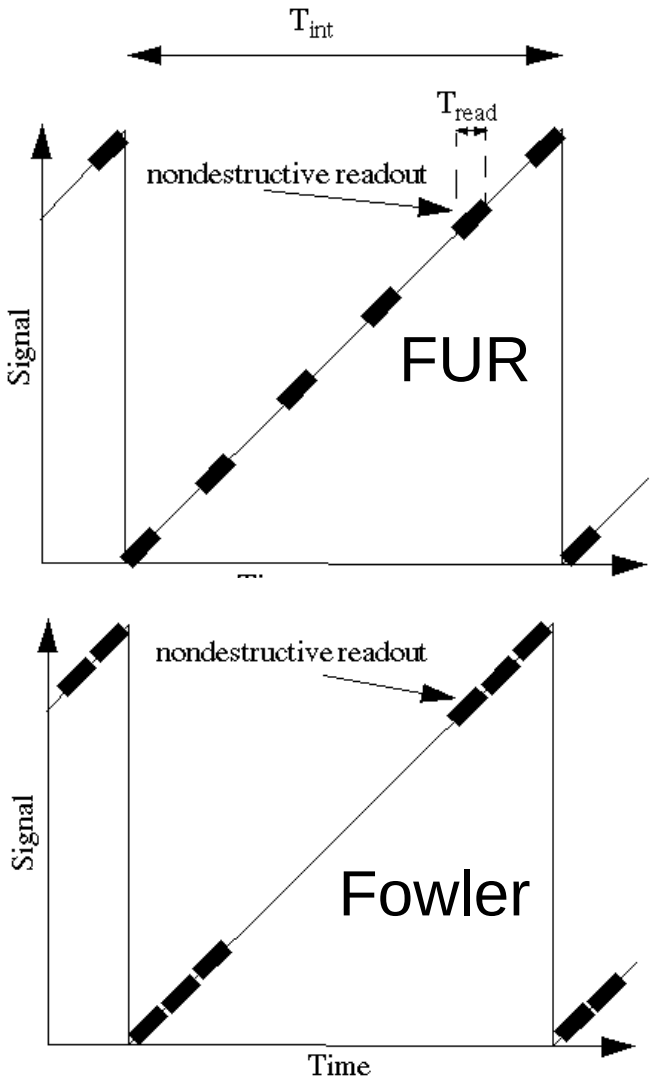
- Special controller needs for IR detectors
- IRACE data acquisition system
- IRACE detector control software DCS

Double correlated sampling Infrared / CCD



- Blue curve:
  power spectral density of
  Picnic 256x256 MBE
- $|N_{CDS}|^2=|N_{DET}|^2 * |H_{CDS}|^2$
  $|H_{CDS}|^2=[2-2\cos(2\pi f t_s)]$
- White Curve Infrared:
  dc coupled
  t_s = 1 sec (can be >1000s)
  fully sensitive to
  1/f noise and 50 Hz
- Red curve CCD
  t_s = 4 µsec
  no 1/f noise and 50Hz

Noise reduction by multiple nondesdructive readoutds



- Follow-up-the-ramp sampling (FUR):
  at equidistant time intervals nondestructive readouts
  least squares fit: slope of integration ramp

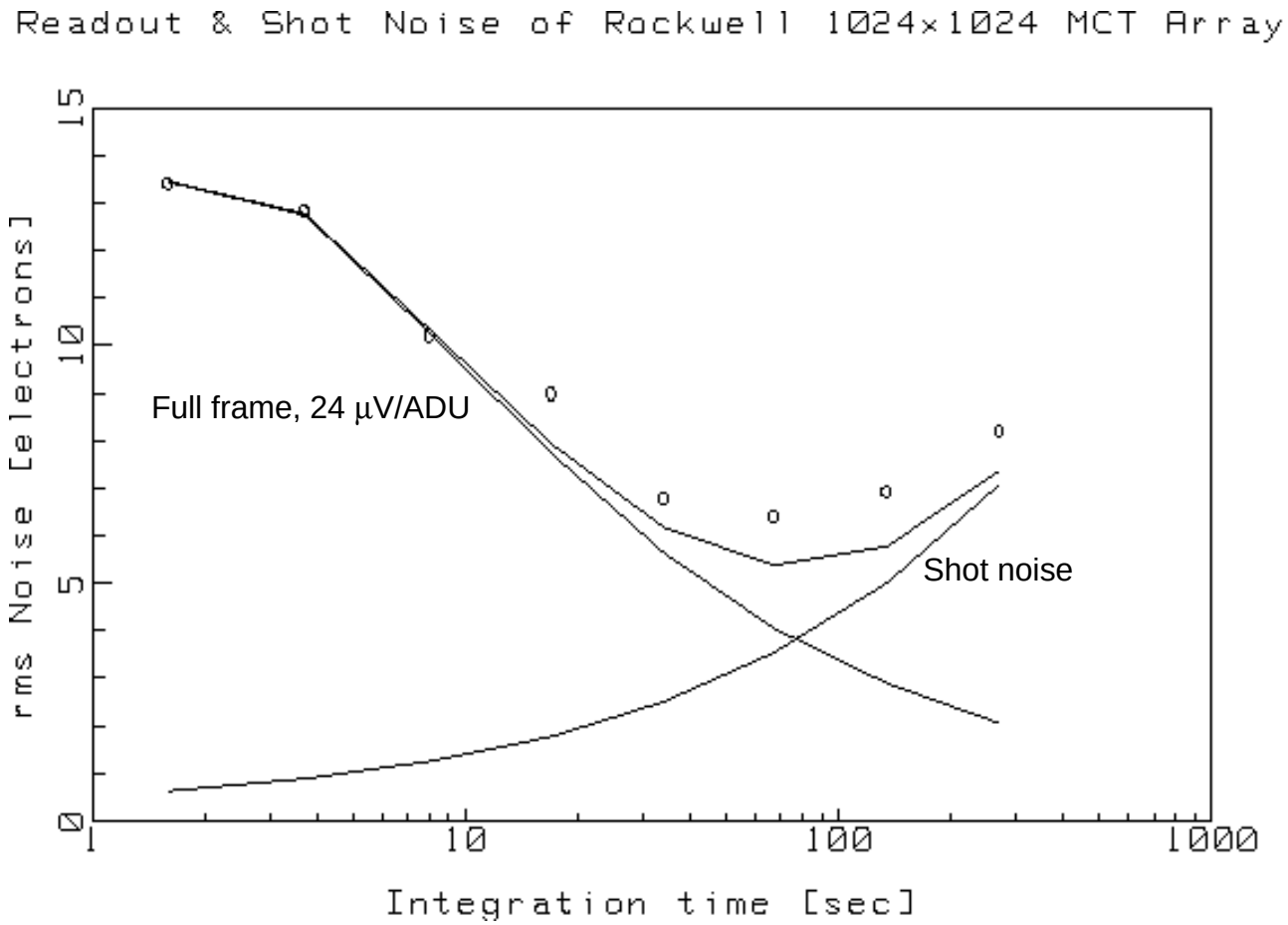
$$SNR_{FUR} = SNR_{DC}\sqrt{\frac{n(n+1)}{6(n-1)}}$$

- Fowler:
  nondestructive readouts at start and at end of ramp
  least squares fit: slope of integration ramp
  for n>>1:

$$SNR_{Fowler} = SNR_{DC}\sqrt{\frac{n}{8}} \cong SNR_{FUR}\sqrt{\frac{6}{8}} \Leftrightarrow T_{\mathrm{int}} = nT_{\mathrm{Re}ad}$$

$$SNR_{Fowler} = SNR_{DC}\sqrt{\frac{n}{2}} \cong SNR_{FUR}\sqrt{3} \Leftrightarrow T_{\mathrm{int}} >> nT_{\mathrm{Re}ad}$$

Readout Noise versus number of nondestructive readouts



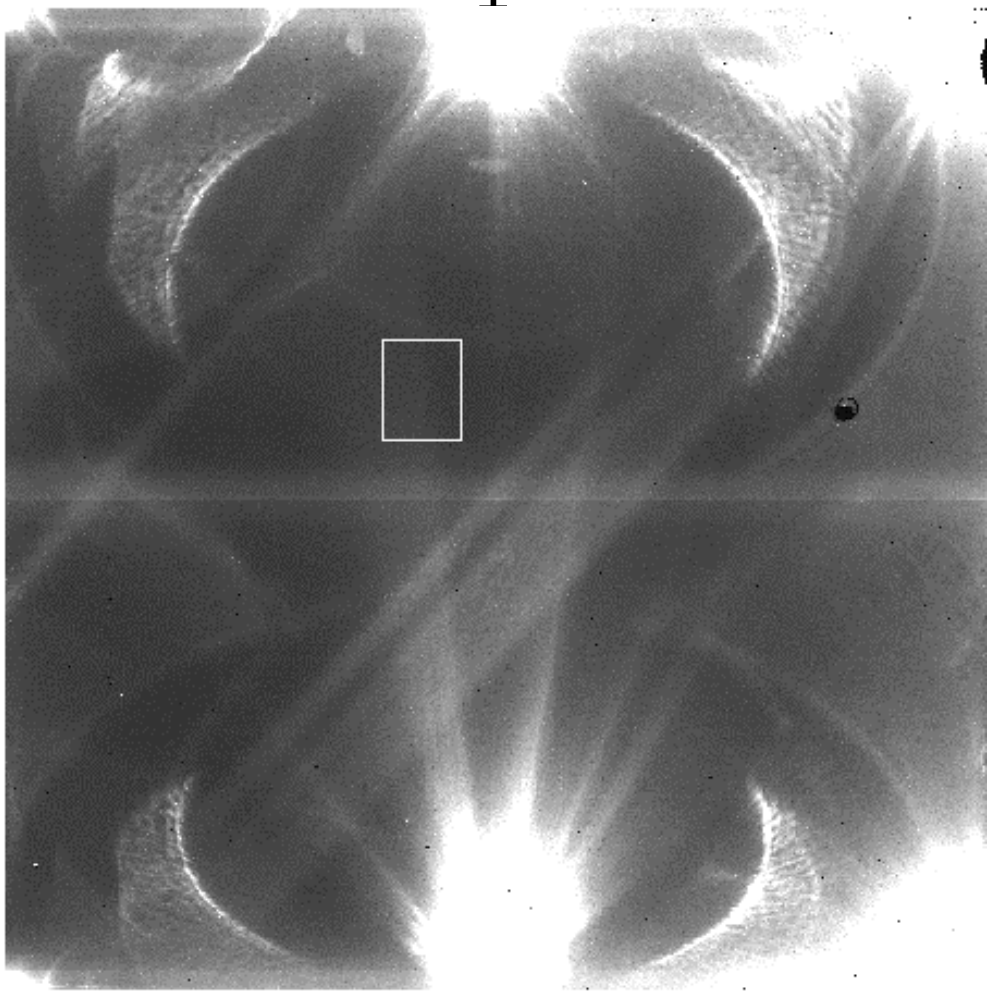
Follow-up-the-ramp sampling:
number of readouts n
proportional to integration time

$\sigma^2_{mult}/\sigma^2_{dc}=6(n-1)/(n(n+1))$

frame rate 1Hz, 64 nd samples
integration time 67 sec
rms noise 6.3 electrons

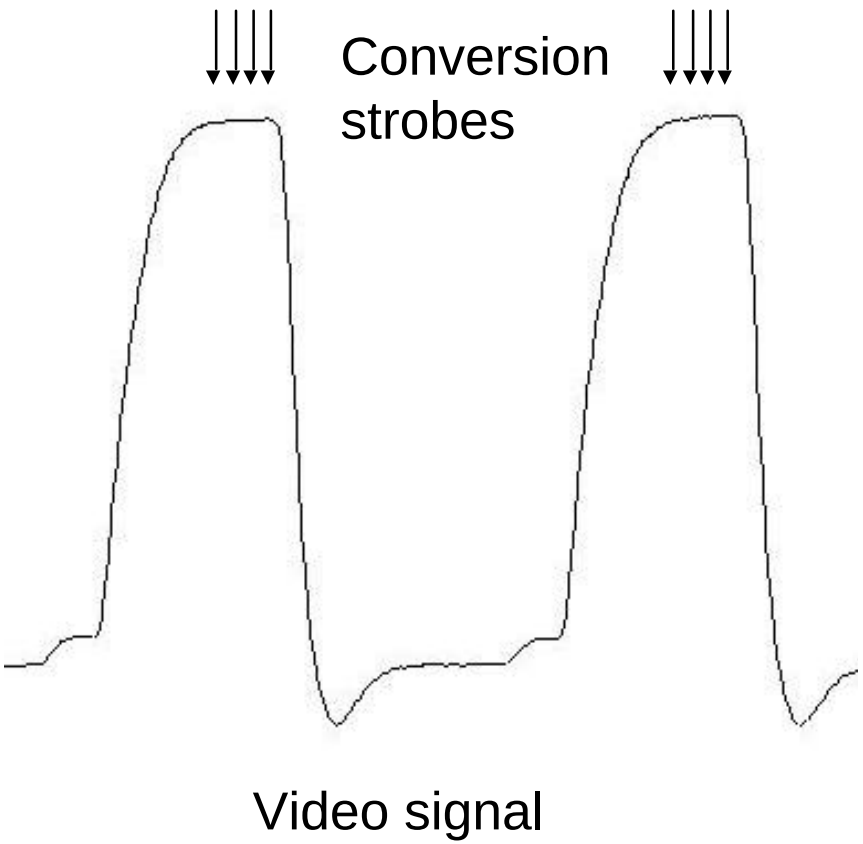
darkcurrent of 30 e/hour too small for shot noise

Shot noise of shift register glow



- shift register glow localized at four points on edges (1,4) and in corners (2,3)
- Remark: arcs are due to reflection of light emitted by glow centers

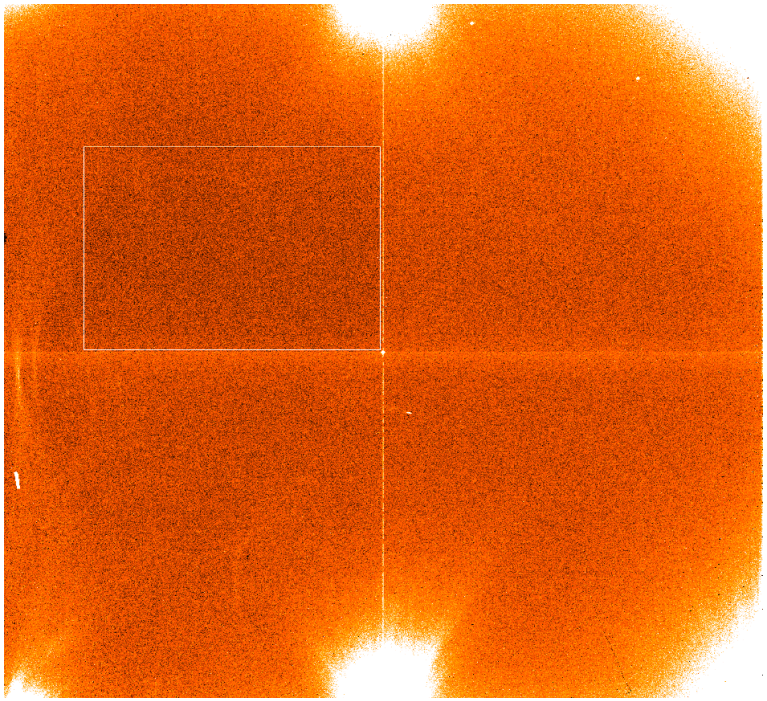
Subpixel sampling to reduce shift register glow



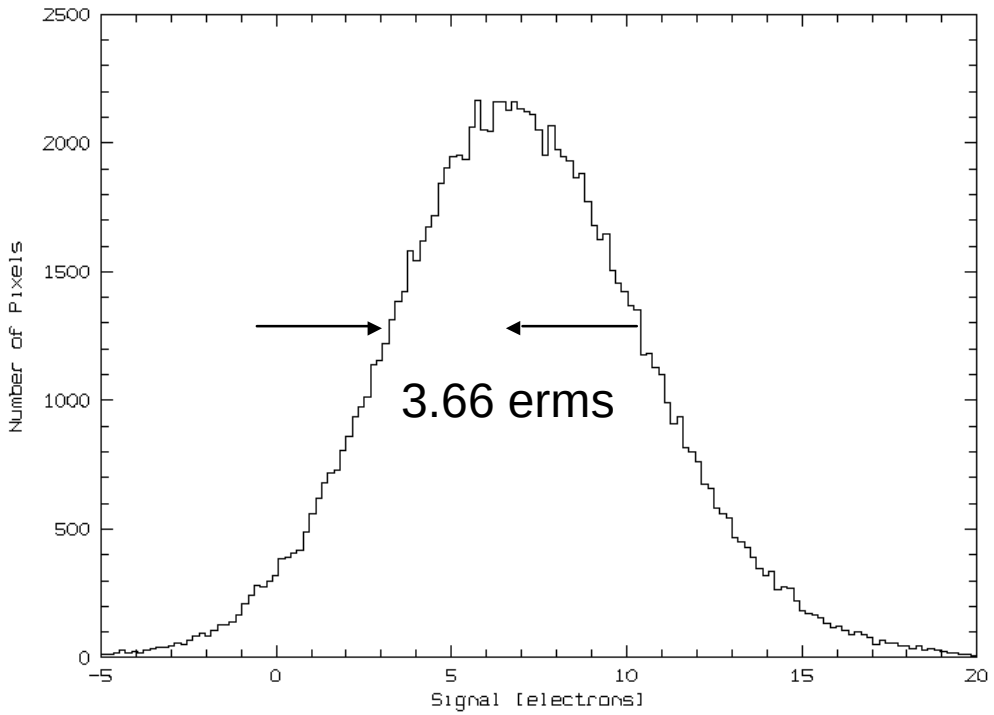
- On-chip amplifiers not used: no glow
- only source of glow is addressing of pixels
- reduce addressing (number of readouts)
- increase number of conversions per pixel
- sufficient samples to beat down noise without glow penalty

Noise of Hawaii LPE raw image on stabilized integration ramp

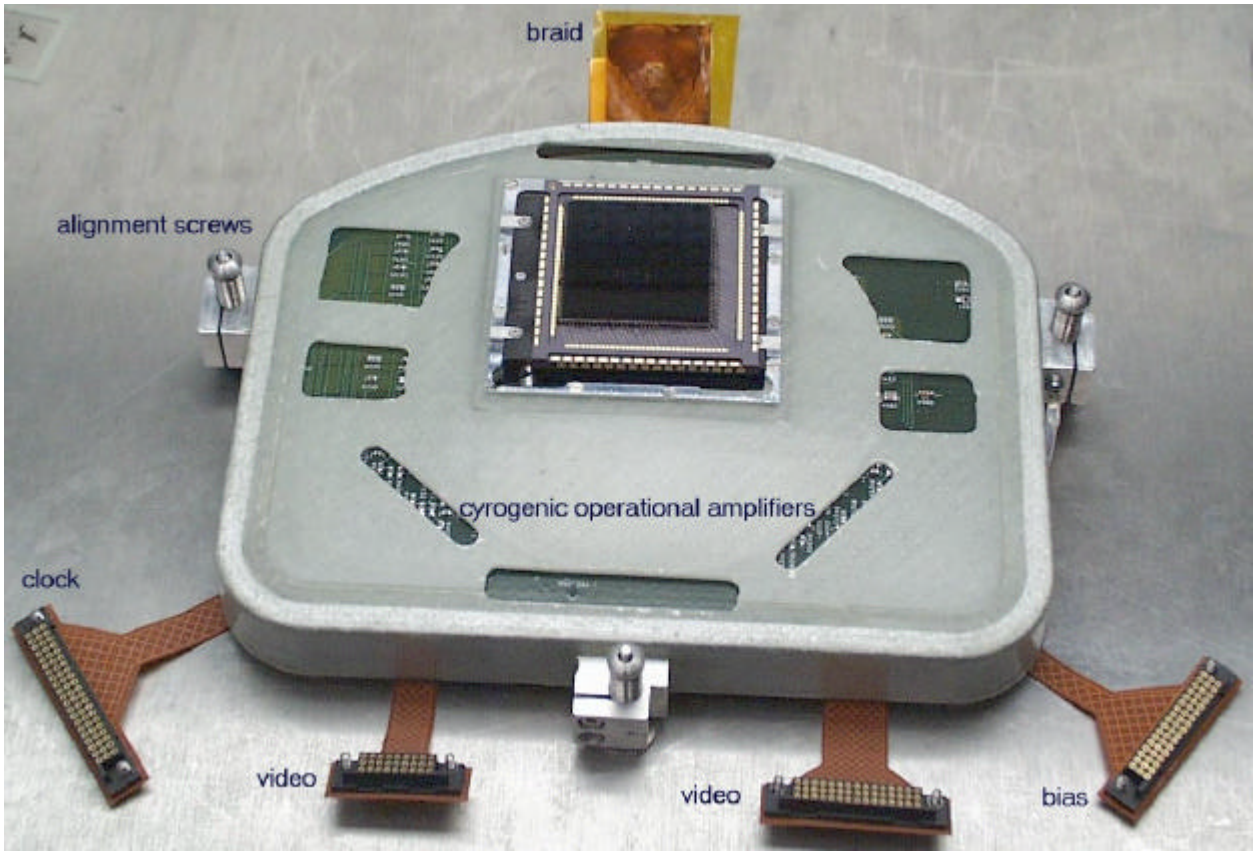
- Introduce delay > 30 s after reset
- with 32 fowler pairs uniformity of raw image 3.66 e rms pixel to pixel
- no difference required : equivalent noise of 2.6 e rms
- discontinuity at quadrant borders: < 4 electrons



Dit = 60 s , Cuts -5 / 40 electrons



Hawaii2 2Kx2K LPE HgCdTe engineering grade



- Hawaii 2Kx2K LPE HgCdTe engineering grade array
- 32 video + 4 reference channels
- Readout time: 800 msec
- RON : 10 erms double correlated
- QE H-Band : 0.81

Status:

- engineering grade array delivered and tested
- science grade array delivered
- cryogenic clamp circuit for 4 reference outputs manufactured

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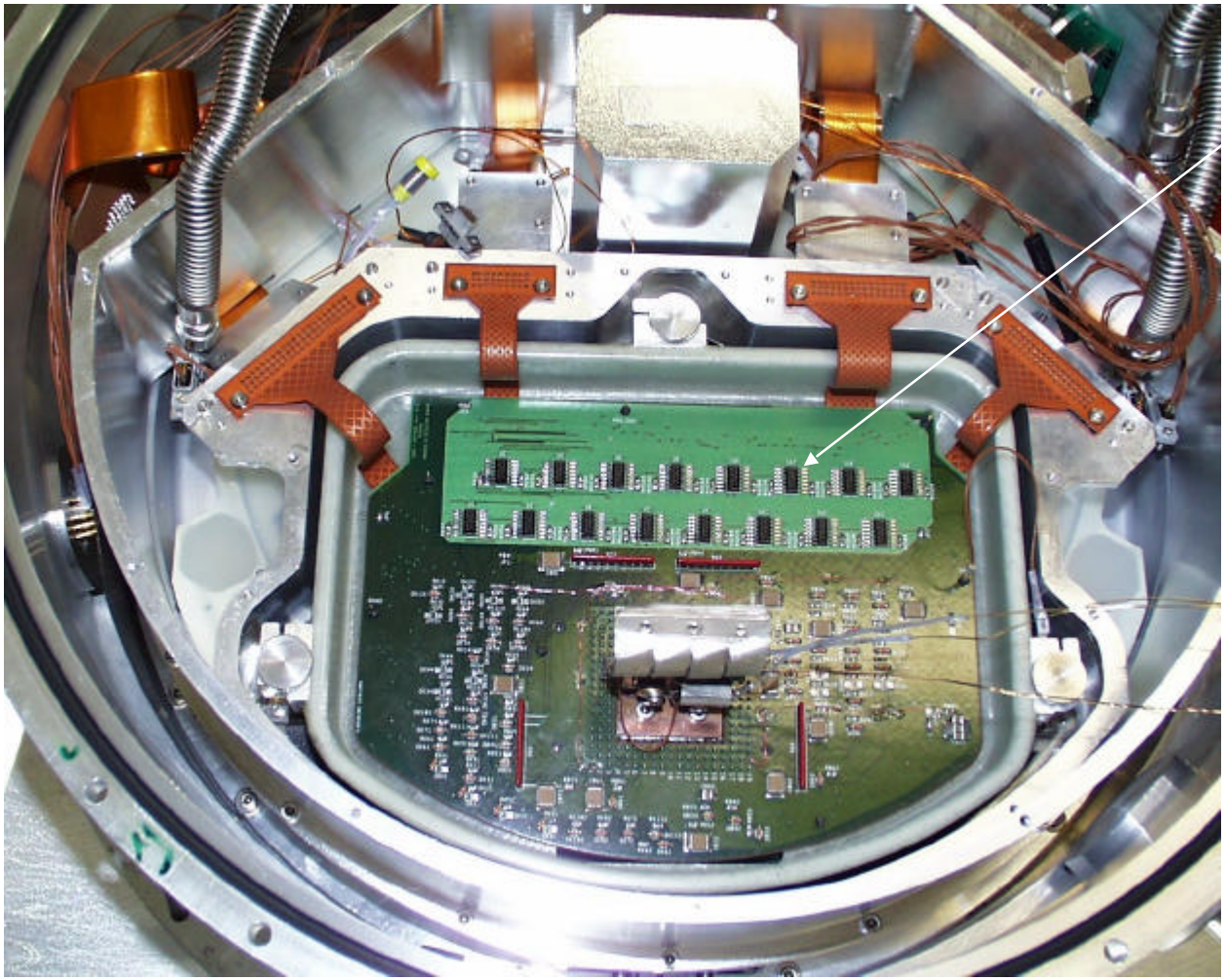

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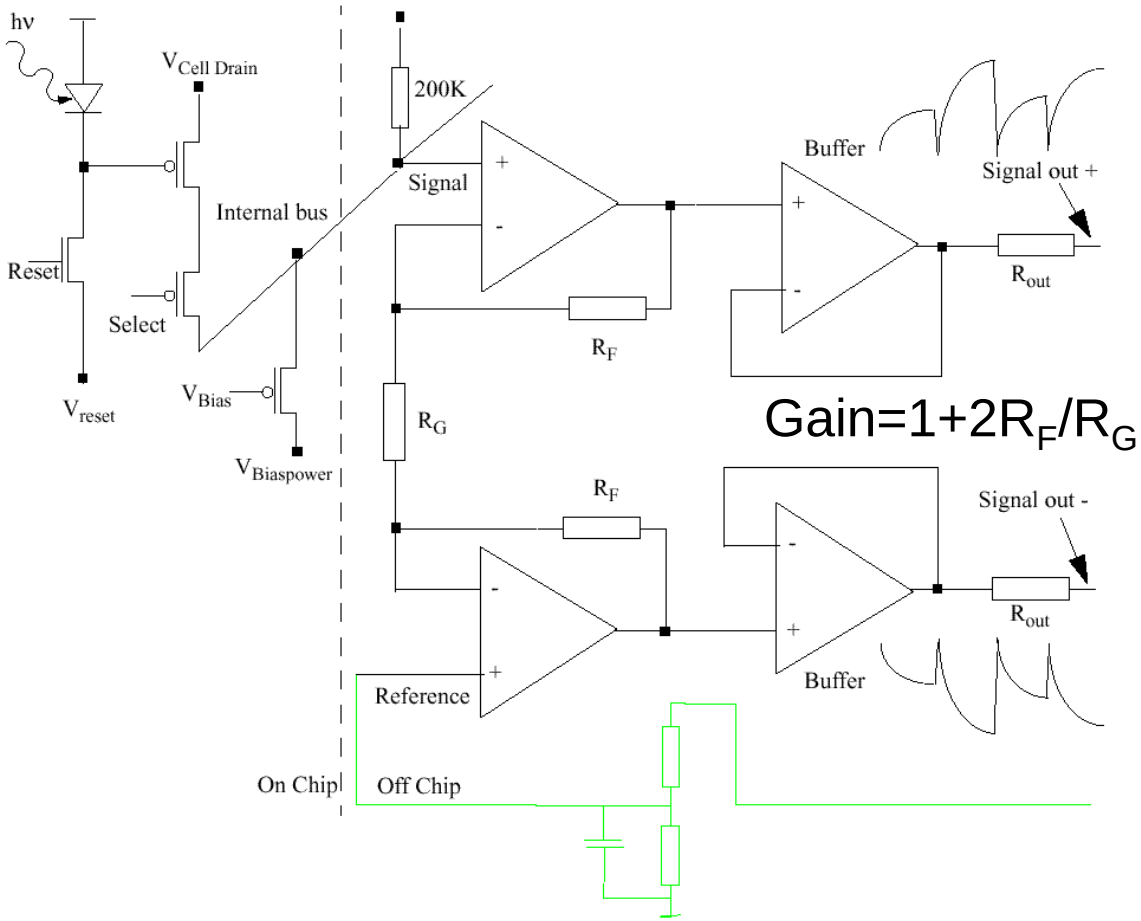
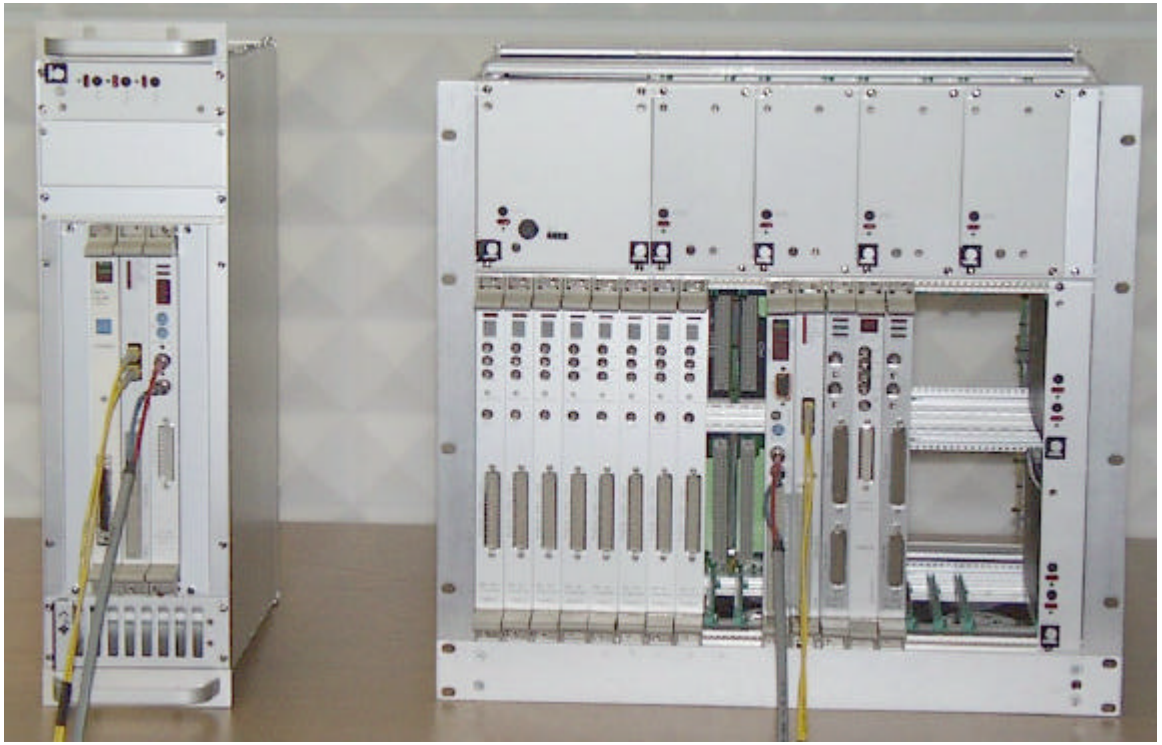
On-chip MUX Unit Cell & off-chip cryogenic opamps



- On-chip source follower not used
- internal bus of detector directly connected to +5V with 200 KΩ load resistor
- linear CMOS opamp (TI LinCMOS TLC2274) 9nV/sqrt(Hz)
- contribution to read noise
  2 electrons rms
  for double correlated sampling at frame rate of 1 Hz
- reduced glow

IRACE 144 channel version



Interface
to Ultrasparc

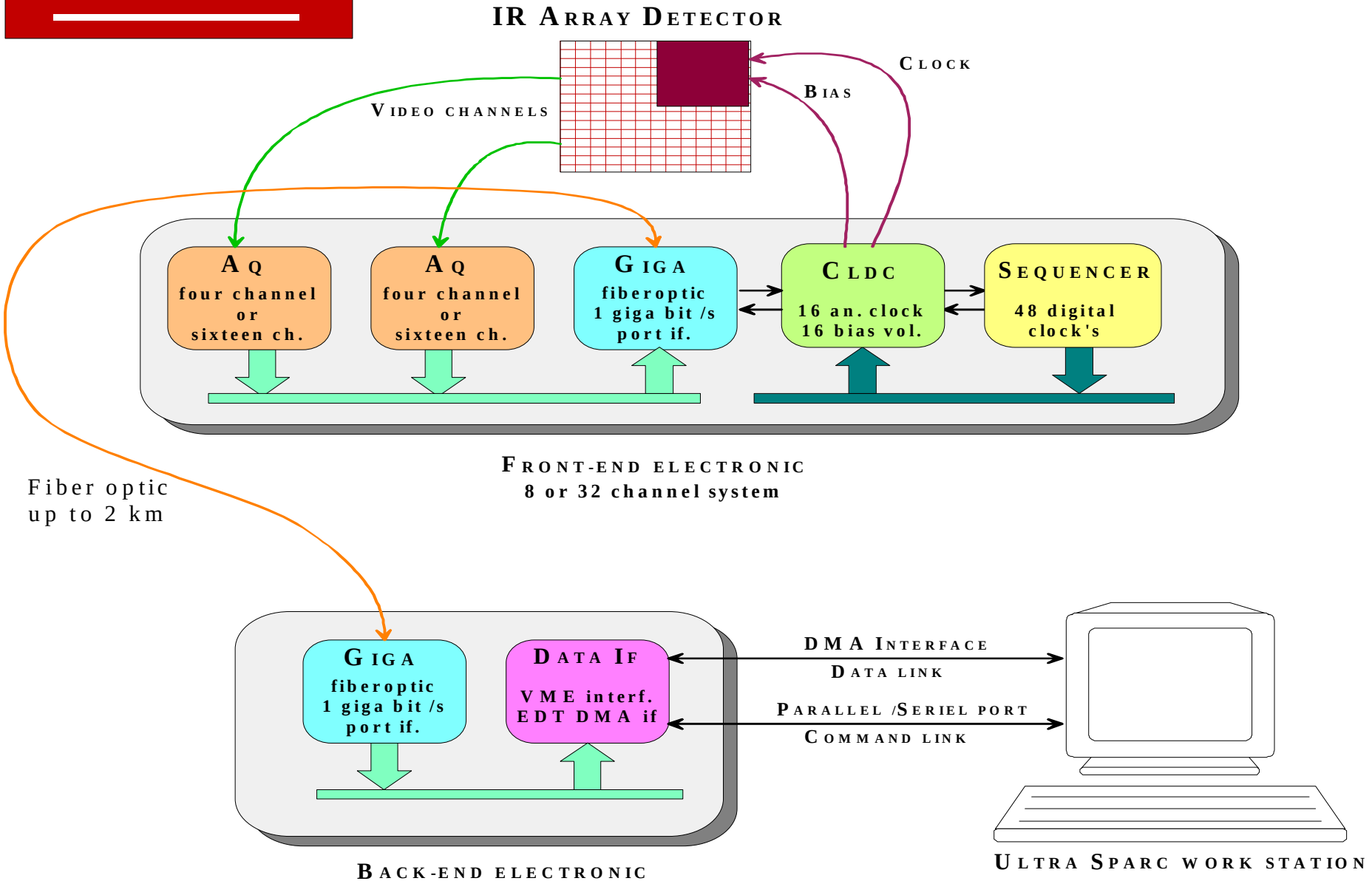
Detector front end
mounted on Instrument

- Nirmos has four 2Kx2K arrays each having 32 video channels and 4 reference channels
- new ADC boards:
  16 channels / board16 bit 500KHZ
  16x9 = 144 channel system
- readout of 4Kx4K array in 1.3 sec

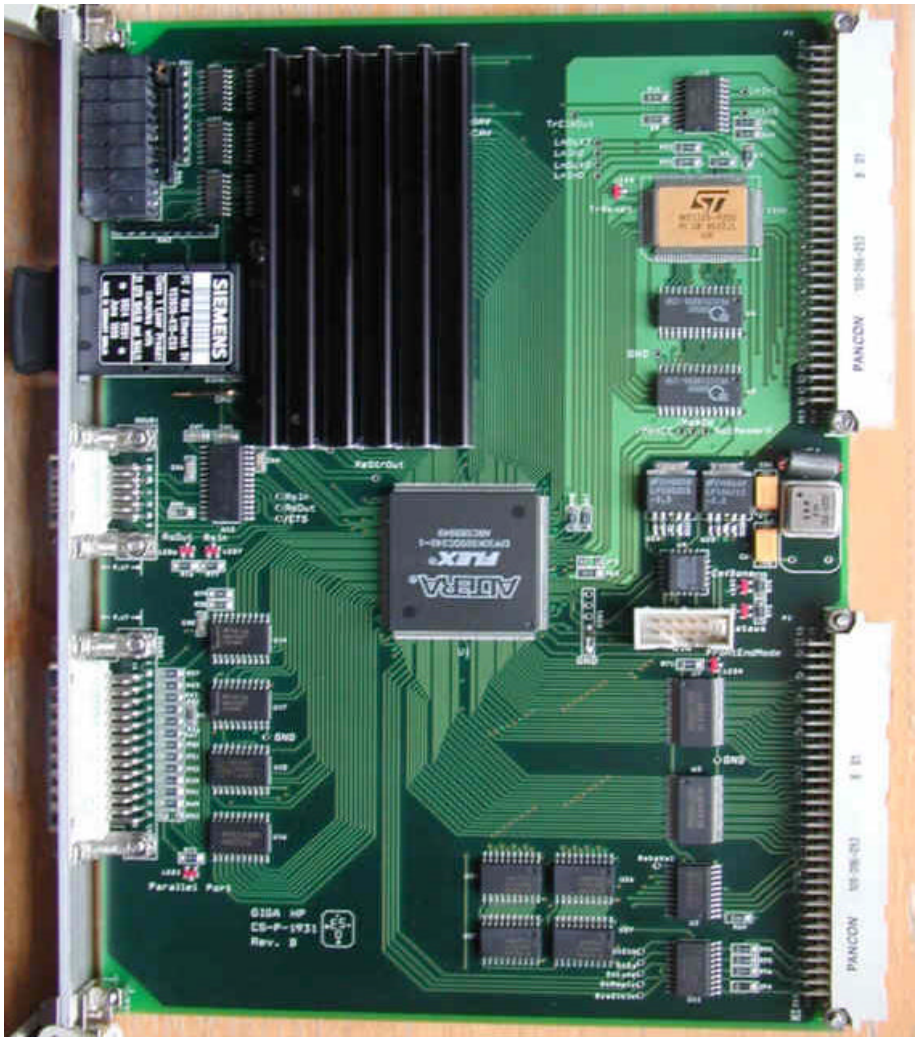
Status:

- tested with Hawaii 2Kx2K array
- 144 channel prototype tested

IRACE

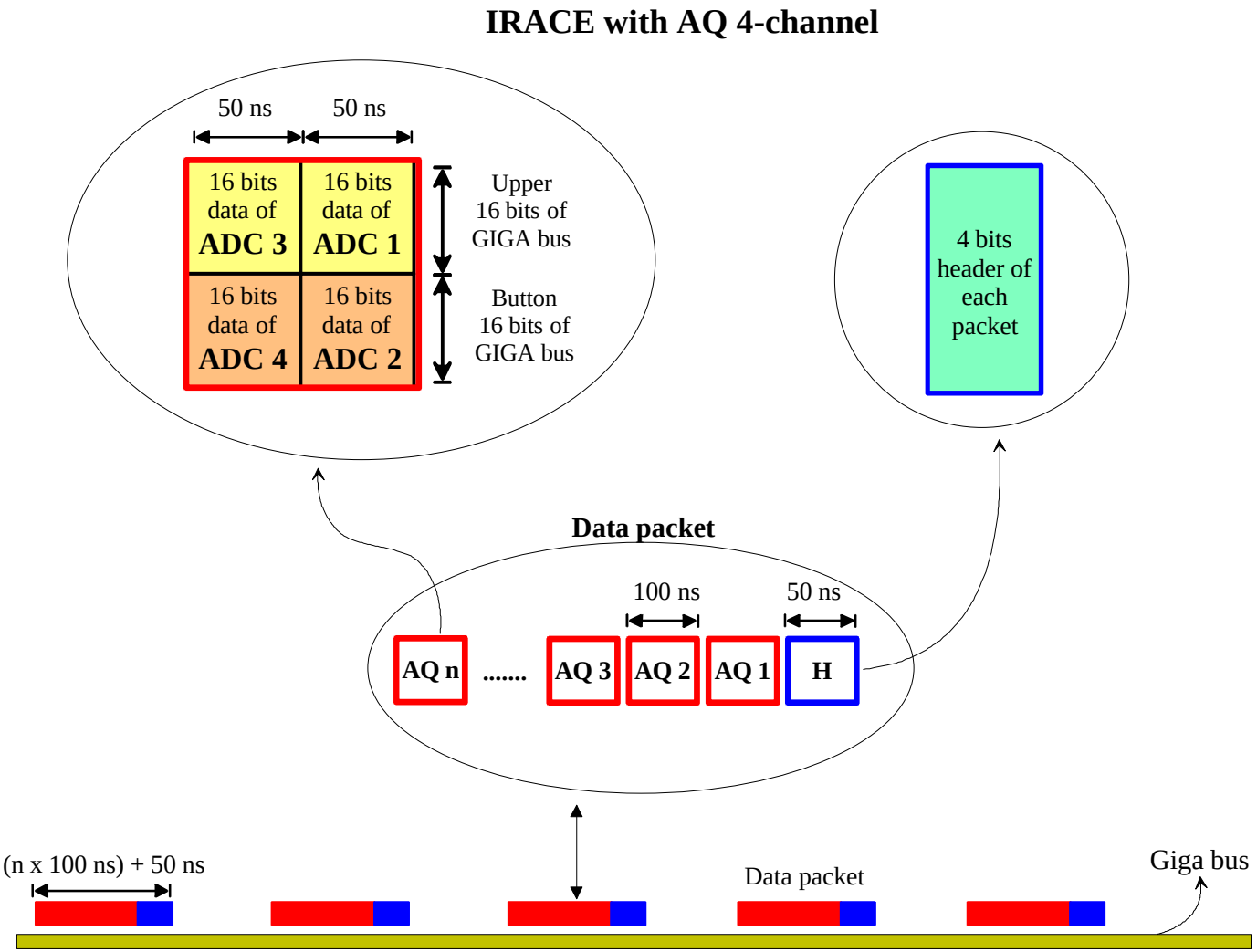

IR Array Detector
Clock
Bias
Video channels
AQ
four channel
or
sixteen ch.
AQ
four channel
or
sixteen ch.
Giga
fiberoptic
1 giga bit /s
port if.
CLDC
16 an. clock
16 bias vol.
Sequencer
48 digital
clock's
Front-end electronic
8 or 32 channel system
Fiber optic
up to 2 km
Giga
fiberoptic
1 giga bit /s
port if.
Data If
VME interf.
EDT DMA if
DMA Interface
Data link
Parallel /Seriel port
Command link
Back-end electronic
Ultra Sparc work station

GIGA

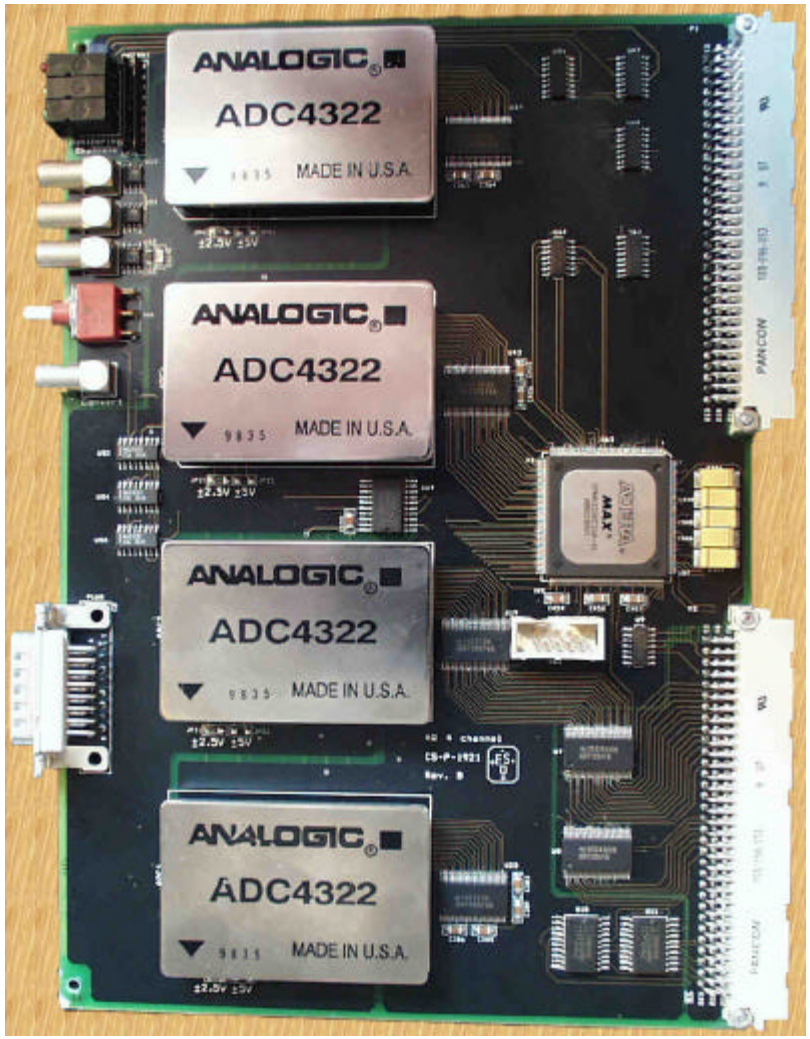


- Fiber optic transceiver data rate of 1 Gigabit/s
- 80 MB/s data bus on P2 connector
- Parallel and serial port interface
- VME bus compatible

Transport of data over the giga bus

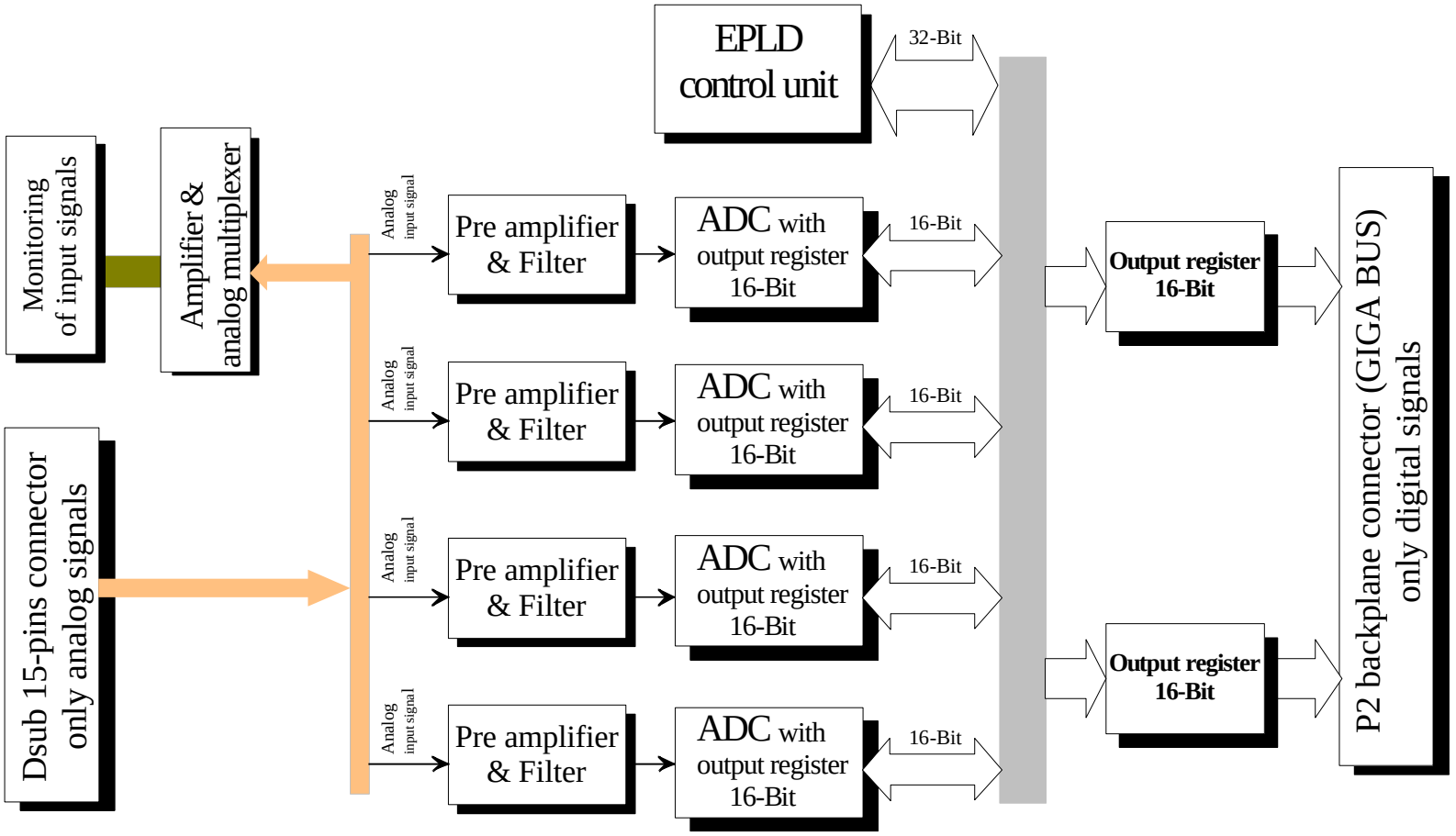


AQ 4-channel

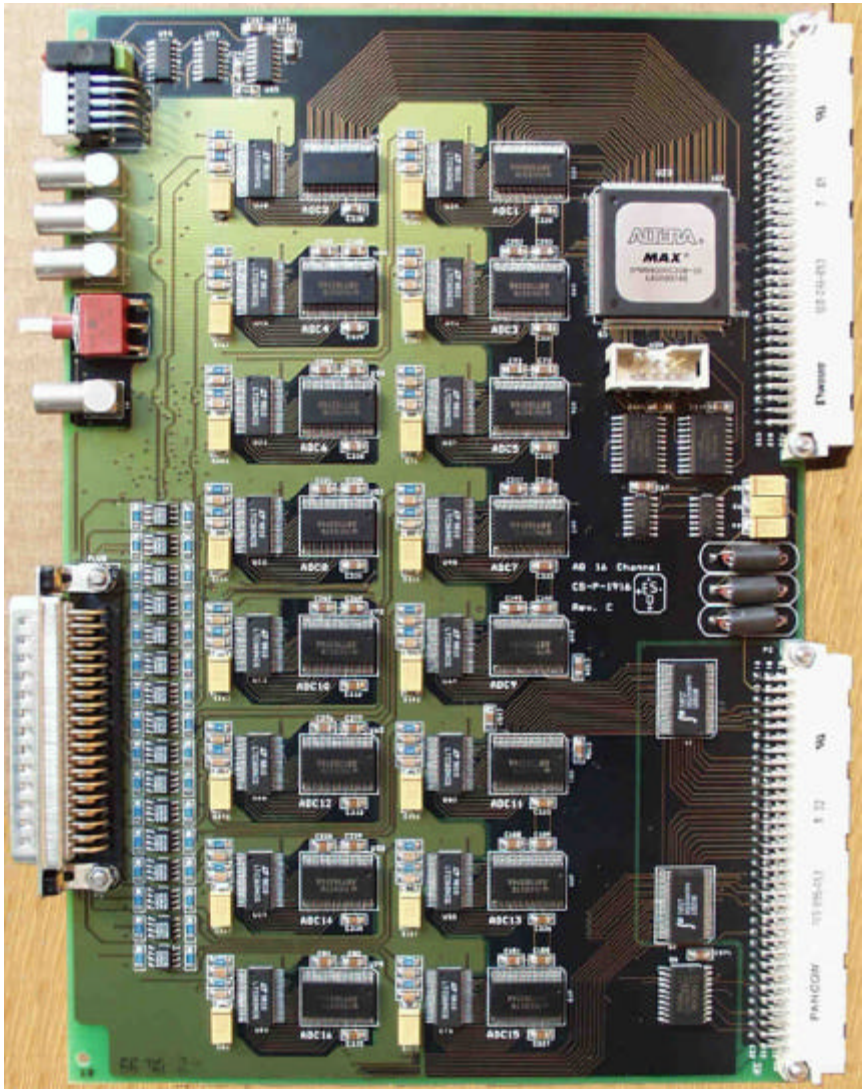


- 4 fast ADC's
  ADC 4322: 16 bit 2MHz
- 8 boards = 32 channel system
  1Kx1K array: frame rate 16 Hz
- True differential analog inputs
- VME compatible I/O pin
- Monitoring of video input signals
- 80 MB/s data bus on P2
- Delay of conversion strobe
  in 50 ns steps
- On board ADC-emulator

AQ 4-channel

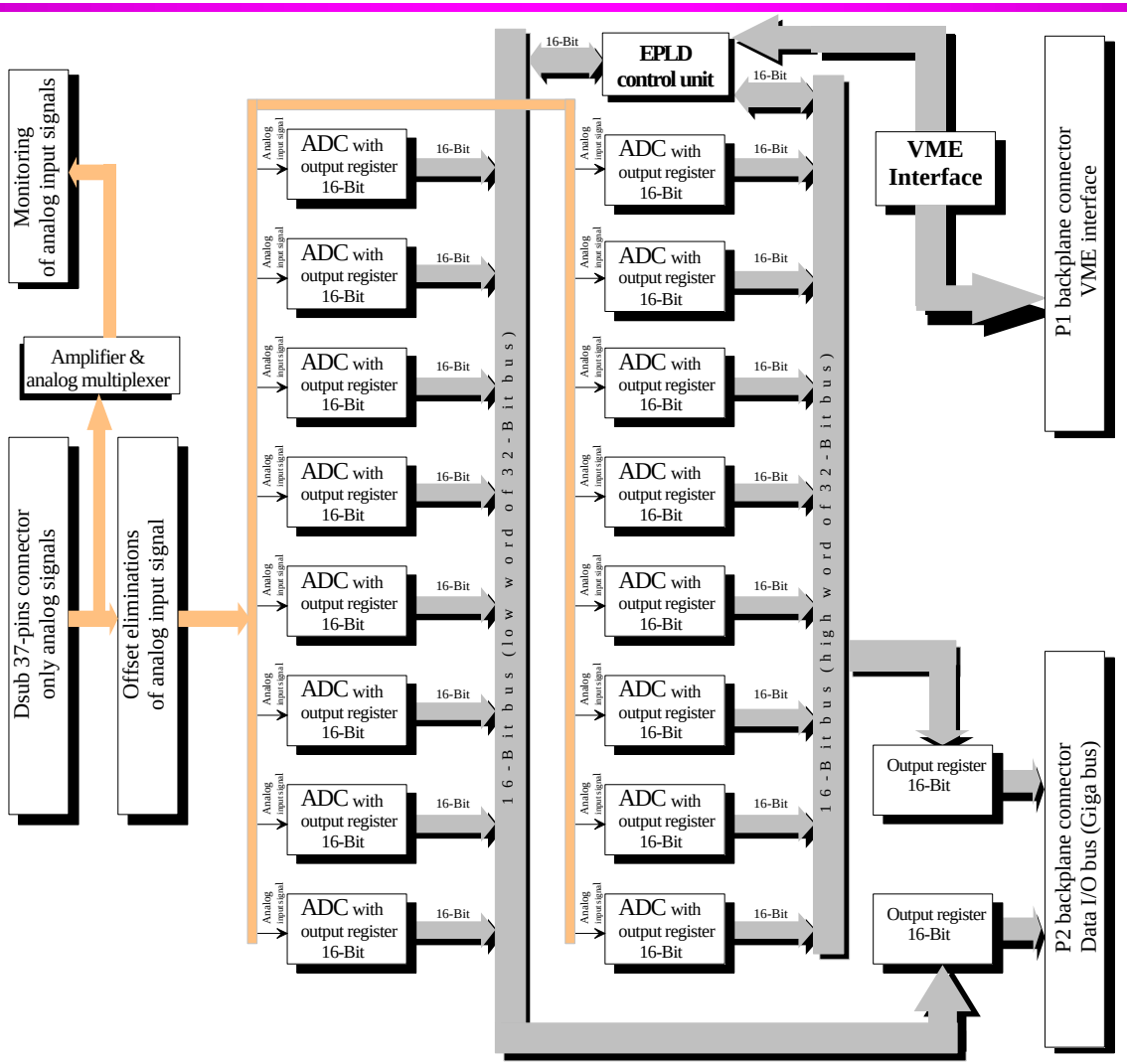

EPLD
control unit
32-Bit
Monitoring
of input signals
Amplifier &
analog multiplexer
Dsub 15-pins connector
only analog signals
Analog
input signal
Pre amplifier
& Filter
ADC with
output register
16-Bit
16-Bit
Output register
16-Bit
P2 backplane connector (GIGA BUS)
only digital signals

AQ 16-channel

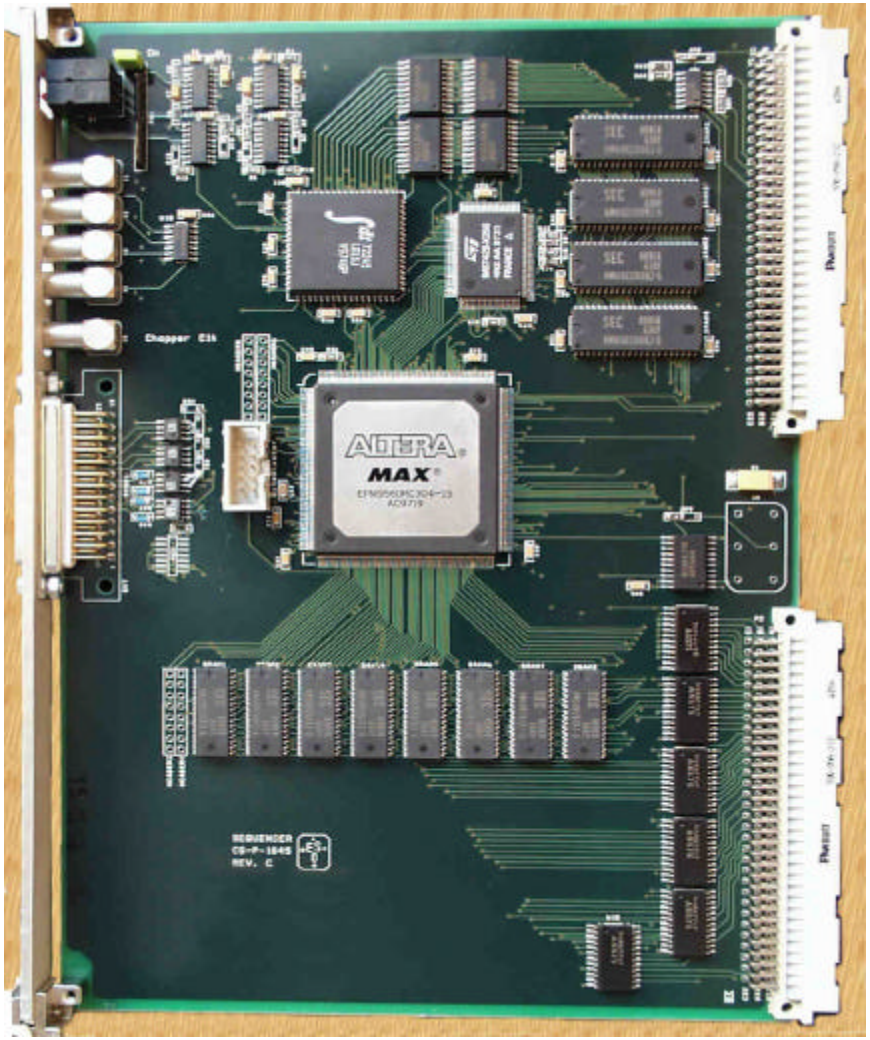


- 16 ADC's
  LTC1608 16 bit 500 KHz
- 9 boards = 144 channel system for 4Kx4K array: frame rate 1.25 Hz
- True differential analog inputs
- True VME bus interface
- Monitoring of video input signals
- 80 MB/s data bus on P2
- Delay of conversion strobe in 50 ns steps
- On board ADC-emulator

AQ 16-channel

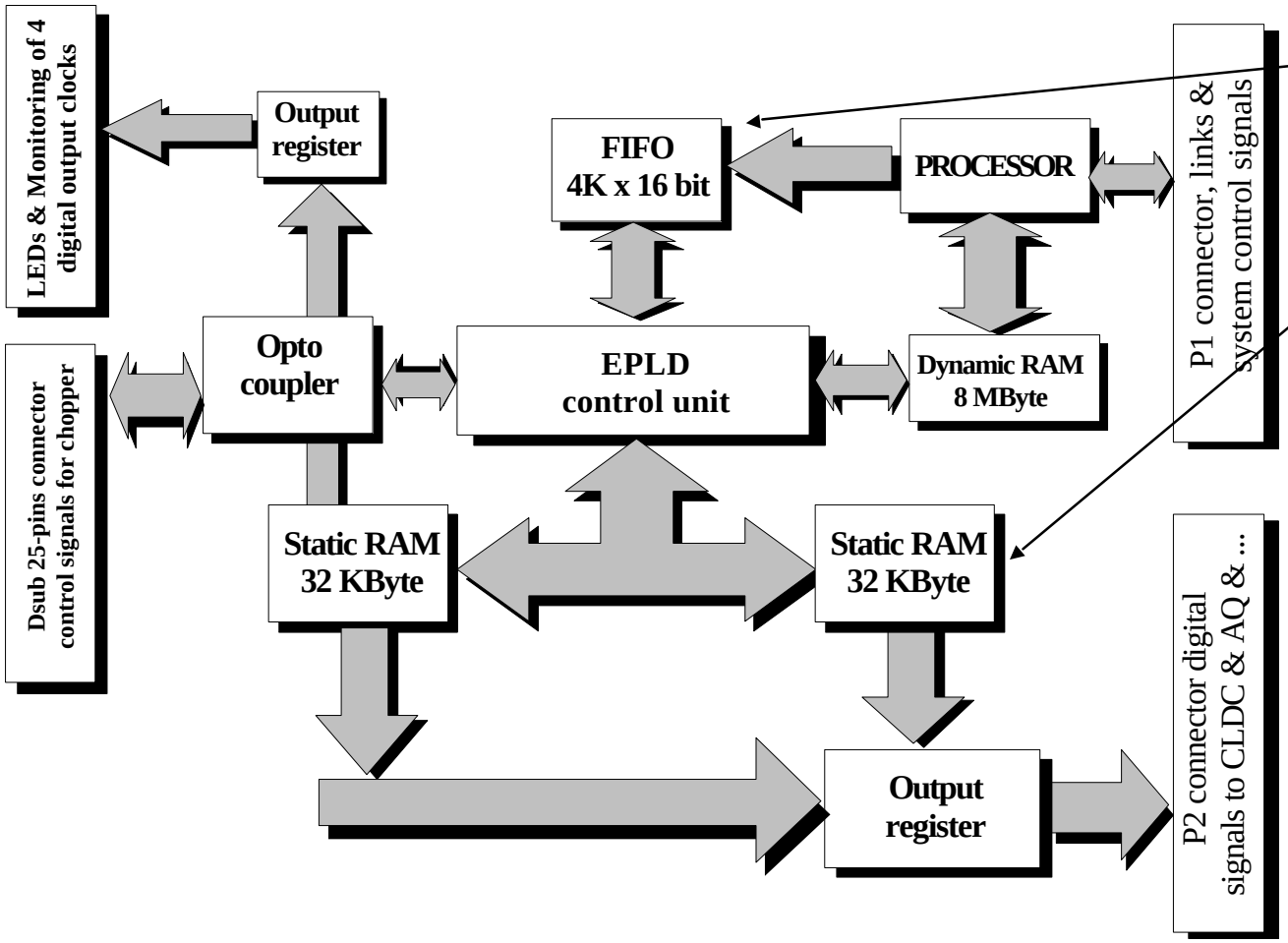


Sequencer



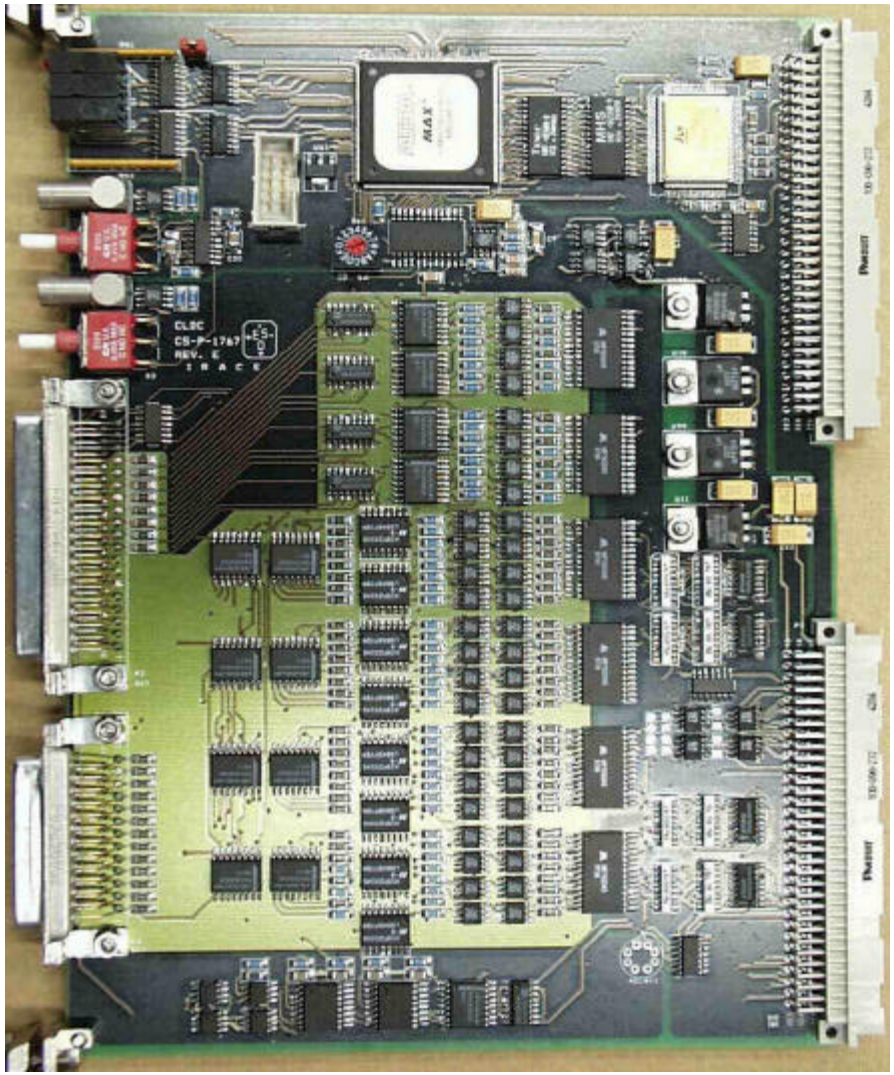
- 48 digital clocks
- Min. pulse width of 50 ns
- Flexible mapping of clocks on output pins
- On board monitor for all clocks
- Control input signal for external synchronization
- 8 MB DRAM

Sequencer



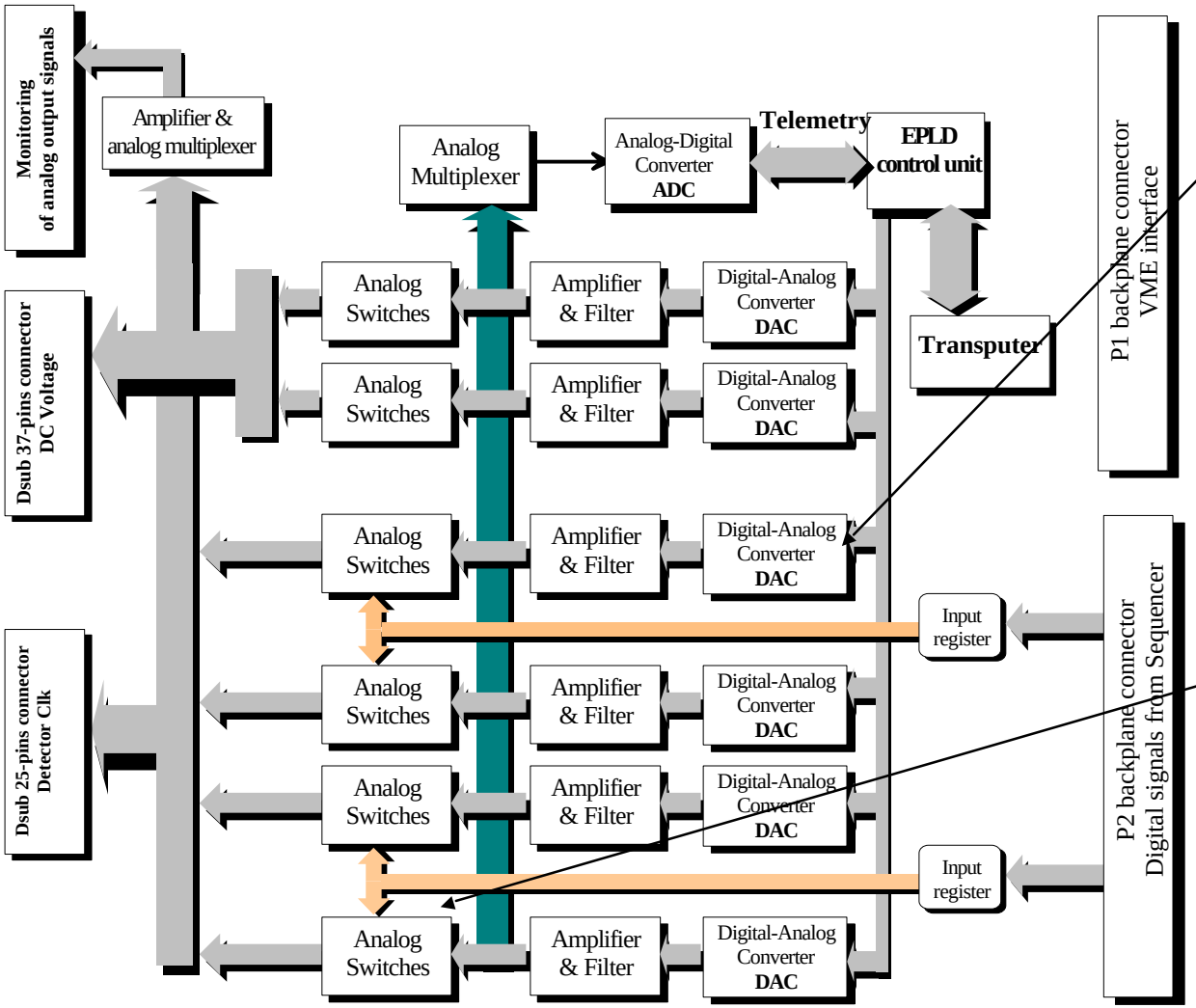
- Order of subpatterns
- low level subpattern

CLDC



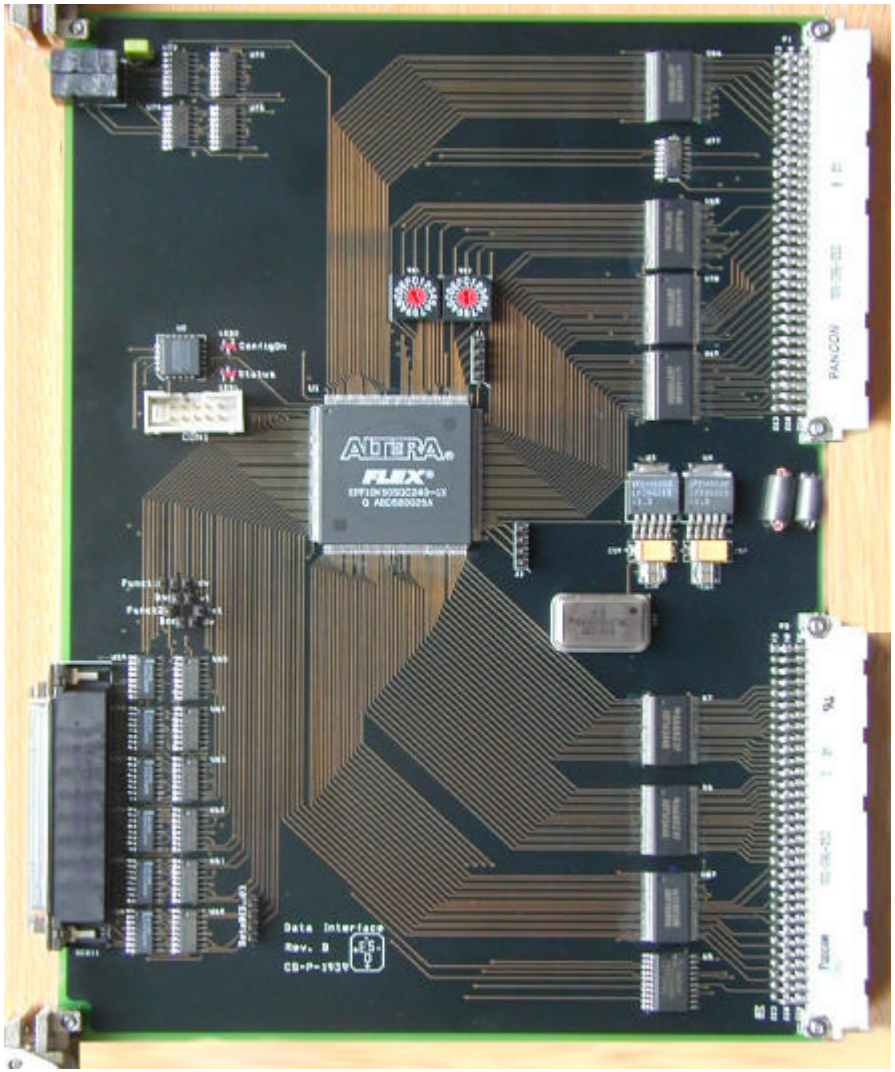
- 16 low noise analog clocks
- 16 low noise bias voltages
- Telemetry of clock and bias voltages
- Monitoring of analog clocks
- Integrated temperature measurement of detector

CLDC



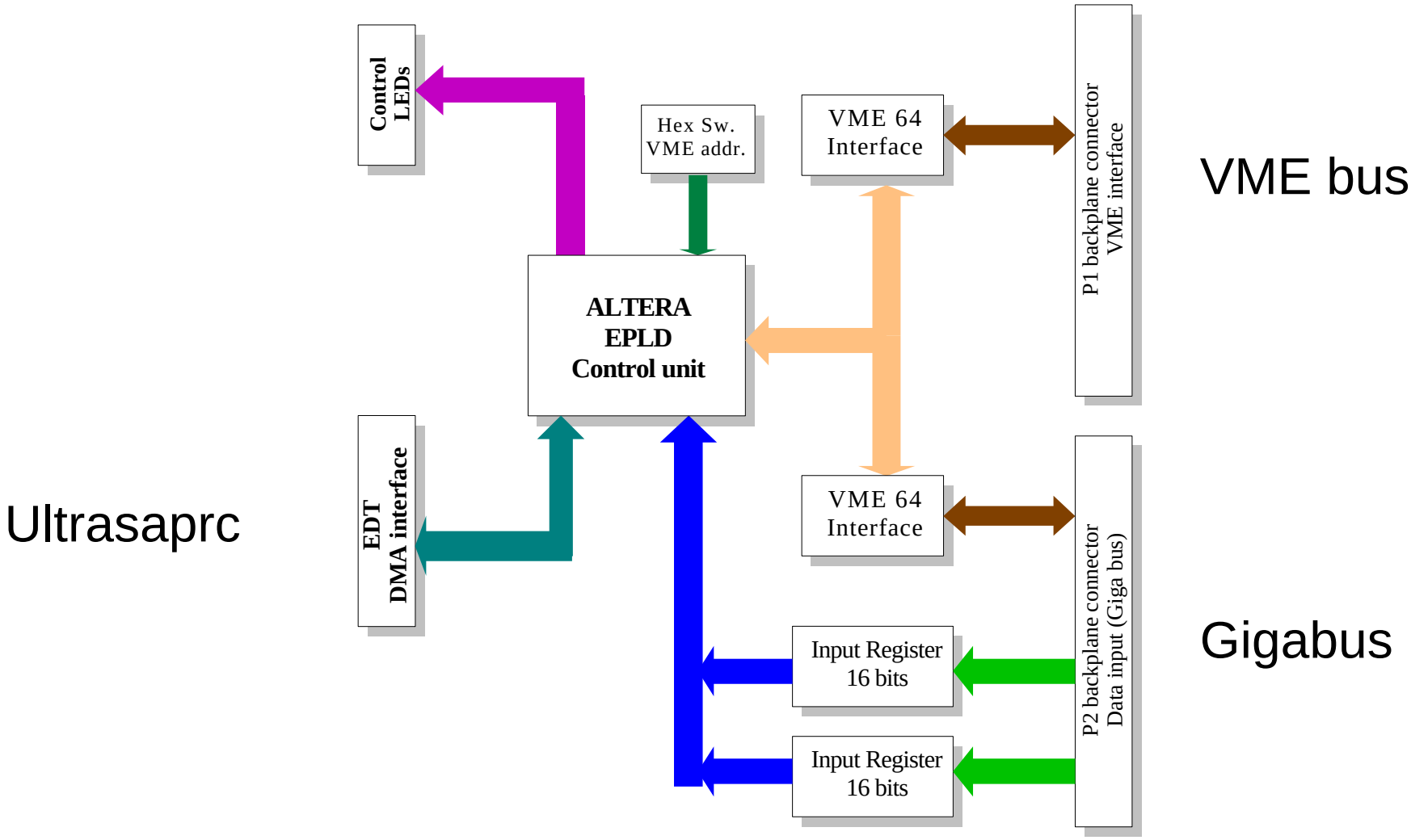
- Programmable bias and clock voltages
- change of voltage settings possible during reading out of detector
- Analog switch Harris HI-201HS

Date interface

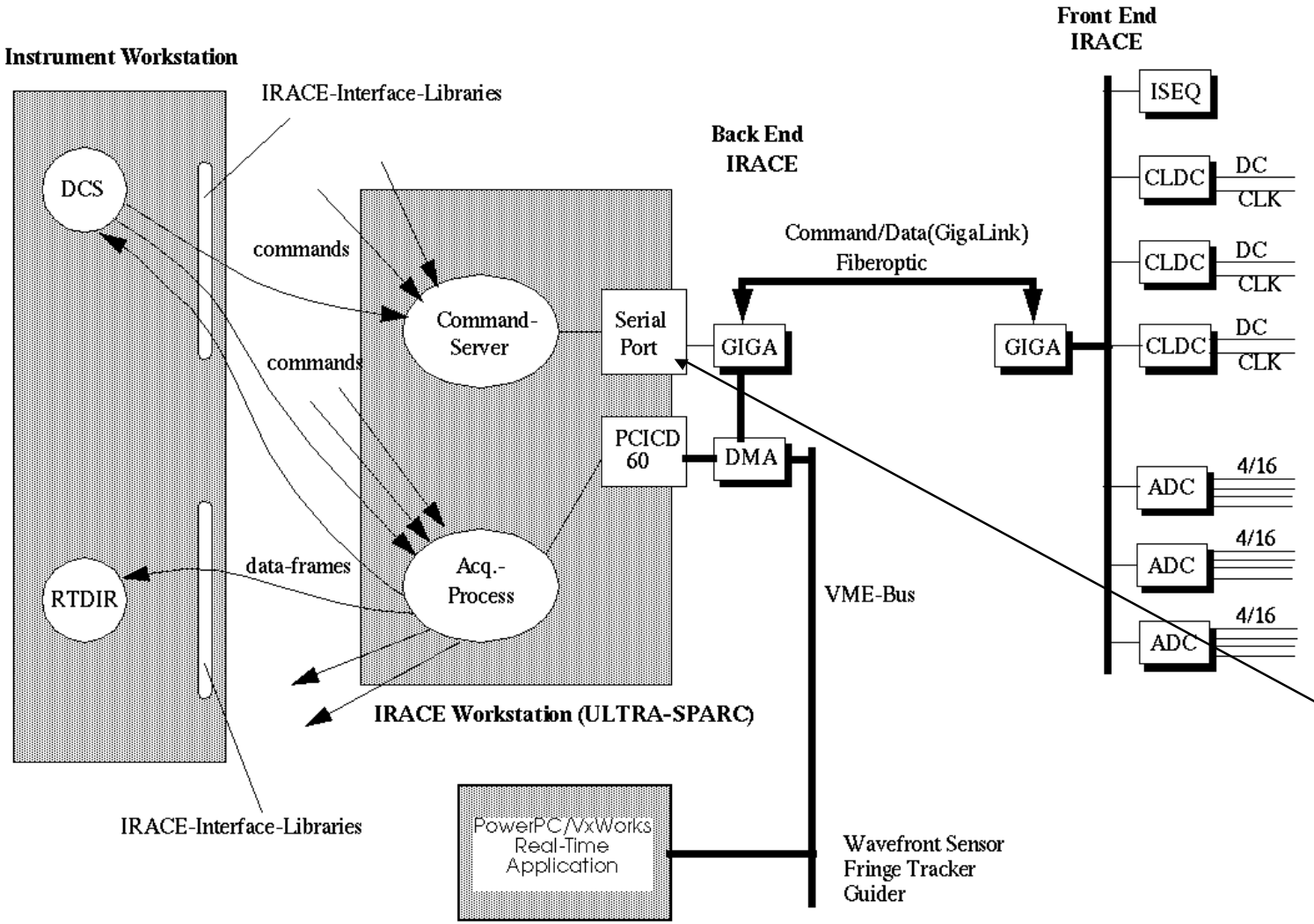


- EDT SCD 60 interface with a transfer rate of 60 MB/s
- VME 64 bit interface
- minimum DIT
  with semaphore: 150 µs
  (power PC on VME)
  without semaphore: 3 µs
- VME interrupt and board ID are programmable by software

Date interface

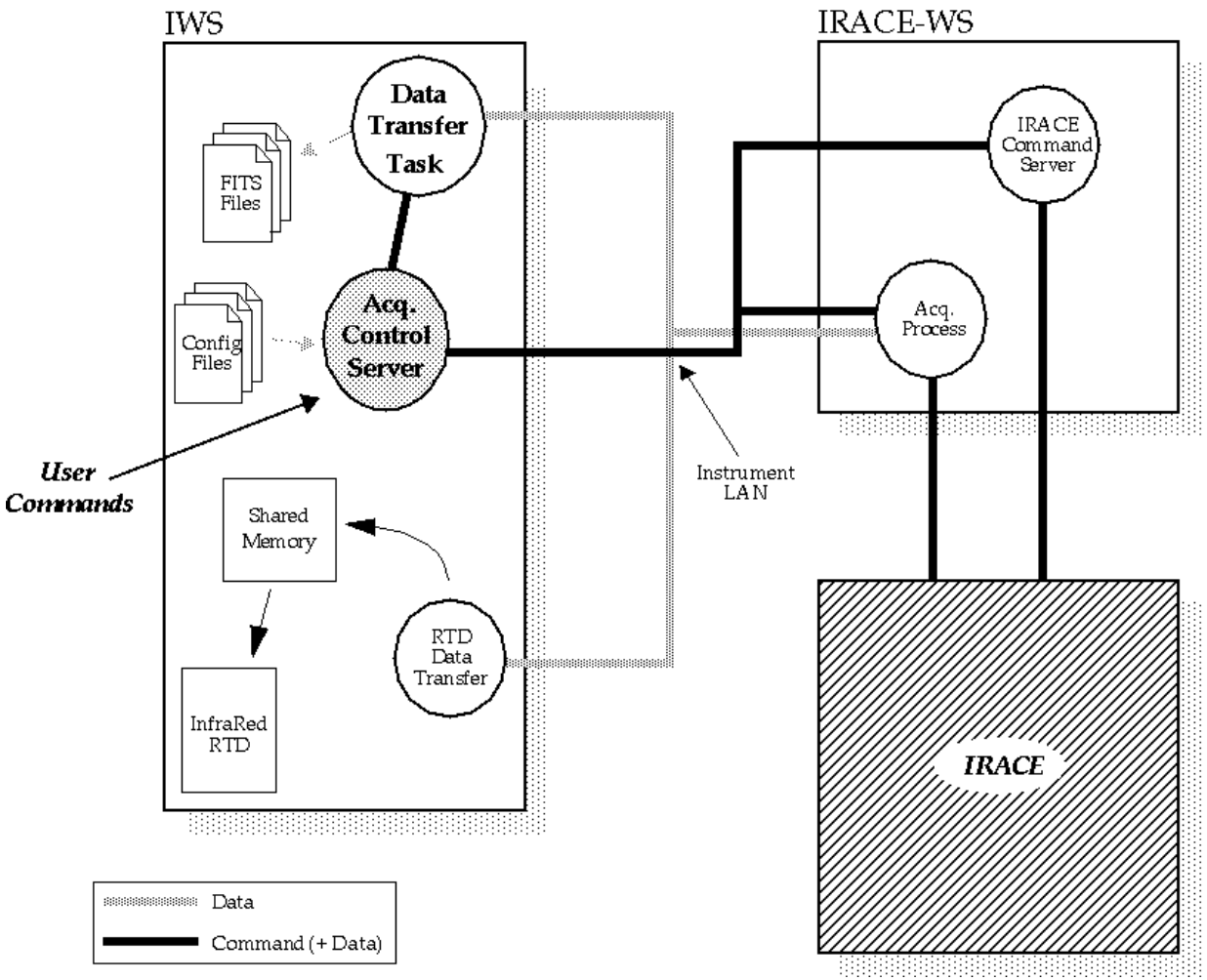


Detector Control Software DCS for IRACE front end



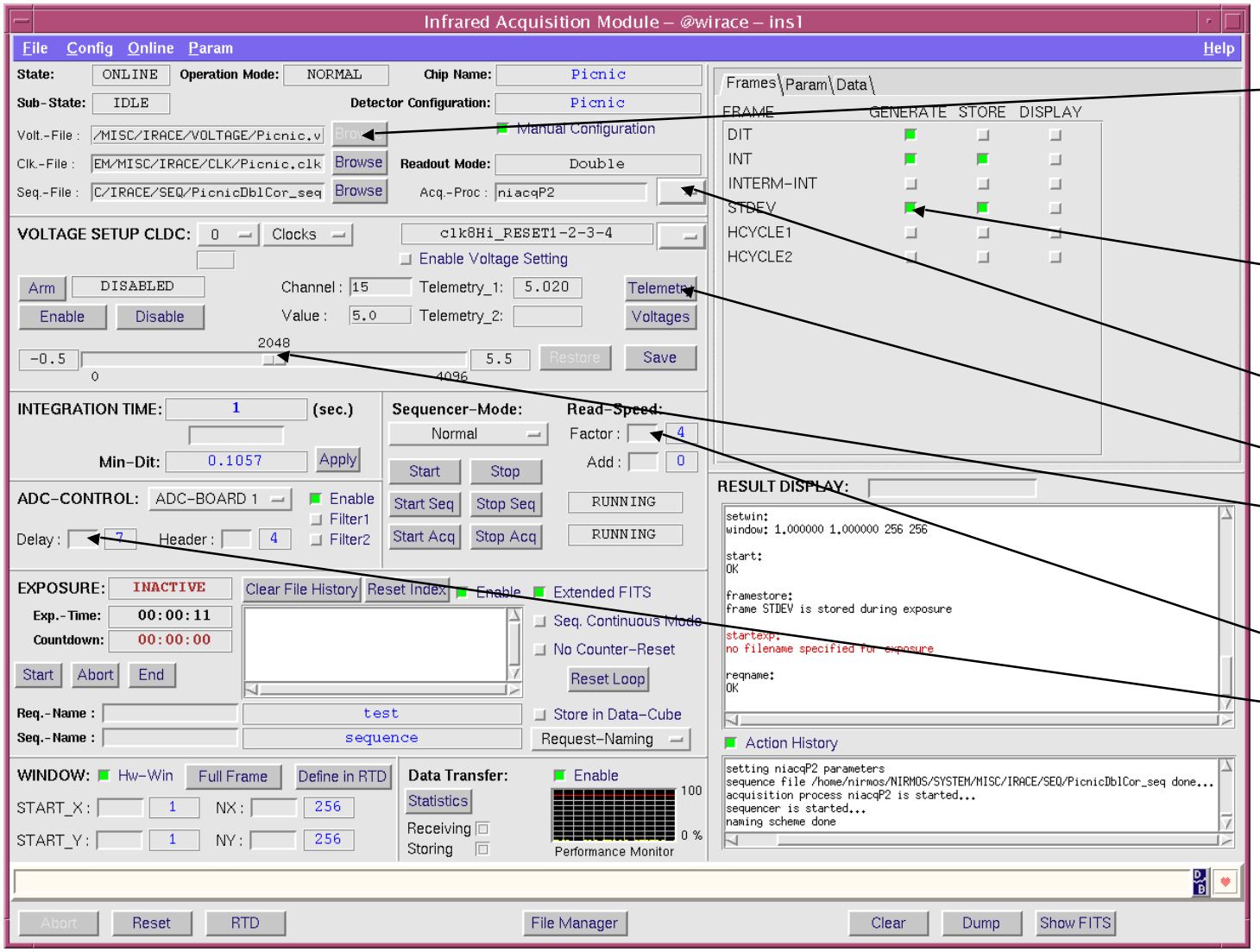
- Programmable Sequencer
- resolution 50 ns
- Tcl-based sequencer language
- TTL input for external synchronization
- progammable conversion strobe delay
- Interfaces:
  Serial RS232
  Parallel BPP
- Front end simulator

Detector control software DCS for Acquisition Process & server



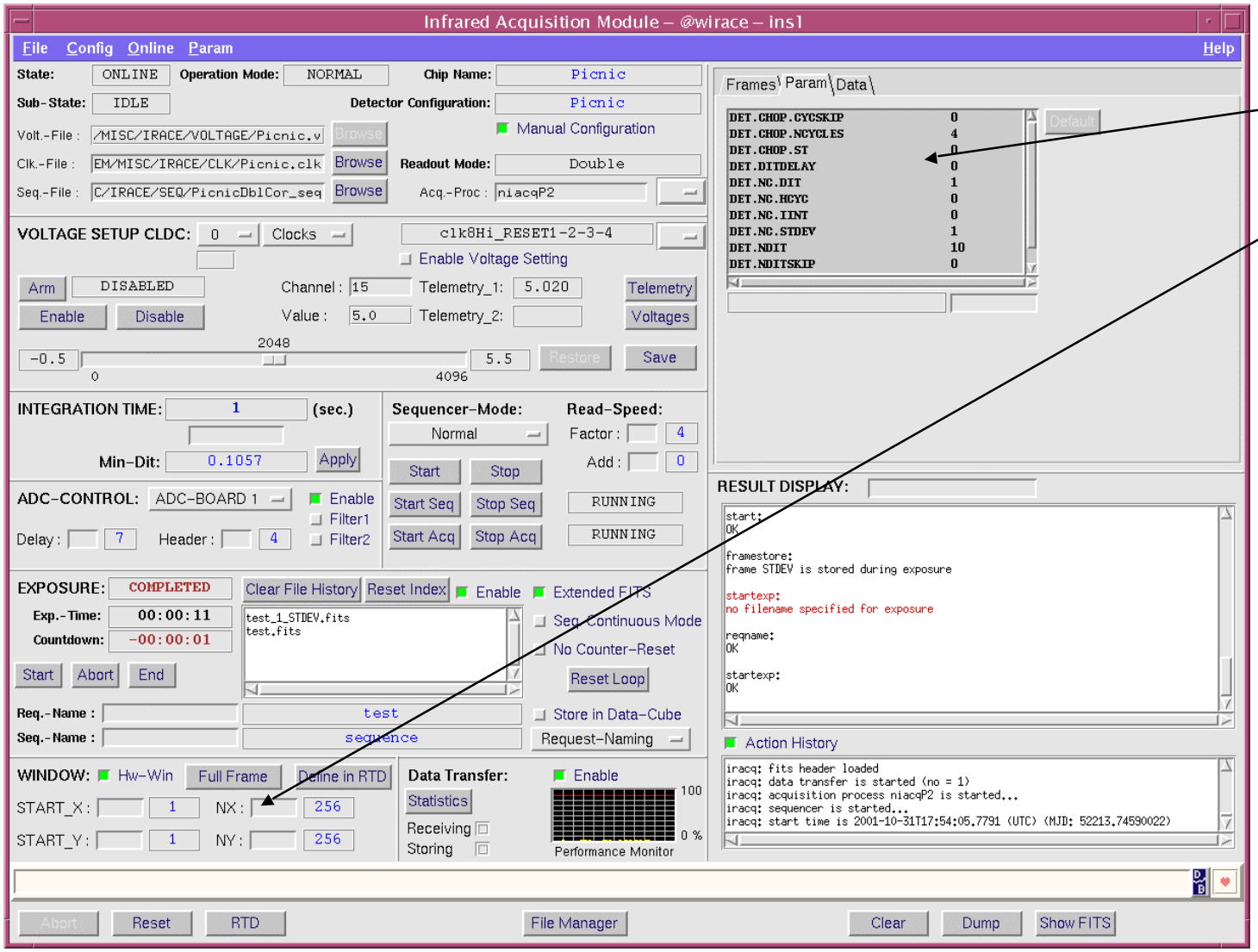
- Acquisition Process
  - » Modular Architecture
  - » Parallel frame transfer to n clients
  - » up to 60 MB/s continuous data reduction flow
  - » built-in burst mode
  - » built in simulation mode
  - » Solaris real time threads with priority control
  - » VME bus interface: VxWorks driver for control loops
- DSC Control server
  - » Control Server and Data Transfer task support hooks
  - » Image postprocessing in data transfer task (flip, rotate)
  - » Engineering GUI with on line help
  - » supported: HP-UX, Solaris, Linux

IRACE DCS Engineering Gui



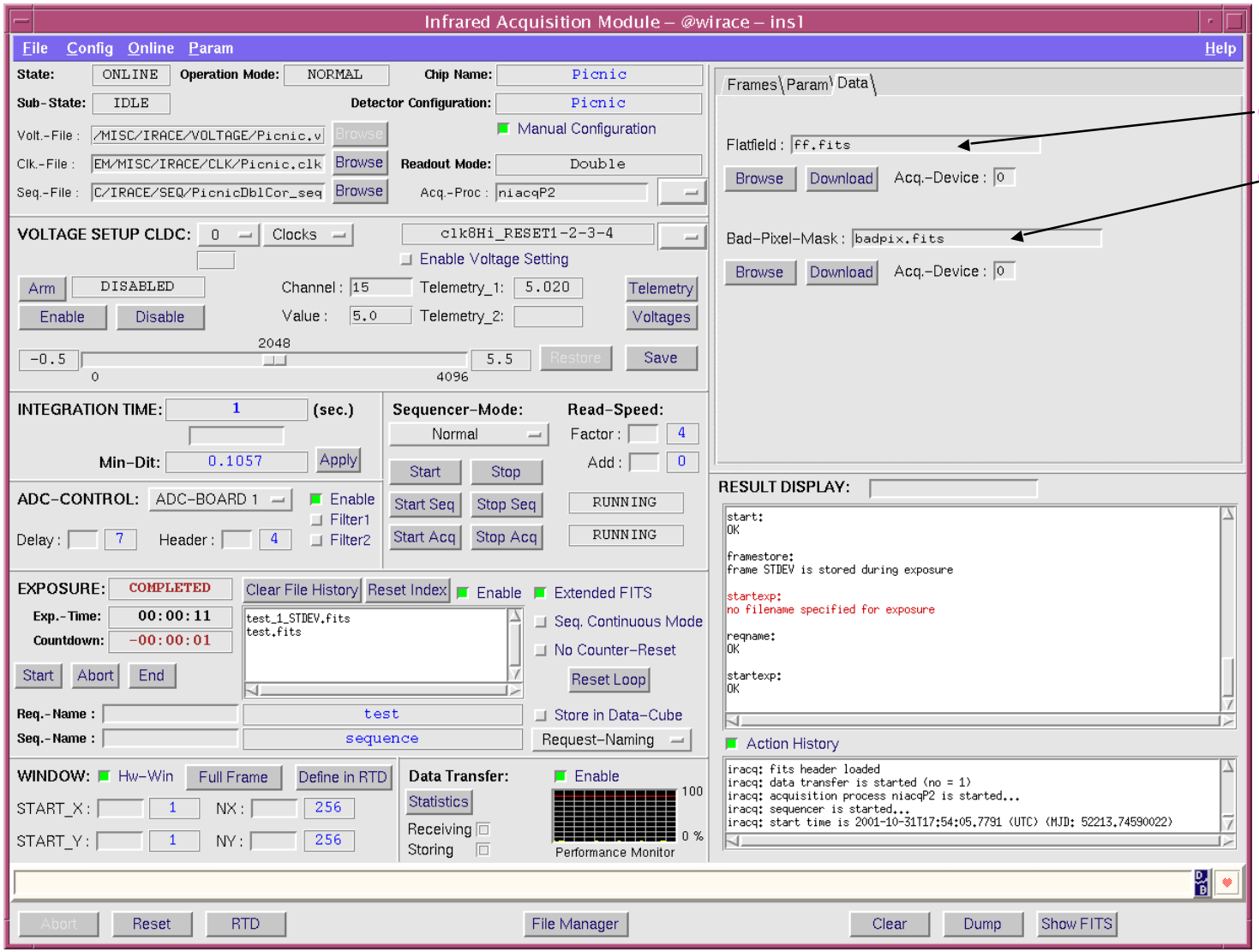
- Voltage file
  clock file
  sequencer file
- standard deviation
  intermediate INT
- readout mode
- telemetry
- slide ruler for voltage setting
- read speed
- ADC conversion strobe delay

IRACE DCS Engineering Gui



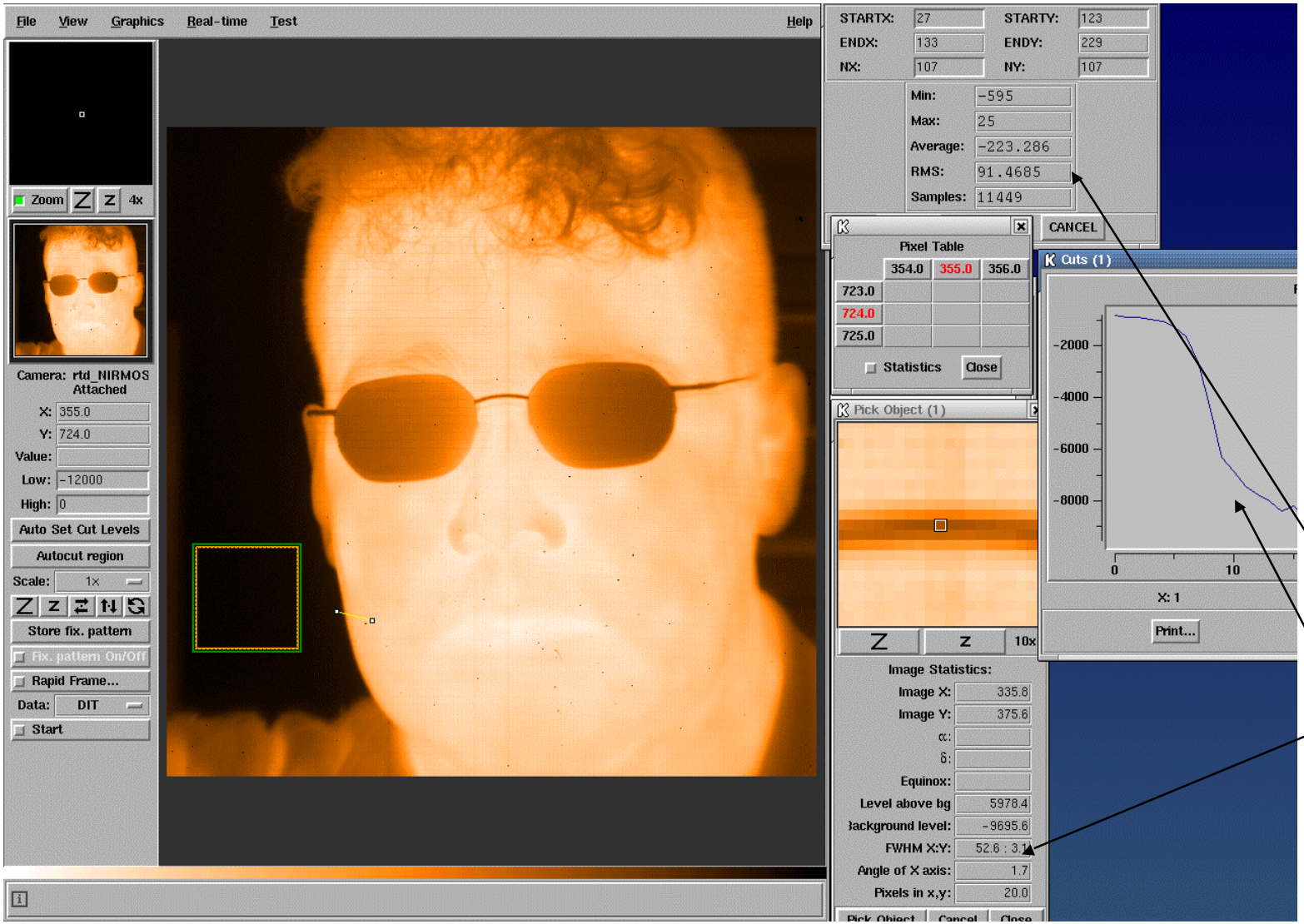
- Exposure parameters chopping
- window parameters for hardware window

IRACE DCS Engineering Gui



- Flat field
- bad pixel mask

Real Time Display



- M band 4.6-4.8 µm
- 640x640 window of 1024^2 InSb array
- Integration time 27 msec

In Real Time:

- fixed pattern subtraction
- statistics inside subframe
- trace
- FWHM & centroid
- intermediate image

Conclusion

- IRACE is modular
  flexible
  scaleable to adapt to all detector needs
- IRACE has low noise: 3 erms with Hawaii1
  by combining non-destructive and subpixel sampling
- IRACE is fast
  0.77 frame/sec with 4Kx4K Hawaii2 (144 outputs)
  16 frames/sec with 1Kx1K InSb (32 outputs)
  6600 frames/sec for real time applications
  (power PC on VME, fringe tracker, wavefront sensor,…)
- IRACE comes with integrated detector control software and real time display offering a wide variety of readout modes