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Upgrading the ALMA Digital System, from Digitization to Correlation

Final Report

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1 Introduction and objectives summary of the development study

As noted in the ALMA development report [1] released in mid-2018, "ALMA is approaching completion of its initially envisaged capabilities and, within the first five years of operations, the original fundamental science goals of ALMA have been essentially achieved." Nevertheless, the current ALMA Digital Signal Processing is limited to 8 GHz of bandwidth per polarization, covering only a small fraction of each atmospheric window available from Chajnantor. Therefore, with the current system, unbiased redshift searches, line identifications, and astrochemical surveys require multiple tunings or spectral setups, presenting one of the main limitations for ALMA science. A working group has been established by the ALMA board to develop a strategic vision and define new capabilities for the Observatory out to 2030 as part of the ALMA Development Program. This group concluded that, based on scientific merit and technical feasibility, and to bring significant gains in the observing speed in particular, the priorities must be:

- to broaden the receiver IF bandwidth (by *at least* a factor of two), and
- to upgrade the associated electronics and correlator (improving both the instantaneous bandwidth and spectral resolution).

The second item above is strongly related to the historical contributions from Laboratoire d'astrophyique de Bordeaux (LAB) during the ALMA construction phase, since our electronics group delivered the digitizer module, part of the backend electronics, and the digital Tunable Filter Bank, which is part of the correlator. LAB has always been heavily concerned with ALMA: scientists contribute to the ALMA Regional Center activities through software development or in kind effort (see [2], [3], and [4] for reference), the electronics group is involved in corrective maintenance services for ESO, and this same groups has successfully answered the ESO calls for development study proposals in 2013 and 2016. The main objective of our first study in 2013 was to evaluate technologies which could be used in a mid-term timeframe to upgrade the sub-systems we originally delivered (see [5]). Our second study was focused on the identification and the evaluation of the critical devices required to enhance digitization (DG), data transmission (DTX-DRX), and digital signal processing (TFB), in accordance with the general ALMA roadmap, the definition of which has meanwhile progressed (see [6]). This second study also includes system architecture considerations and comparisons, from digitization to correlation. Today we believe that we have identified technological solutions that meet the top level requirements of the digital system that, as was recommended in [1], are set in anticipation of future growth.

During our new one-year study we aimed to:

- confirm the technological solutions,
- design detailed block diagram, mathematical model, and HDL description,
- address many of the system, calibration, and interface issues,

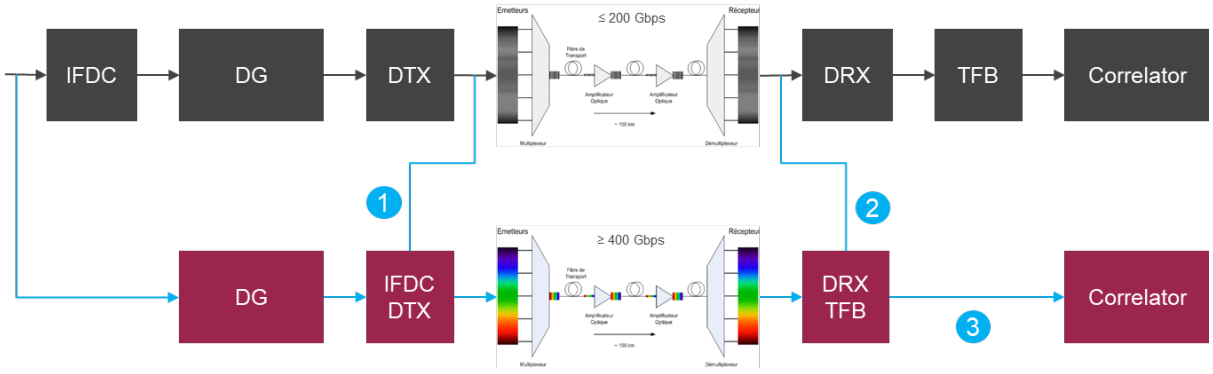
- produce cost estimations for prototyping and production,
- prepare a plan for on-site demonstration and upgrade at relatively short term.

In this final report, we provide a brief description of the proposed upgrade in Section 2, we present our solution for the digitization based on the Micram device, including a discussion on the digitizer requirements and the digitization efficiency, in Section 3.1, we describe our preliminary work to design a new digitizer clock module in Section 3.2, we give an update of our plans for the data transmission in Section 4 and for the Digital Signal Processing in Section 5, we briefly discuss the question of upgrading the control/monitoring system in Section 6, we produce a rough estimate of the hardware cost for prototyping, on-site demonstration, and production, and we propose a preliminary schedule for this project in Section 7.

2 Technical description of the proposed upgrade

The top priority for increasing the science capability of ALMA is to improve the survey speed by expanding the instantaneous bandwidth and enhancing the spectral resolution. The exact specifications of the next generation receivers are not yet finalized, but as explained in [1], “Any receiver upgrade that increases the IF bandwidth must be accompanied by an upgraded signal transport chain to digitize the receiver output and transfer the data to the correlator, and an upgraded correlator to process the increased bandwidth”. This is why LAB, supported by ESO, carried out development studies in each of the 2013, 2016, and 2019 proposal cycles. The latest study is ongoing, and is the subject of this final report. All these studies aim at upgrading the ALMA digital system from digitization to correlation.

Our current plan for this upgrade is described by the global block diagram in **Figure 1**, with on-site demonstration in 3 potential steps to ensure compatibility with the existing infrastructure (physical locations, power supplies, reference signals, M&C interfaces and optical fibers) before a full production and integration. The recommended strategy is to deploy the new ALMA 2030 digital system in parallel with existing hardware, with all new components deployed to different physical locations, so that the current system can continue science operations until the new system is commissioned. The bulk of commissioning could then be accomplished during periods of unfavorable / less favorable observing conditions (i.e. daytime), while science operations continue with the current system during optimal conditions.



Step	Quantization	Efficiency	Bandwidth	Spectral coverage
#1	3 bits x 2 bits	0.84	2 x 4 GHz / pol	128 x 62.5 MHz / pol
#2	6 bits x 2 bits	0.88	2 x 16 GHz / pol	128 x 62.5 MHz / pol
#3	6 bits x 6 bits	0.99	2 x 16 GHz / pol	256 x 125 MHz / pol

Figure 1: ALMA signal flow (in black: current system, in color: new system)

3 Digitization

Digitization is one of the main technological challenges for increasing the ALMA instantaneous bandwidth because the market of analog to digital converters with analog bandwidths and sampling frequencies above 10 GHz is a niche market, extremely limited and unsteady. For the past ten years, the electronics group from LAB has investigated fully in-house custom ASIC designs (CMOS or BiCMOS technologies, see [7]), has evaluated several devices from small micro-electronics startup or worldwide electronics companies (see [8] and [9], and has considered various digitization topologies (e.g. multi-rate, interleaved, see [10]).

Our objective has always been to design a digital back-end including the digitizer and the DTX functions which would be able to digitize the full IF bandwidth delivered by the receivers, process and format the digital samples for transmission over the optical fiber. Removing most of the analog parts (currently used for the second frequency conversion prior to digitization), we would enhance back-end versatility, reproducibility, and reliability, as well as ease calibration and failure analysis.

Today, **our baseline solution for digitization is an ADC from the Micram Company**. This commercial device was initially given a specification of 34 GSps, but has been extensively evaluated by our group up to 40 GSps (see [11] for details), and then subsequently by Micram. This digitizer chip is built on two internally interleaved ADC cores using flash folding and interpolating architecture. This complex calibration is required to optimize the linearity of each core and minimize the mismatch between cores. With this solution we can achieve direct digitization of e.g. [2 – 19.5] GHz IF (see discussion about the IF spectral position in Section 5.3) at 40 GSps, ten times better than the current digitizer does, and we will also significantly increase the quantization efficiency since the Micram device is a 6-bit ADC (versus 3 bit for the current digitizer).

The new Digitizer Assembly (DG in Figure 1) will be mounted near the Front-End Assembly (inside or bolted to the Front-End Electronics Chassis). It will be composed of (see Figure 2):

- RF signal conditioning modules (one per sideband), with custom band-pass filters, wide band amplifiers, digital step attenuators, and custom gain equalizers.
- 2-polarization digitizer modules (one per sideband), with two 6-bit ADCs from Micram.
- DGCK module generating 20 GHz clock signals from a 125 MHz reference (one clock signal per ADC).

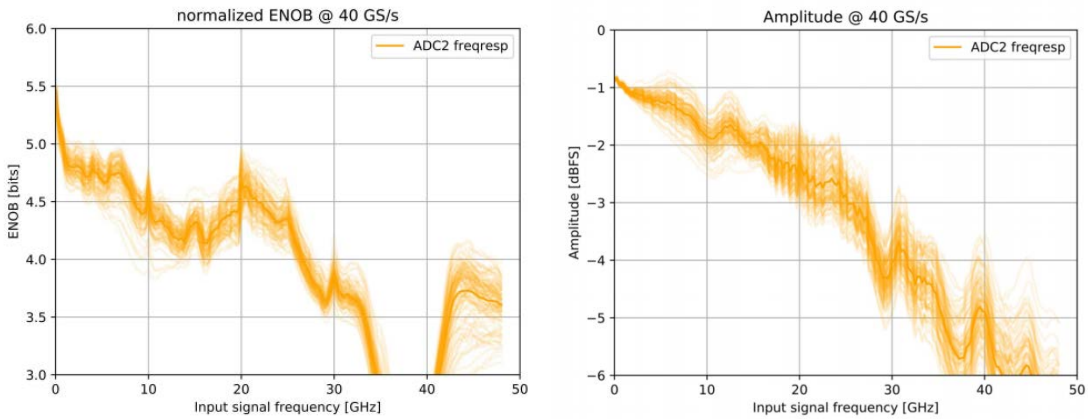


Figure 2: ENOB and bandwidth of the Micram ADC

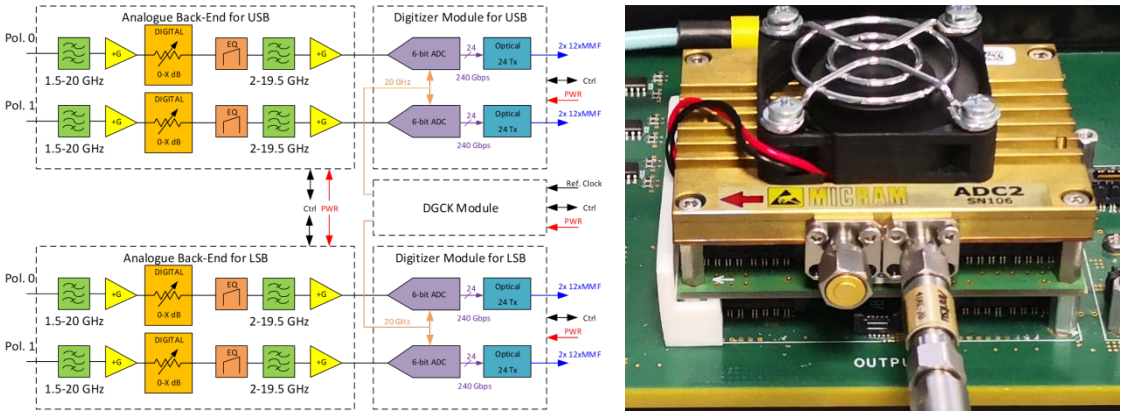


Figure 3: Digitizer assembly based on Micram 6-bit ADC module at 40 GSps

Sampled data are transmitted to the DTX (located in the digital backend rack) through optical data links (FireFly optical module from SAMTEC). Each module will embed a microcontroller placed inside an RF shielding to communicate with the DTX through 10/100 Mb Ethernet optical links. Optical data links are preferred because it offers the best compromise between RF performance and EMI suppression, ensuring a galvanic isolation between the DG and the DTX.

3.1 Digitizer requirements discussion

In the next paragraphs are given a number of recommendations from the ALMA FE & Digitizer Technical Requirements Working Group that we use as a starting point for a detailed discussion on the digitizer requirements and performance measurements.

- **Digitizer Sampling Speed ≥ 40 GHz**
  From [12]: ""Assuming that the Nyquist frequency is equal to an upper limit of 20 GHz, e.g. for an IF Band of 4 to 20 GHz, the sampling frequency equals 40 GHz. It might be that a single digitizer core cannot achieve the required performance in terms of Effective Number of Bits (ENOB) at the specified digitizer sampling speed. As an alternative to a single core digitizer, interleaved or dual-rate digitizer architectures can be considered as long as they achieve the applicable requirements as provided in this document. A second down-conversion stage is not favored due to the increased complexity, costs and practical issue with internally generated spurious signals due to additional, secondary, local oscillators."

- **Effective Number of Bits (ENOB) ≥ 5**
  From [12]: "The ENOB to be achieved for the digitizer is a major technological challenge recognizing the strong desire to increase the quantization efficiency to at least 99% for standard, excluding solar and calibration, astronomical observations from the current 96 %. The digitizer performance matching our astronomical requirements, including continuous sampling with very low spurious levels, is a niche market for commercial devices. Taking into account the ongoing evaluation of COTS devices and market forecasts we have come to the following, conservative requirement: ENOB ≥ 5

- **Passband Gain Variations < 5.4dB**
  From [12]: "These Passband Gain Variations are directly coupled with the requirements for quantization efficiency of the digitizer and the Effective Number of Bits (ENOB). Since the quantization efficiency should be at least 99%, and the ENOB is set at least 5 ENOB, this leads to the following requirement: Passband Gain Variations < 5.4dB."

The requirements that drive the digitizer selection are the sampling frequency and the digitization efficiency. It is important to stress that the quantization efficiency of the current system is not equal to 96% which is the theoretical efficiency of a 3-bit ADC (from [13]). Because of imperfections and passband gain variations, the real efficiency of the current ADC is estimated to be around 92%.

From [13]: “We are here concerned with signals with Gaussian amplitude distribution that are processed by cross correlation. Quantization efficiency is the relative loss in signal-to-noise ratio resulting from the quantization process. We provide a method of calculating the quantization efficiency for any number of uniformly spaced levels, as a function of the level spacing, using formulas that are easily evaluated with commonly used mathematical programs. This enables a choice of level spacing to maximize sensitivity or to provide a compromise between the sensitivity and the voltage range of the input waveform.”

The quantization efficiency depends on the number of quantization levels and the statistical property of the input signal. Reference [13] deals with noise-like signals (Gaussian probability distribution with σ^2 as the variance/power) and shows the relation between efficiency, number of levels, and level spacing relative to sigma for a perfect ADC. Indeed, in this ideal case, the number of digital output levels is 2^N, with N being the number of physical bits generated by the ADC, and the quantization is performed with equally spaced thresholds.

The deviation from the ideal quantization step width, which necessarily exists with a real ADC, is called differential non-linearity (DNL) and is measured as number of counts (LSBs). DNL greater than 1 LSB can result in missing codes in the transfer function and consequently degrade the digitization efficiency. For DNL lower than 1, the number of levels is kept to 2^N, but the efficiency is also degraded. In that case, it has been often suggested that the digitization efficiency could be estimated from the digitizer ENOB. If it is true that the ENOB aims at defining the effective number of bits contributing to a digitization process, taking into account the imperfections of the ADC performing the digitization, it has to be considered very carefully in the ALMA case for various reasons, which we summarize below:

- The ALMA ENOB specification has been defined as a “conservative requirement.”
- The ENOB that can be found in any ADC datasheet is usually measured for strong CW input signals whereas ALMA digitizer has to process wideband signals dominated by nearly Gaussian noise.
- The ENOB will change depending on the conditions under which it is measured.

We also stress that optimizing the ENOB for CW signals does not yield to the same ADC parameter tuning as optimizing the SNR for Gaussian noise, as we have demonstrated with the Micram device; ENOB optimization is not the ultimate goal for ALMA.

Moreover, it is well known that ADC is a critical technological point for the ALMA instrument just because there are very few candidates that may have the required performance and because the niche market for ADCs is highly unpredictable. Therefore, it would be particularly unfortunate to over-constrain this subsystem or be mistaken in the evaluation and selection process. Actually, considering the ALMA ENOB specification as a strong requirement would basically lead to rejecting the Micram solution, which has “only” an ENOB of 4 bits over 20 GHz (see **Figure 2**), whereas we believe this solution could meet the real ALMA scientific needs, which were originally and rationally expressed in terms of efficiency. In the next section we describe a novel approach which consists in estimating the digitization efficiency from SNR measurements for a Gaussian noise input signal and propose to use this as a selection criterion for ALMA.

3.2 Digitizer efficiency measurement

The digitizer efficiency can be defined as the fractional loss in signal-to-noise ratio resulting from digitization:

$$eff_{DG} = \frac{signal_{analog_{pwr}}}{signal_{digital_{pwr}}} = 1 - \frac{noise_{dg_{pwr}}}{signal_{digital_{pwr}}} = 1 - 10^{-\frac{SNR_{dB}}{10}} \quad (Equation\ 1)$$

SNR_{dB} is measured from the Power Spectral Density (PSD) of the digitized signal (see **Figure 4**). Here, the analog input signal is Gaussian noise ($\sigma = 10$), shaped with a bandpass filter (2-18 GHz) and a notch filter (10-11 GHz). The notch is used to accurately measure the noise floor due to the digitization. The 50dB attenuation of the notch is expected to be sufficient to measure the noise floor level. The SNR is plotted rescaling the PSD to 0dB in the notch region. The shape of the bandpass has been compared with and without the notch filter. The notch filter has no major impact on the bandpass shape outside the notch region.

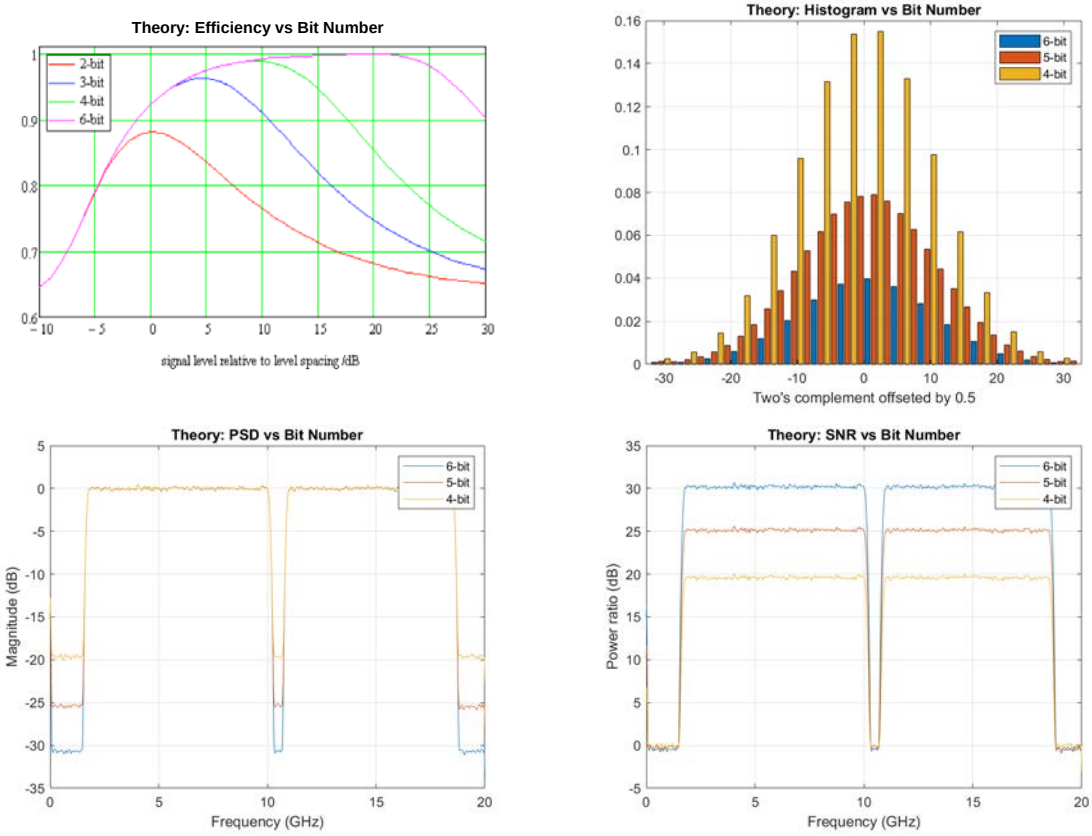
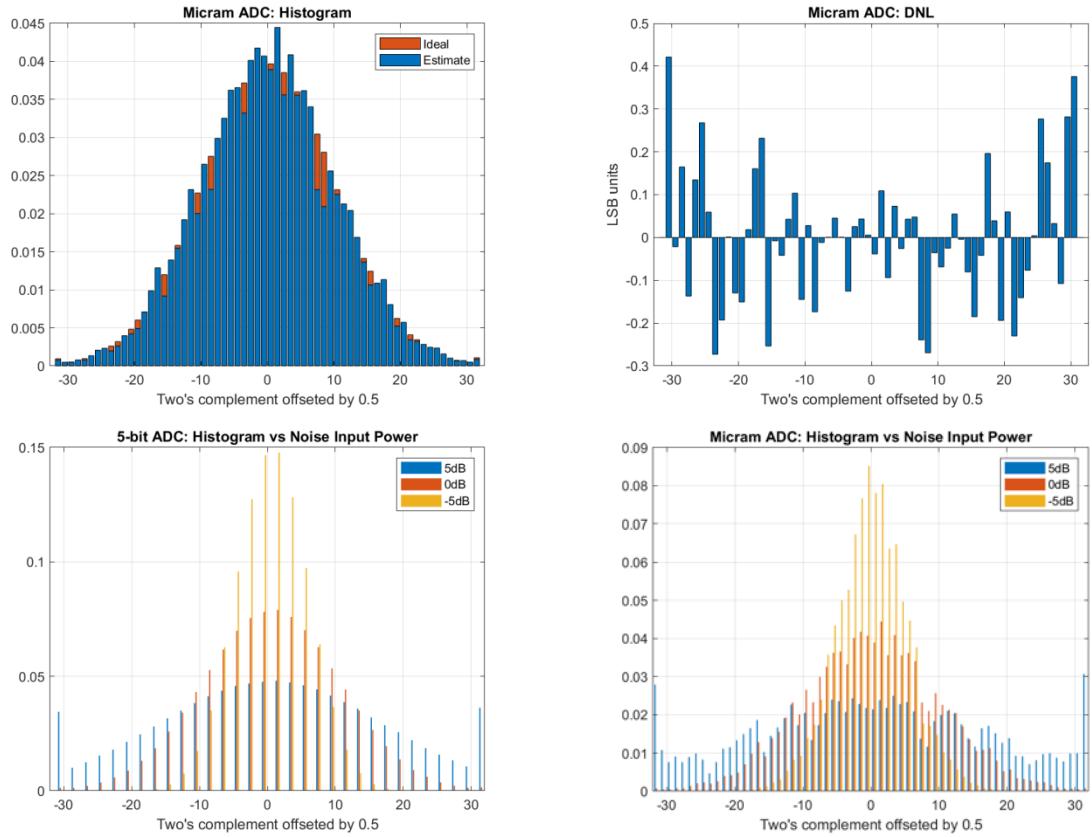


Figure 4: Impact of the number of physical bits



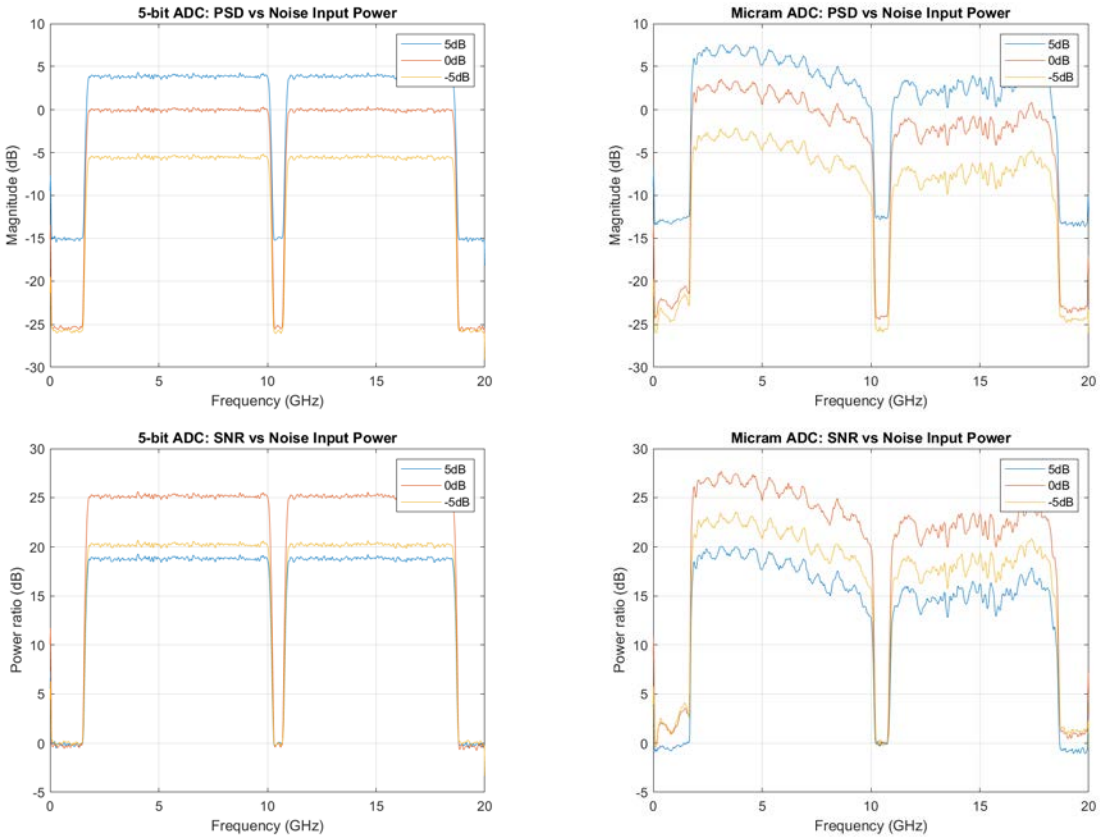


Figure 5: Impact of the input power and the residual non-linearity (after thresholds optimization)

The maximum efficiency that can be reached with N-bit resolution (N being the physical number of bits) is given by the theory in [13]: 99.9% for 6-bit, 99.7% for 5-bit, and 98.8% for 4-bit (see **Figure 4**, top left). From these values and Equation 1, we can compute the maximum SNR_{dB}: 30dB for 6-bit, 25dB for 5-bit, and 19.4dB for 4-bit. This is verified by the mathematical model, as shown in **Figure 4**, bottom right. In practice however, ADCs have non-uniformly spaced levels plus sampling noise (due to aperture and external jitter), that is why the quantization thresholds have to be finely tuned to optimize the measured SNR which is inevitably lower than the maximum theoretical values predicted for perfect ADCs (see **Figure 5**). Note that in case of saturation (e.g. the noise input power is 5 dB higher than the optimal), the maximum SNR degradation is due to the signal clipping which results in an increase in the digitization noise floor (see **Figure 5**).

To avoid this saturation, the ADC calibration process can be set in such a way that the threshold tuning will be optimized for an input power higher than the nominal power delivered by the receivers. Doing so, the digitization efficiency will be slightly lowered (for the nominal power), but the ADC will be able to accommodate some increase of the analog power, ensuring better linearity. If this analog power increase happens, then the efficiency will also increase, following the curve given in Figure 6, up to the saturation point.

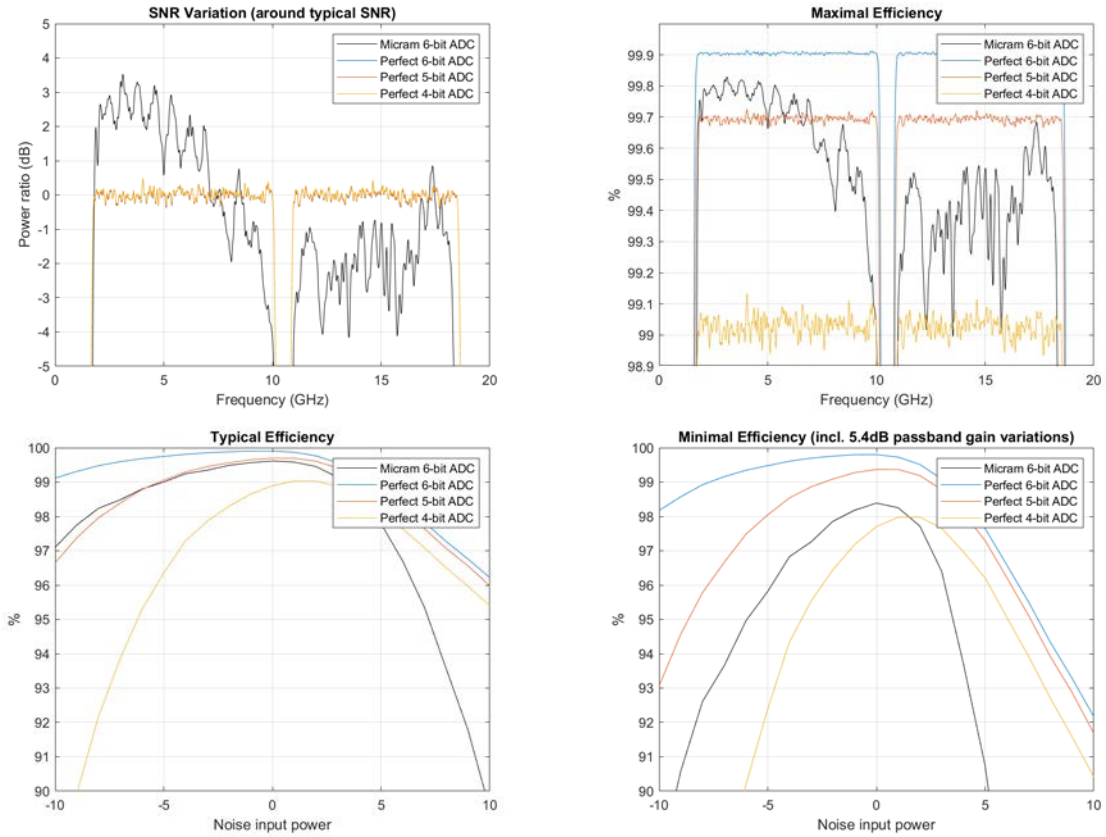


Figure 6: Efficiency measurements

From the SNR measurements and Equation 1, we can perform efficiency measurements that demonstrate the impact of the passband gain and the noise input power variations on the digitization efficiency. The SNR variation shown in **Figure 6** (upper left panel) explains why the maximal efficiency of the Micram device across the bandwidth is not constant, but in the range 99% - 99.8% (see **Figure 6**, upper right). Based on the typical efficiency variation in the linear region (noise input power < 0dB, **Figure 6**, lower left), the Micram ADC has comparable performance to a ideal 5-bit ADC. **Figure 6**, bottom right, shows that **the minimal efficiency would be 97.8% for standard astronomical observations** (passband gain variations < 5.4dB over 16 GHz, and signal level changes ≤ 4dB) and 92% for flux calibration/solar observation (signal level changes ≤ 13dB).

To put this performance in a global context, let us consider one of the original science drivers and improvement goals for ALMA 2030: a factor of 2.5 times increase in survey speed for galaxy detection (a rate if 2 galaxies per hour, see [14]). An effective imaging speed figure of merit of the instrument can be defined as: $(eff_{DG} \times eff_{corr}) \times BW$, for given digitizer and correlation efficiency $\mathrm{eff_{DG}}$ and $\mathrm{eff_{corr}}$, respectively and bandwidth BW. The current system is based on an ADC with 3 physical bits of resolution (yielding a maximum of 92% efficiency due to imperfections and passband gain variations), 2-bit correlation (88% efficiency), and 7.5 GHz instantaneous bandwidth per polarization. This results in an effective mapping speed figure of merit that scales as $(0.92 \times 0.88)^2 \times 7.5 \approx 4.9$. The proposed upgrade is based on 6-bit resolution ADC (97.8% efficiency), a minimum of 99% correlator efficiency (4 stages of 5-bit quantization → 98.8% efficiency) and 32 GHz instantaneous bandwidth per polarization. This results in an effective bandwidth of $(0.978 \times 0.99)^2 \times 32 \approx 30$, which in principle brings **a gain of a factor > 6 in the survey speed**. We note, however, that in observations requiring wide contiguous bandwidth, such as full spectral scans used for redshift searches or the characterization of chemical complexity of molecular clouds and protoplanetary disks, this factor of 6 is actually a lower limit. Due to the anti-aliasing filters and current IF band design, the current system is inefficient a providing complete, wideband spectral coverage; the USB/LSB gap for the current system (8.0 GHz for most receivers, except Band 6) is just above an integral multiple of the effective maximum bandwidth per sideband

(3.75 GHz). Hence, 3 rather than 2 tunings are needed to completely fill this gap, creating significant additional overheads associated with the extra tuning. Additionally, we note that for (single) line observations, where the bandwidth is not a limiting or major factor, the lower limit on the improvement in imaging speed is $(0.978 \times 0.99)^2/(0.92 \times 0.88)^2 \approx 1.4$ (where again, the lower limit is due to the current system featuring approximately ~2.3 ENOBs rather than 3).

3.3 Digitizer clock module

3.3.1 Specification on sampling clock

This section describes the preliminary specifications that can be defined on the sampling clock for a digitizer based on the Micram ADC.

- The 6-bit 40 GSps ADC from Micram accommodates two interleaved cores, each operating at 20 GSps. Thus, the sampling clock is 20 GHz.
- The power level of the clock signal in differential operation is around 0 dBm [15].
- The jitter of the clock is estimated from the following equations, giving the SNR in dB versus the physical number of bits or versus the jitter (see [16] and [17]).
    - $SNR = 6.02 \times n + 1.76$ (dB) with a single-tone signal
    - $SNR_{Jitter} = -20 \times Log_{10}(2\pi \times t_{jitter} \times f_{max})$ (dB)

    With f_{max} = 20 GHz and n = 6 bits, the jitter must be around 100 fs

NB: As the aperture time delay of the Micram ADC is not known, the rms jitter on the clock signal has been overestimated: we have taken a max analog frequency 20 GHz, worst case for 40 GSps digitization, and 6 bits, which is the physical number of bits of the Micram ADC.

Table 1: Sampling clock specification

	Min value	**Max value**	**Unit**
Sampling frequency		20	GHz
Power level at ADC input (differential)	-4	+5.6	dBm
Jitter clock		0.100	ps

3.3.2 Phase-locked loop device selection

During this study, a state-of-the-art of commercially available phase-locked loop devices (PLL) which could operate at 20 GHz has been performed. Several PLL devices ([18], [19] and [20]) have been characterized using manufacturer evaluation boards and a 125 MHz reference clock board already available in our lab. Our current baseline solution to design the future DGCK module is the LM2820 PLL from Texas Instruments (TI).

The LMX2820 is a wideband PLL with integrated VCOs (from 5.65 GHz to 11.3 GHz) that can generate a frequency of 20 GHz using an internal frequency doubler. This PLL can produce very low integrated jitter (40 fs obtained from phase noise at 20 GHz, integrated between 12 kHz and 20 MHz). The LMX2820 allows users to synchronize the output of multiple devices and is suitable for applications which need a deterministic delay between input and output. This device runs from a single +3.3 V supply and has integrated linear dropout regulators (LDO) which eliminate the need for onboard low-noise LDOs. This PLL has two differential RF outputs. The typical power level at each RF output is +3 dBm at 22 GHz, in single-ended configuration.

Because the fundamental VCO frequency is in the digitizer passband, the level of the spurious products will have to be measured and considered at system level. Various mitigation options have already been identified: the clock module could be assembled in a separate mechanical enclosure, with specific RF gaskets between lid and body, SMA and panel, to prevent RFI leakage, some reflectionless bandpass filters could be placed on the clock path to attenuate the conducted perturbation, and microwave absorber could be glued in the cavity to attenuate

the radiated interferences. Moreover frequency offsetting could be implemented on the array with a specific scheme per antenna and polarization to mitigate the interference.

The test bench (shown in **Figure 7**) used to evaluate the LMX2820 PLL is composed of the evaluation board of the PLL, a laboratory power supply for the +3.3 V, the Reference Pro board from TI to provide a clean 125 MHz clock, and a 26.5 GHz spectrum analyzer to capture the phase noise of the RF output signals.

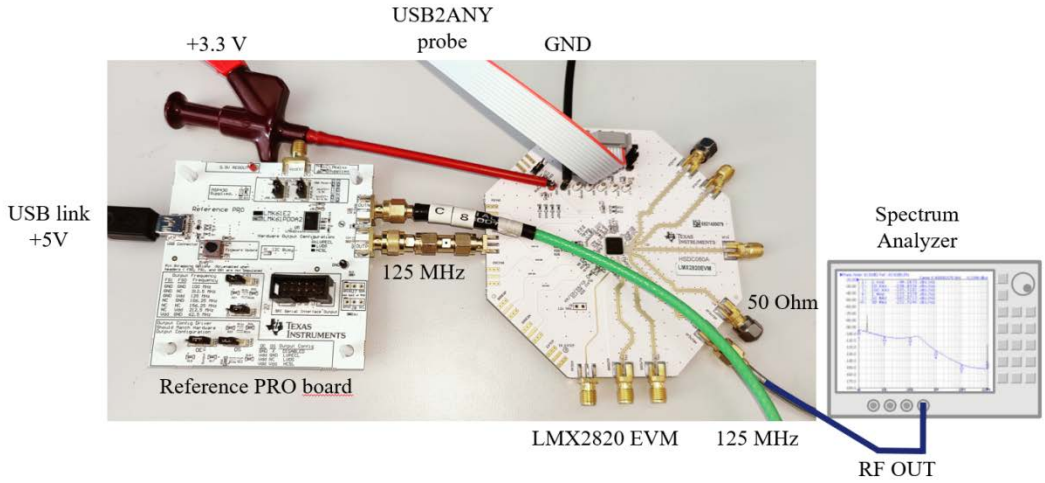


Figure 7: Test bench for LMX2820 evaluation

The measured phase noises of the 125 MHz clock and of the RF output are summarized in Table 2 below.

Table 2: Phase noise of the reference clock and of the RF output

Offset frequency	125 MHz ref signal	20 GHz signal
100 Hz	-118 dBc/Hz	-80 dBc/Hz
1 kHz	-130 dBc/Hz	-97 dBc/Hz
10 kHz	-140 dBc/Hz	-100 dBc/Hz
100 kHz	-141 dBc/Hz	-100 dBc/Hz
1 MHz	-148 dBc/Hz	-112 dBc/Hz
10 MHz	-161 dBc/Hz	-139 dBc/Hz
100 MHz	-160 dBc/Hz	-150 dBc/Hz

The values given in Table 2 are estimated from the curves in **Figure 8**.

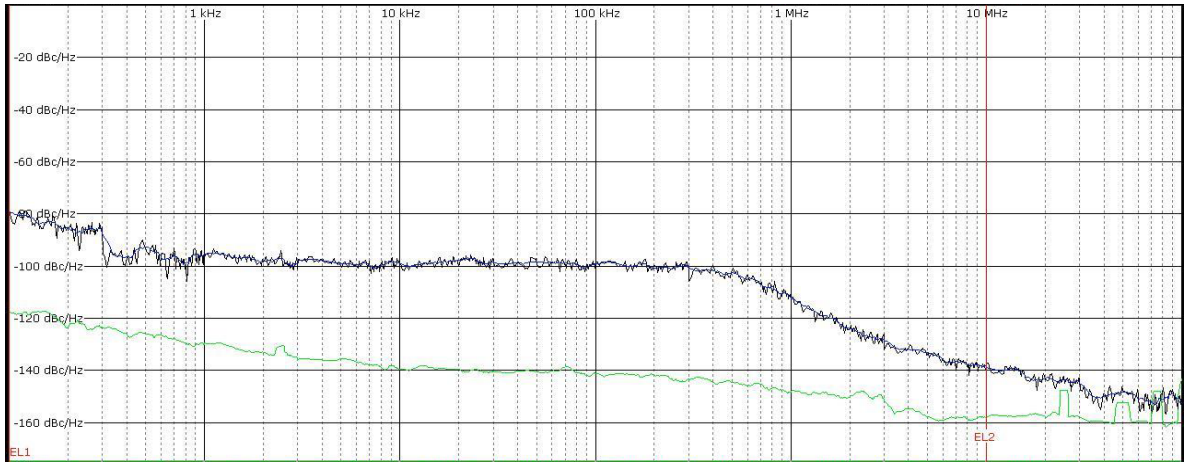


Figure 8: Phase noise of the 125 MHz ref signal (green curve), of the RF output (blue/black curve)

The RMS jitter measured with the LMX2820 evaluation board with the 125 MHz provided by the Reference PRO board is 90 fs by integrating the phase noise at 20 GHz between 100 Hz and 100 MHz.

Note that the loop filter implemented on the LMX2820 evaluation board is not optimized to exhibit minimal jitter at 20 GHz. The 125 MHz reference clock provided by ALMA system should be cleaner than the one provided by the Reference PRO board from TI. We have used the software tool PLLatinum Sim from TI to simulate the LMX2820 and to estimate the jitter at 10 GHz for the following configurations:

1- Default filter loop with our 125 MHz reference signal (current test bench)
2- Loop filter optimized for minimal jitter at 10 GHz with our 125 MHz reference signal
3- Loop filter optimized for minimal jitter at 10 GHz with a 125 MHz clock described in Table 3

Table 3: Phase noise of the ALMA 125 MHz reference signal [21]

Offset frequency	Phase noise
100 Hz	-131 dBc/Hz
1 kHz	-155 dBc/Hz
10 kHz	-175 dBc/Hz
100 kHz	-177 dBc/Hz

The estimated jitter for each configuration is described in Table 4 below.

Table 4: RMS jitter at 10 GHz

Configuration	Jitter (integrated from 100 Hz to 100 MHz)
Evaluation board with our 125 MHz	115 fs
Loop filter for best jitter with our 125 MHz	97 fs
Loop filter for best jitter with the ALMA reference	53 fs

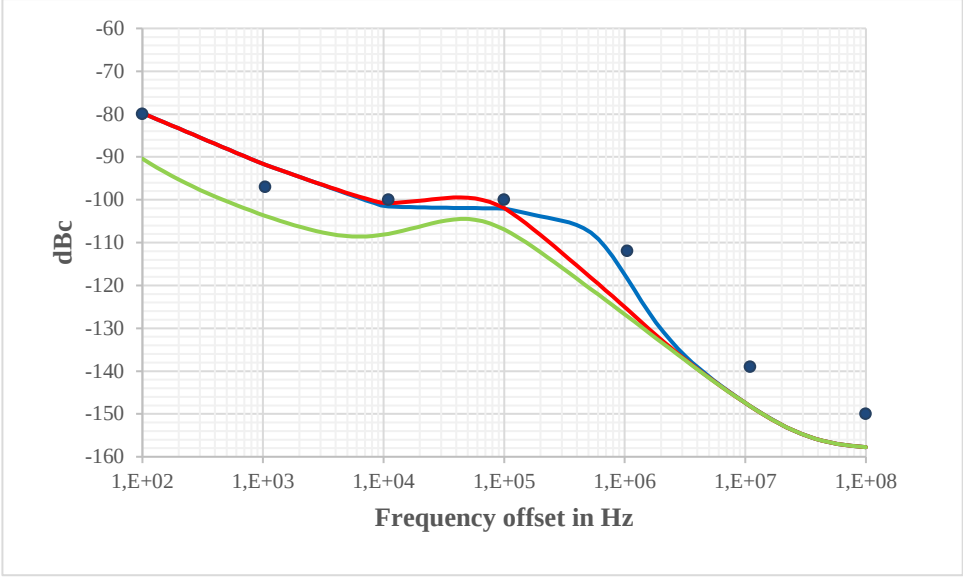


Figure 9: Phase noise at 10 GHz for current test bench. The simulation is shown in blue, the measurement at 20 GHz is in dotted blue, the best jitter with our 125 MHz is in red, and best jitter with ALMA 125 MHz is in green.

The RMS jitter is calculated from the phase noise curve (*PN(f)*) by equation below:

$$RMS\ Jitter = \frac{\sqrt{2\int_{f1}^{f2} 10^{\frac{PN(f)}{10}} df}}{2\pi fc}$$, where $\int_{f1}^{f2} 10^{\frac{PN(f)}{10}} df$ is the noise power between frequencies f1 and f2 on each side of the carrier frequency fc.

The contribution of the internal frequency doubler on the phase noise must be taken into account. The comparison between the simulated phase noise at 10 GHz (blue curve) and the measured phase noise at 20 GHz (blue dot) shows that the frequency doubler increases the phase noise of around 6 dB for frequency offsets above 1 MHz. So the RMS jitter at 20 GHz is not half of the RMS jitter at 10 GHz. If the loop filter is optimized to minimize the RMS jitter, the latter could be below 97 fs which is in agreement with our specification (Table 1).

A simplified block diagram of the future DGCK module is described in **Figure 10**. Two LMX2820 PLL are used to generate the 20 GHz clocks which feed the four Micram ADCs in a differential configuration. The PLLs are mounted on a printed circuit board with RF surface mount components (RF baluns, pass-band filters centered at 20 GHz, attenuators, amplifiers) for each RF output. The printed circuit board is assembled inside a mechanical enclosure with RF shielding. Several cavities are milled in this enclosure to isolate each RF output path from the others. Reflectionless bandpass filters, XBF-24+ from Mini-Circuits, are used to absorb and terminate stopband signals. The 10 GHz signal and its harmonics at 30 and 40 GHz (also harmonic of 20 GHz) are attenuated to avoid radiation (or emission). A gain block amplifies each RF output to provide a signal with a power level of +3 dBm in differential configuration. The single-ended-to-differential conversion is performed using an RF balun (MTY2-243+) from Mini-Circuits. An alternative is to implement this conversion at the input of the digitizer board in order to simplify connectivity.

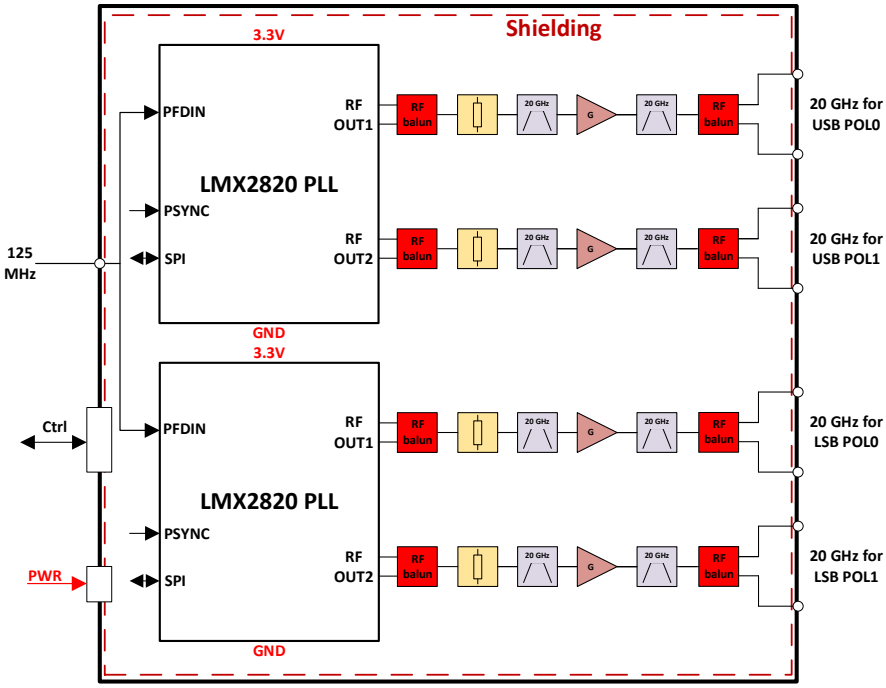


Figure 10: Simplified bloc diagram of the DGCK module

4 Data transmission system

The antennas are connected to the AOS technical building through a network of optical fiber cables. Each antenna is connected with eight single-mode optical fibers, allocated as follows: one fiber for the Data Transmission System, one fiber for the Photonics Local Oscillator reference, two fibers for the monitoring and control signals, and four spare fibers (see **Figure 11** below from [22]).

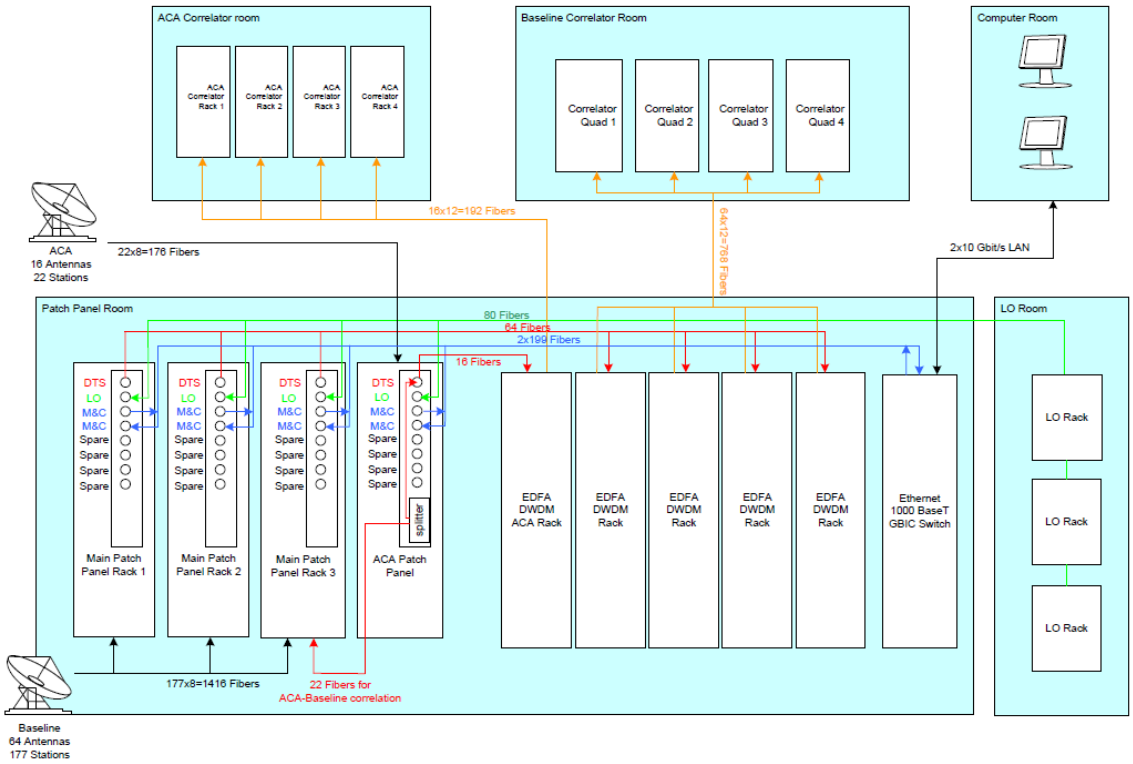


Figure 11: Existing network of optical fiber cables

The current system is based on 20 channels Mux/Dmux 10G DWDM where only 12 channels are populated. The current throughput of 120 Gb/s per antenna could then be increased up to 200 Gb/s, but regardless this would not be sufficient to support the IF doubling, which is a minimal objective for ALMA 2030.

4.1 DSP/OT Board

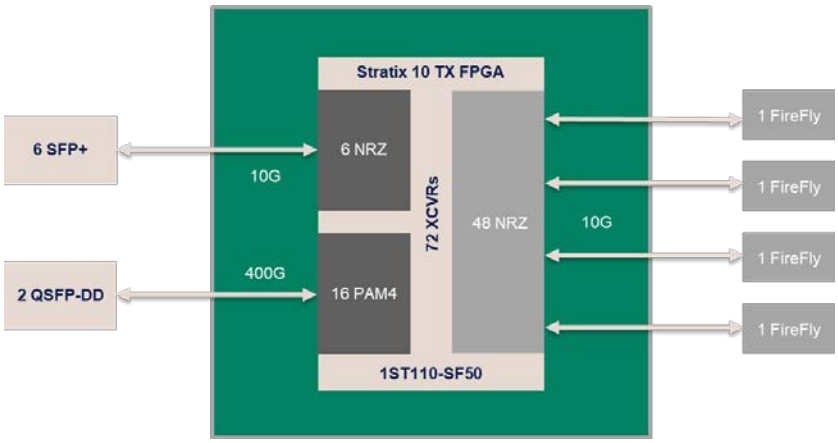
In order to ease the transition from the current to the future systems, we have selected both 10G SFP+ (Small Form-factor Pluggable Plus) and 400G QSFP-DD (Quad Small Form-factor Pluggable Double Density) optical transceivers for the **generic DSP/OT FPGA board** design (see **Figure 12** and Section 5). Note that 10G SFP+ could be implemented using prototypes for on-site demonstration only. They might not be required during the deployment phase.

Based on the required number of PAM4 (for 400G) and NRZ (for 10G) transceivers, we have selected the Intel FPGA Stratix10 TX 1ST110-SF50 for the DSP/OT board. According to Intel support, considering the ALMA site location and the number of FPGA (264), the expected MTBF (Mean Time Between Failures) due to SEU (Single Event Upset) is 224 hours with this device.

The unformatted data streams from the ADCs are fed into clock recovery and data aligner circuitry, channelized using Oversampled Polyphase Filter Bank (OPFB) and re-formatted by the DTX for long haul transmission to the correlator for final processing. This multi-step process provides flexibility (by adapting the data streams) making it possible to interface with:

- the current optical system with a maximum throughput of 200 Gb/s,
- the upgraded optical system with more than 400 Gb/s throughput.

At the other side of the optical fiber, the digital samples are retrieved and could be re-channelized by the DRX, and then the TFB would perform digital down-conversion to extract the sub-bands (SB) that feed the correlator (see Section 5 and **Figure 15** for details).



Stratix® 10 TX Devices – Package Plan

Stratix 10 TX Device	F1152C HF35 – 24 XCVRs total (35x35 mm²)				F1760C NF43 – 48 XCVRs total (42.5x42.5 mm²)				F2397C UF50 – 96 XCVRs total SF50 – 72 XCVRs total (50x50 mm²)				F2912B YF55 – 144 XCVRs total (55x55 mm²)			
	GPIO	3V IO	LVDS Pairs	XCVR (E,H)	GPIO	3V IO	LVDS Pairs	XCVR (E,H)	GPIO	3V IO	LVDS Pairs	XCVR (E,H)	GPIO	3V IO	LVDS Pairs	XCVR (E,H)
1ST040	384	0	192	24,0												
1ST085					440	8	216	24,24	440	8	216	48,24				
1ST110					440	8	216	24,24	440	8	216	48,24				
1ST165									440	8	216	72,24				
1ST210									440	8	216	72,24				
1ST250									440	8	216	72,24	296	8	144	120,24
1ST280									440	8	216	72,24	296	8	144	120,24

Pin migration across devices within family

Figure 12: DSP/OT Board (DTX/DRX/TFB) based on Stratix10 FPGA

4.2 Optics transceivers

One of the ALMA2030 priorities is to implement more extended baselines. The cable length to such remote new antenna pads may be significantly longer than the baseline length to the AOS; lengths of 50 or even 60 km cannot be excluded at this point, while the distance between the AOS and the OSF is below 40 km. The 400G ZR Data Center Interconnects (DCI) technology allows for transmission reach up to 120km, making it an ideal solution for the Antenna to AOS links. Inphi (now part of Marvell) and NeoPhotonics announced earlier in 2021 the general availability of 400ZR QSFP-DD pluggable coherent optics transceivers.

Considering the 66 antennas and 4 optics transceivers per antenna, 48 SMF are available for this connection whereas 264 fibers would be required. Installing additional fibers (264-48=216) might not be possible, so we have identified a fully commercial solution for a complete **40 channels Mux/Dmux DWDM module compatible with 1/10/40/100/200/400G Ethernet**. Eight of these modules would increase the ALMA optical transport capacity up to 2 Tb/s per antenna, while only using 8 SMF fibers. This solution combined with 400G ZR transceivers allows for Antenna to AOS distance up to 80 km.

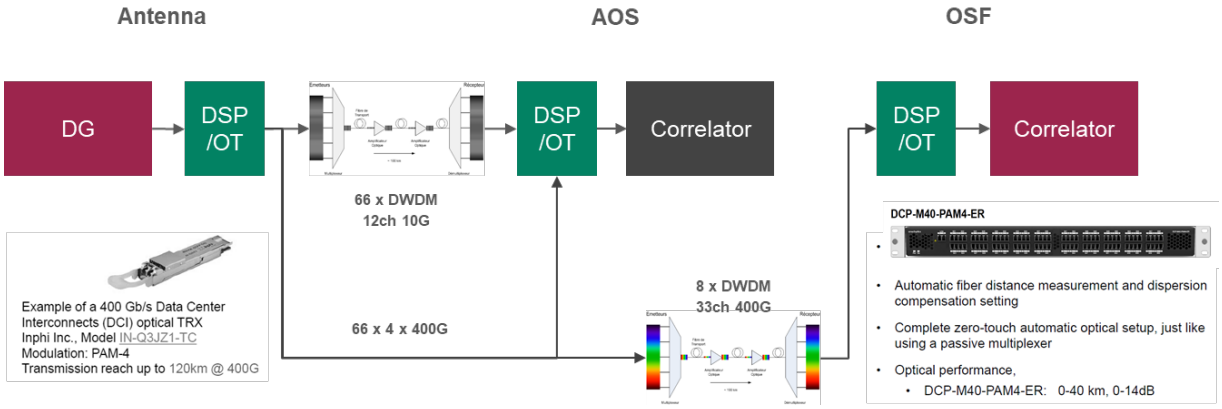


Figure 13: Data transmission from antennas to correlator

4.3 Data transmission protocol

The QSFP-DD transceiver presents an 8-lane electrical interface (up to 50 Gb/s per lane). Because transmission delays and errors can occur on each of them independently, synchronization is a serious system issue to be considered. The most natural strategy consists in transmitting 1 bit per lane and reconstructing the 6 bits samples at the other end of the fiber. This would require 6 lanes running at 40 Gbps. However, we believe that transmitting frequency chunks (typically 2 GHz sub-bands) per lane would be a better option for various reasons. First, it would require 8 lanes running at "only" 30 Gbps (5 GSps x 6-bits), making it easier to synchronize the data and to correct any transmission errors. Moreover, the frequency division that could be applied at both ends of the transmission system in the DSP/OT board is required as part of the FFX correlator architecture. Actually, the FPGA required in the DSP/OT board to transmit and receive data are sized by the XCVR requirements and will offer plenty of computational resources which will be wasted if not used for DSP. So we stress that implementing a "first F at the antenna" and more generally considering the DSP/OT as potential DSP stages as part of the overall correlator architecture, should be considered very seriously by the project, especially because it may result in overall cost savings and ease the synchronization issue related to the transmission system.

The current DTS is based on a custom frame protocol (data link layer within the semantics of the OSI model) associated with a Virtual Parallel Bus system (physical layer). The frame consists of a synchronization word, a sequence word, payload, and a checksum (see **Figure 14**). The frame is scrambled with a pseudo random pattern to provide adequate recovery timing information and a reduction of low frequency content. The VPB supplies a 192-bit wide word clocked at 125 MHz to the correlator inputs. It requires exact synchronization across all optical and electrical components within the VPB. In addition, the VPB must compensate for changes in the propagation times due to variations in the environmental factors affecting the optical fibers. With skew and propagation effects eliminated, correct timing sequencing is maintained throughout, from the digitizer to correlator.

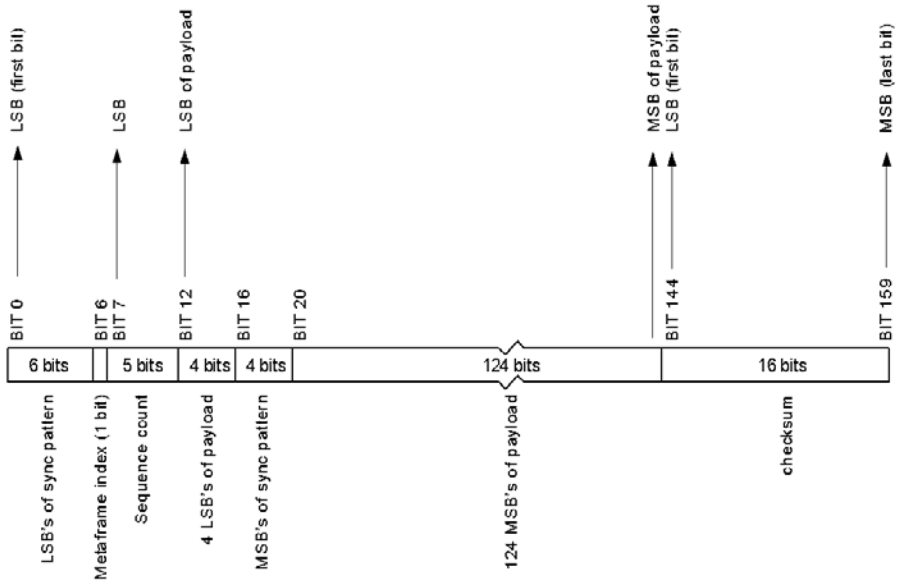


Figure 14: Current DTS system 160-bit frame organization (128-bit of payload)

Today's FPGA transceivers embed a physical layer that would naturally replace the current VPB. Because these transceivers are asynchronous, the current data link protocol should be revised to retain the ability to compensate for latency changes. One can think about the Ethernet protocol which uses a unified physical layer leading to lower prices and vast choice of network components but the standard data link layer of the Ethernet protocol does not exactly fit our need for continuous and unidirectional communication. Because we will not use the Ethernet protocol for what it has been designed, we may have to use the Ethernet physical layer combined with a custom data link. Moreover, the use of standard Ethernet data link requires time stamping which could be

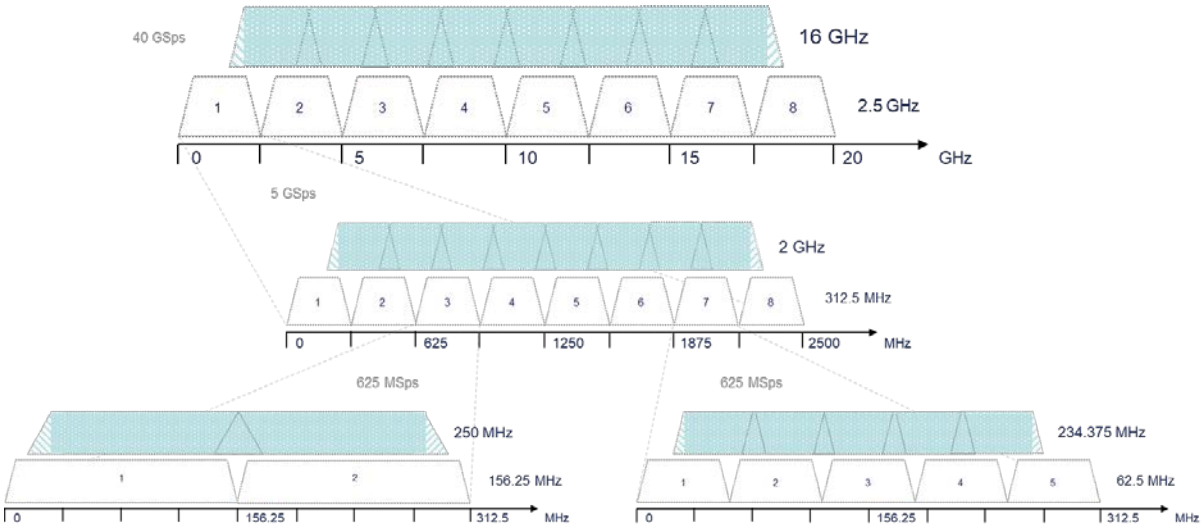
difficult to implement using the Micram ADC because it does not support advanced protocols such as JESD204. To synchronize multiple ADCs, we have to switch to a strobe signal at the digitizer input and to process the delay on the signal path from each DG. The strobe signal arriving on multiple DG and DTX must be synchronized and phase-locked. Once the delays are processed within the DTX, time stamping could be performed using the strobe signal as a time reference. The existing 48ms TE could be used as a strobe signal if it is provided to the receivers since the DG will be located near the FE Assembly.

5 Digital Signal Processing

Digital Signal Processing (correlation excepted) is performed using FPGA at different stages along the signal path, at the antenna, and at the AOS building. In the current system, digital samples generated by the digitizer are captured and formatted by the DTX, prior to optical transmission. At the other side of the optical fiber, the digital samples are retrieved by the DRX, then the TFB performs digital frequency conversion and filtering to extract 62.5 MHz or 31.25 MHz sub-bands that feed the correlator.

For the upgrade, state-of-the-art FPGAs are required at both ends of the optical fiber, because we need a large number of high-speed FPGA transceivers to capture, transmit, and receive the extended data flow. Since this kind of FPGA will necessarily come with a very large number of computational resources, various partitioning configurations of the overall DSP between the antenna, the AOS, and the OSF buildings can be considered in order to minimize the cost and facilitate deployment. In particular, we stress that having a first DSP stage like a frequency division at the antenna is the most straightforward strategy to transmit the overall data stream over the optical system. Reference [23] gives an overview of the possible configurations and solutions we have identified using Intel Stratix 10 FPGA. Note that the Stratix 10 GX/SX presented in this reference has been replaced by a Stratix 10 TX device, allowing increased data rates up to 56 Gbps, in **Figure 16**. We also explain how FPGA versatility could be used to achieve compatibility with various generations of receivers and correlators. For example the TFB could implement different sampling clocks, band-pass ratios, and quantization factors:

- 312.5 MHz x 0.40000 x 128 = 16.00 GHz /polarization /sideband
- 125.0 MHz x 0.46875 x 128 = 7.50 GHz /polarization /sideband
- 62.5 MHz x 0.46875 x 128 = 3.75 GHz /polarization /sideband



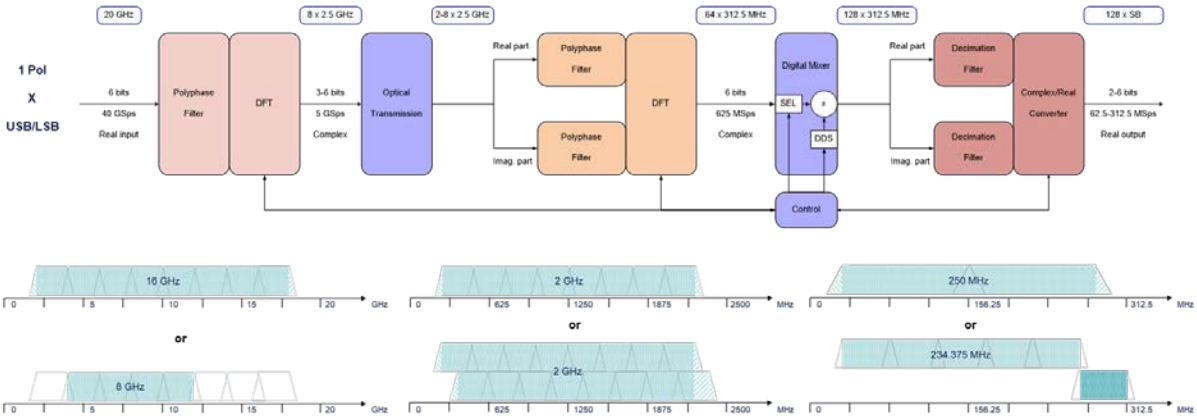


Figure 15: DSP architecture example using several stage of OPFB

One important conclusion is that **the transceiver requirements and DSP partitioning are compatible with the idea of a generic DSP/OT board** (see Section 4.1) that could be used at both ends of the optical data transmission system **to support the current DTX, DRX, and TFB functions**, as shown in **Figure 16**. Note that DRX and TFB functions can be merged in a single Stratix10 FPGA. The only differences would be the firmware to be implemented and the "input/output direction". This would be a tremendous advantage in terms of validation, manufacturing, fault analysis, and maintenance.

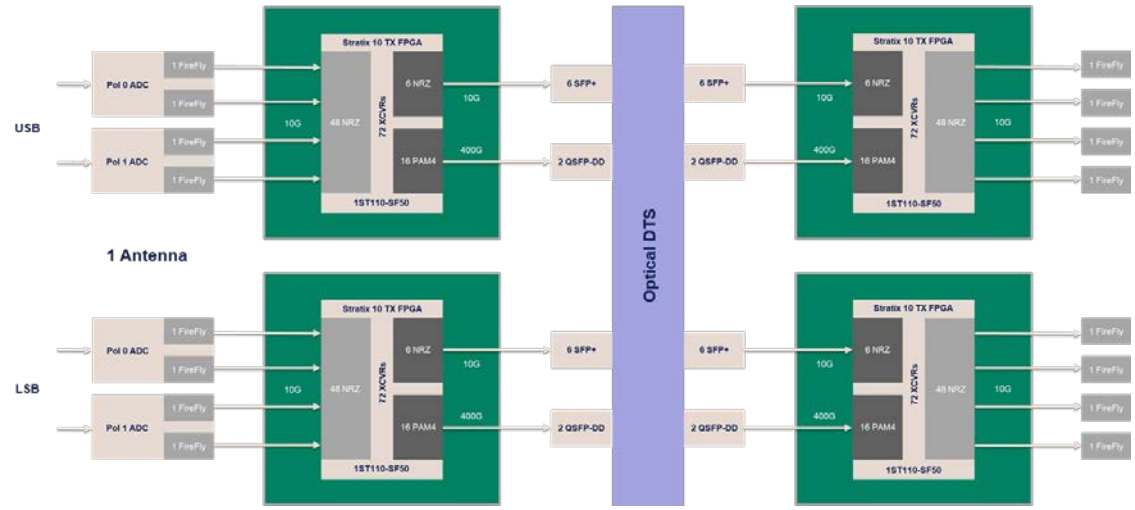


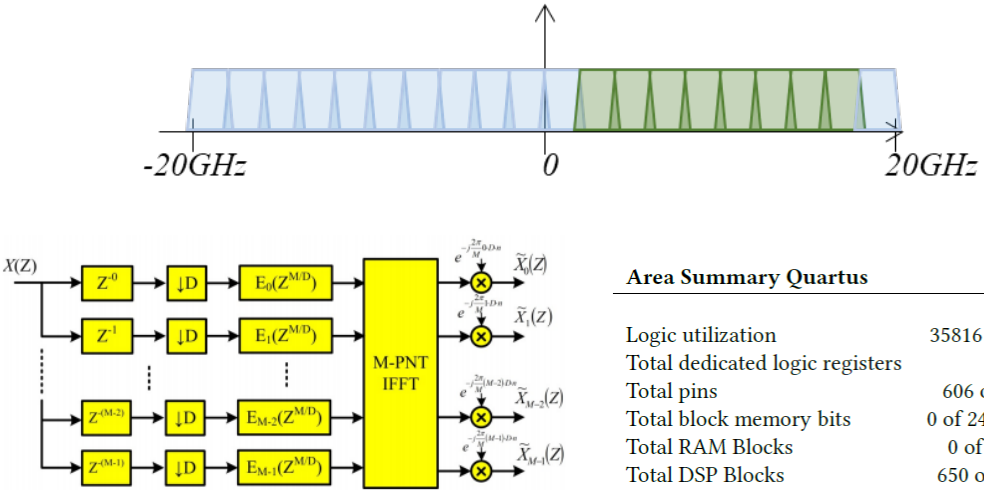
Figure 16: DSP partitioning example, based on the DSP/OT board

5.1 OPFB

The use of an Oversampled Polyphase Filter Bank (OPFB) provides the ability to switch between Time Division Multiplexing and Frequency Slicing keeping the same usable bandwidth and throughput. During this study, we have performed HDL implementation and validation of tunable OPFB with D-parallel M-point FIR and DFT. The block diagram of the OPFB is given in Figure 14. The design specifications are:

- Internal clock: 312.5 MHz
- Input: 2-18 GHz IF oversampled at 40 GSps
- Output: 8 base-bands of 2 GHz oversampled at 5 GSps
- OPFB Ratio: 8/20 (D=8, M=20)
- Frequency overlap using OPFB for full continuous frequency coverage

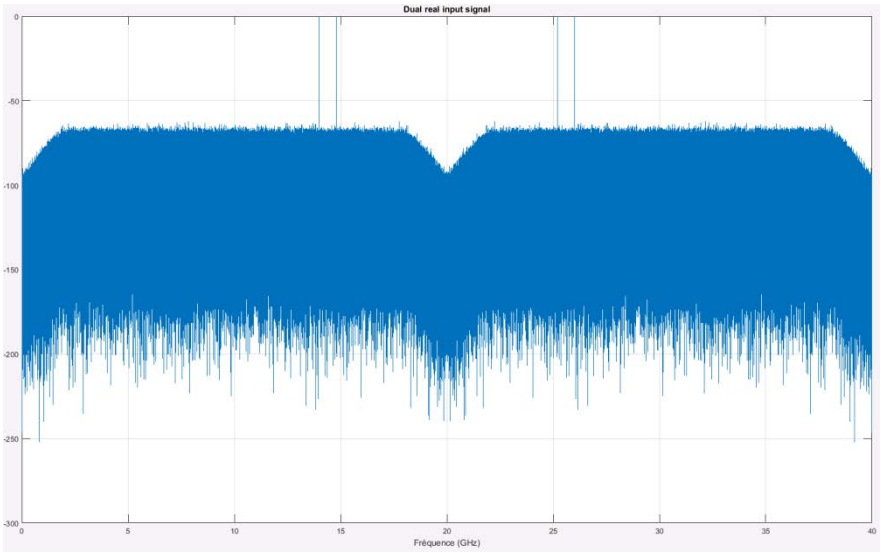
Based on the resource counts (see **Figure 17**), we can confirm that the extraction of 8 base-bands of 2 GHz in 2 polarizations is possible using a single DSP/OT board. Note that the final specifications of the OPFB may be different from the one presented here, but this will not substantially change the general DSP principle, its implementability, and the FPGA resource estimation. Specially, the IF absolute position may be any 16 GHz within the range [2-19.5] GHz (see discussion in Section 5.3).



Area Summary Quartus

Logic utilization	35816 of 933120 (4%)
Total dedicated logic registers	88707
Total pins	606 of 704 (86 %)
Total block memory bits	0 of 240046080 (0 %)
Total RAM Blocks	0 of 11721 (0 %)
Total DSP Blocks	650 of 5760 (11 %)

Figure 17: OPFB block diagram and implementation results using Intel FPGA Stratix10 GX 1SG280



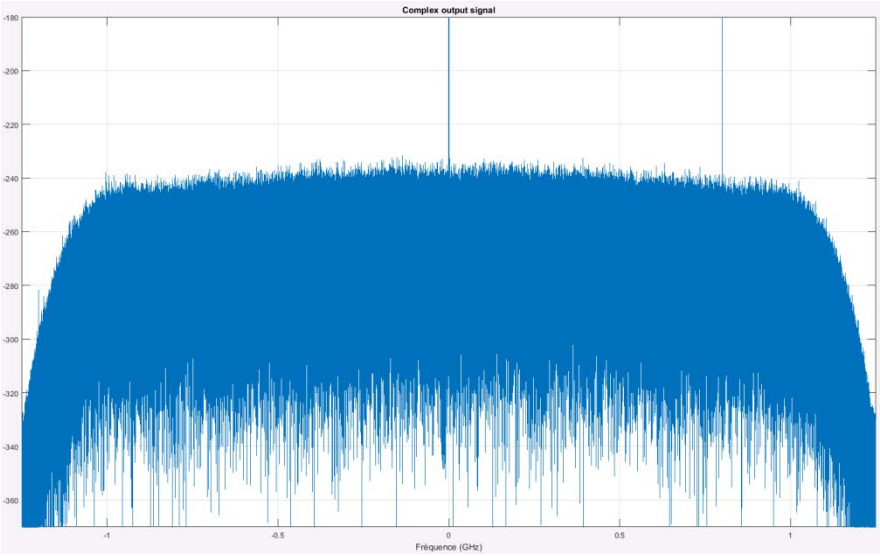


Figure 18: MATLAB simulation of 2 GHz base-band extraction from 16 GHz IF

5.2 Phase switching and delay compensation

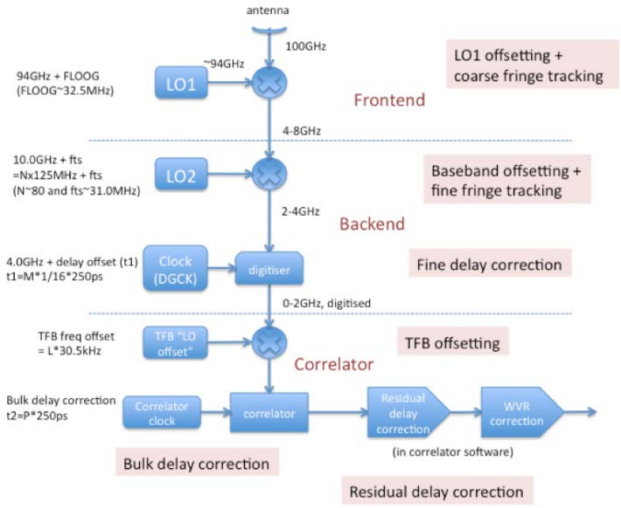


Figure 19: LO mixing and delay correction

In the current ALMA system, there are three frequency conversions along the signal path from the front-end to the correlator. The associated LO and IF sub-systems perform multiple functions (see [24]) including phase switching and delay tracking. The 180° phase switching capability is implemented to suppress spurious signals and IF crosstalk between the first LO in the receiver and the digitizer. Demodulation is currently performed in the DTX. The fine delay tracking (or time offset) is applied on the 4 GHz digitizer clock in units of 1/16 of the clock period in the digitizer clock module. Finally, the digital LO in the TFB (**Figure 19**) can be used to offset the frequencies in conjunction with the receiver LO to suppress interference and select the sideband. Upgrading the digital system, we must keep / optimize / enhance these functionalities.

With an output frequency of 20 GHz and jitter of 0.1 ps, the specifications for the new digitizer clock module are already very ambitious. Performing phase control of the digitizer clock, like in the current system, would require more active components which would decrease the basic performance and reliability of the module. Being in charge of the maintenance of the current one, we have also experienced a lot of failure concerning this module. Basically, the higher the analog part complexity is, the lower the system reliability is.

Since digital filtering implementation is considered, we propose to use fractional delay filters in order to apply the fine delay correction digitally (see **Figure 20**), with a delay step of 1.5625 ps (sampling period / 16). A fractional delay filter (FDF) is a filter that delays the digital samples by any fraction of its sampling period, say τ = δT, where τ is the fractional delay; δ is the fraction |δ| ≤ 1; and T is the sampling period. The legacy design of any FDF falls in line with the interpolators, among which polynomial interpolation and polyphase filters are the two most commonly used techniques. Notice that the basic Fourier transform property states that time delay is phase shift, and the phase shifter has frequency response $S(\Omega) = e^{i\Omega\tau}$ where **Ω** is the continuous frequency in Fourier transform. From the spectral approximation point of view, the problem becomes using M spectral samples to approximate complex sinusoids $e^{i\frac{2\pi}{M}m\tau}$, for m = 0 … M-1 and |τ| ≤ 0.5.

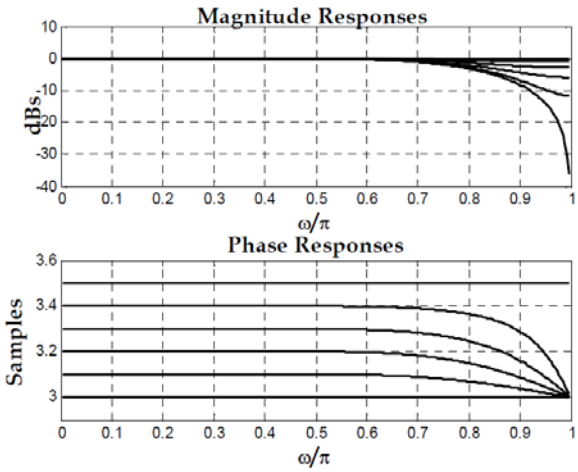


Figure 20: Frequency response of a fractional delay filter (Farrow structure)

As shown in Fig. 20, the response is non-ideal, and varies between different delay states near the Nyquist frequency. But combined with a decimation filter (with at least a factor of 1/2) that could be introduced in the DSP chain prior to the correlator (see **Figure 15**), the non-ideal region near the Nyquist frequency would become out-of-band. Using several stages of OPFB, we can easily apply the polynomial interpolation technique of fractional delay filter (Farrow structure) on a reduced bandwidth signal. So, in addition to an OPFB that extracts 250 MHz base-bands, the DSP/OT board at the correlator side could also perform the global geometric delay (coarse + fine) compensation.

5.3 IF setups for continuous wide spectral coverage

For redshift searches and other science use cases requiring complete spectral scans, several tunings are required to fill the gap between the LSB and USB. **Figure 21** is an example of IF 4-20 GHz 2SB setup with 6 tunings (see [25]) providing double coverage over 88 GHz (single coverage in the outer 8 GHz on each side). Double coverage is often useful to detect or confirm faint lines.

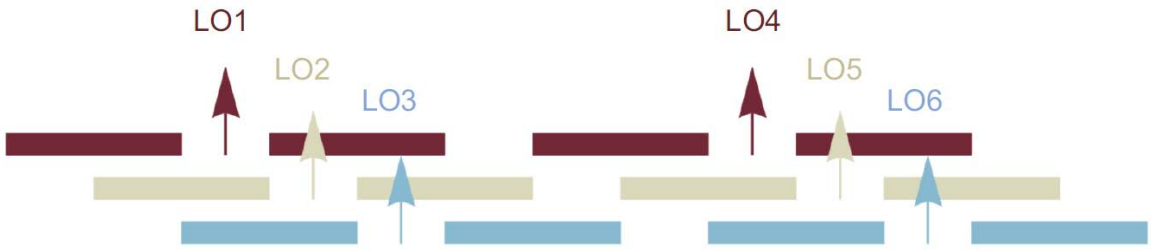


Figure 21: IF coverage 4-20 GHz 2SB: 6 tunings for 88GHz double coverage

But the digitizer running at 40GSps cannot sample input signal at 20GHz due to the antialiasing filter. The proposed IF 2-18 GHz to be extracted is indeed optimal from a scientific point of view, but some receivers may only be able to provide 4-20 GHz due to other technical limitations. That is why we propose to digitize [2-19.5] GHz IF. This allows for 2-18 GHz compatible receivers to deliver 16GHz to the correlator. For the others, 3.9-19.5 GHz IF would allow for continuous double coverage of 85.8 GHz with 6 tunings (IF 15.6 GHz instead of 16 GHz).

6 Control/Monitoring

The current control/monitoring system is based on CAN Bus. The fastest transmission rate is 1 Mbps which was sufficient 20 years ago but now presents as a strong limitation, since there were no speed improvements in the last 20 years. The bus length is limited to 40m at the fastest transmission rate; therefore computers are required in the receiver cabin and the AOS technical building. The NRAO group proposes to use Ethernet Switch to replace the current Antenna Bus Master that converts Ethernet packets sent from/to the OSF to CAN bus for Front-End and Back-End equipment M&C.

To minimize the change on the ALMA control monitoring system, a general strategy to be investigated consists in using the FPGA in the DTX and in the DRX/TFB to perform local self-consistent control monitoring and disrupt the ALMA control monitoring system only for sending final status and information required at the system level (e.g TFB sub-band power measurement used for spectral stitching). This is probably feasible by taking advantage of the processors which are now commonly embedded in the FPGAs we plan to use. As an example, there have been discussions with the NRAO correlator group about functions that could be included in the DTS FPGAs to improve performance and relax the constraints on the ALMA control monitoring system:

- Calculate scaling factors in the FPGA, saving considerable processing time in the SCC microprocessor.
- Continuously measure baseband total power and provide it, on request, to the SCC microprocessor.
- FPGA remote update capability especially for subsystems deployed within the antenna: updating the FPGA bitstream is not something that happens often, but when it becomes needed it can be a heavy task.
- Enhance the set of test patterns: provide a test pattern that allows to ensure the data integrity, provide a Gaussian distributed pseudo random noise plus a set of tunable tones that allows to set the correlation levels between pairs of antennas.
- Ensure compatibility with the ALMA VLBI phasing system

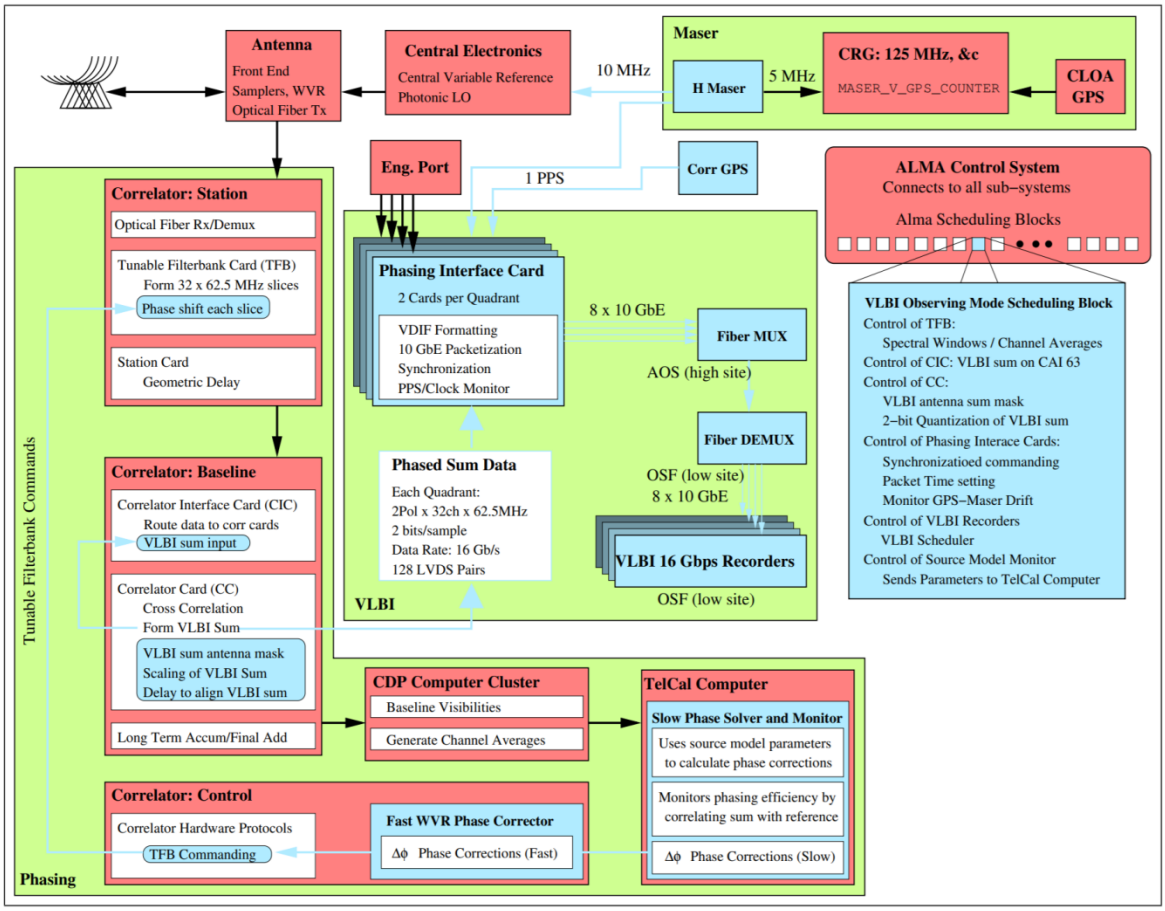


Figure 22: The ALMA phasing system

7 Prototyping, Onsite demonstration, and production

In this section we give an overview of the current plans we have for prototyping, onsite demonstration, and production in terms of schedule and cost. This preliminary plan will be refined and consolidated during the next weeks and months, depending on the final recommendations from various ALMA working groups on the front-end, digitizer, signal path, and correlator upgrades. It is based on the 3 step deployment strategy described in **Figure 1**. This strategy was defined to ensure relative independence versus the concurrent upgrade projects and to ensure backward compatibility with the current system, both of which are suggested important objectives. This may be totally reconsidered in the near future if required. We stress that demo/prototyping is not required from a design point of view but primarily from a system point of view.

- Small project proposal obtains ALMA Board approval: 04/2022
- Prototype: 2023
- System demonstration: 2023
- Preliminary design review (block diagram DG, DGCK, FPGA): 02/2024
- Detailed design review: 2024
- (Pre)-production: 2024-2026
- Integration: 2025-2026

In the following tables we give rough estimates of the hardware cost for a possible onsite demonstration (Table 5) with 2 antennas and for the full production (Table 6) of the ALMA digital system, including digitization, data transmission, and digital signal processing. Note that most of the device costs are not based on official quotations for volume production and that the exact number of items to be built and delivered is still to be determined, including consideration of the long term maintenance strategy.

Table 5: Onsite demonstration cost

Description:	**Cost:**	**Comment:**
Analog backend Module	100 k€	Cost based on RF connectorized components.
Digitizer module	170 k€	Digitizer boards ADC cost: 20 k€ per unit.
DGCK Module	10 k€	Cost based on COTS PLL.
DTX, DRX, and TFB	170 k€	Generic DSP/OT boards FPGA cost: 7 k€ per unit.
Optical components	100 k€	SAMTEC FireFly modules, SFP+ transceivers (10 GbE), QSFP-DD transceivers (400 GbE), Optic cables
Total cost	**550 k€**	**To equip 2 antennas**

Table 6: Full production cost

Description:	**Number**	**€ / unit**	**k€**
DG			
PCB	66 antennas *2	2000	264
ADC	66 antennas *4	8000	2112
DGCK	66 antennas	1400	92.4
DSP/OT			
PCB	66 antennas *4	2000	528
FPGA	66 antennas *4	5000	1320
ODTS			
DWDM	8	15000	120
400G	66 antennas *8	5000	2640
Total cost			**7076.4**

APPENDIX

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Abbreviations and Acronyms:

ADC	Analog-to-Digital Converter
ALMA	Atacama Large Millimetre/submillimetre Array
AOS	ALMA Operations Site
ASIC	Application-Specific Integrated Circuit
BiCMOS	Bipolar CMOS
CAN	Controller Area Network
CMOS	Complementary Metal Oxide Semiconductor
CNES	Centre National d'Etudes Spatiales
COTS	Commercial off-the-shelf
CUP	Correlator Upgrade
CW	Continuous Wave
DCI	Data Center Interconnects
DFT	Discrete Fourier Transform
DG	DiGitizer
DGCK	DG Clock module
DMUX	Demultiplexer
DNL	Differential Non-Linearity
DRX	Digital Receiver
DSP	Digital Signal Processing
DTX	Digital Transmitter
DWDM	Dense Wavelength Division Multiplexing
EMI	Electromagnetic Interference
ENOB	Effective Number Of Bits
ESA	European Space Agency
ESO	European Southern Observatory
FDF	Fractional Delay Filter
FE	Front-End
FPGA	Field-Programmable Gate Array
FTE	Full Time Equivalent
HDL	Hardware Description Language

IF	Intermediate Frequency
IFDC	IF Down Converter
JESD	JEDEC standard
LAB	Laboratoire d'Astrophysique de Bordeaux
LDO	Linear Dropout regulator
LO	Local Oscillator
LSB	Least Significant Bit
MUX	Multiplexer
NASA	National Aeronautics and Space Administration
NRAO	National Radio Astronomy Observatory
OPFB	Oversampled Polyphase Filter Bank
OSF	Operations Site Facility
PAM	Pulse Amplitude Modulation
PCB	Printed Circuit Board
PSD	Power Spectral Density
PLL	Phase-Locked Loop
QSFP-DD	Quad Small Form-factor Pluggable Double Density
RMS	Root Mean Square
RX	Receiver
SCC	Station Control Card
SFP+	Small Form-Factor Pluggable
SKA	Square Kilometer Array
SNR	Signal to Noise Ratio
TFB	Tunable Filter Bank
TX	Transmitter
VCO	Voltage Controlled Oscillator
XCVR	Transceiver
WDM	Wavelength Division Multiplexing